F71889A

Super Hardware Monitor + LPC I/O

Release Date: Sep, 2011
Version: V0.21P

F71889A Datasheet Revision History

Version	Date	Page	Revision History
V0.10P	2010/4	-	Preliminary Version.
V0.11P ~ V0.19P	2010/5 ~ 2011/6	-	Shorten history description
V0.20P	2011/7/18	72-73	Add USBEN/VCCGATE timing and SUSC# timing Protection Mode Configuration Register — Index 02h, bit 3
V0.21P	2011/9/14		Made Correction & Clarification Update VIN3 (pin96) description

Table of Content

1. General Description

The F71889A which is the featured IO chip for new generational PC system is equipped with one IEEE 1284 parallel port, two UART ports, KBC, 80-Port (multi with COM2), CIR with RC6 and SMK QP protocols supported and 54 GPIO pins. The F71889A integrated with hardware monitor, 9 sets of voltage sensor, 3 sets of creative auto-controlling fans and 3 temperature sensor pins for the accurate dual current type temp. measurement for CPU thermal diode or external transistors 2N3906.

The F71889A provides flexible features for multi-directional application. For instance, IRQ sharing function also designed in UART feature for particular usage and accurate current mode H/W monitor will be worth in measurement of temperature, provides 3 modes fan speed control mechanism included Manual Mode/Speed Mode/Temperature Mode for users' selection.

Additionally, integrated 80-Port, and 5VDUAL voltage switch and adjustable voltage reference outputs related functions. The 80-Port is for engineering and debuging usage. F71889A also provides 5V dual controller and some voltage reference outputs for system application. Others, the F71889A supports newest AMD new interface TSI and Intel PECI 3.0 /SST interfaces and INTEL IBX PEAK SMBus for temperature reading. These features will help you more and improve product value.

In order to save the current consumption when the system is in the soft off state which is so called power saving function. The power saving function supports the system boot-on not only by pressing the power button but also by the wake-up events (GPIO5x, CIR, RI#) . When the system enters the S3/S4/S5 state, F71889A can cut off the VSB power rail which supplies power source to the devices like the LAN chip, the chipset, the SIO, the audio codec, DRAM, and etc. The PC system can be simulated to G3-like state when the system enters S3/S4/S5 states. At the G3-like state, the F71889A consumes 5VSB power rail only. The integrated two control pins are utilized to turn on or off VSB power rail in the G3-like status. The turned on VSB rail is supplied to a wake up device to fulfill a low power consumption system which supports a wake up function.

Finally, the F71889A is powered by 3.3V voltage, with the LPC interface in the package of 128-LQFP (14mm*14mm) green package.

2. Feature List

General Functions

- ✓ Comply with LPC Spec. 1.1
- ✓ Support DPM (Device Power Management), ACPI
- ✓ Provides two UARTs, KBC and Parallel Port

- ✓ H/W monitor functions
- ✓ Support OVP & UVP for VCC and VIN 5/6
- ✓ Reference voltage outputs support
- ✓ 5VDUAL voltage switch
- ✓ Support AMD TSI interface and Intel SST interface
- ✓ Support PECI Spec.3.0
- ✓ Support CIR with RC6 and SMK QP protocols
- ✓ Support IBX protocol SMBus interface
- ✓ 80-Port interface from COM2
- ✓ Support LED blinking function at deep S5
- ✓ 54 GPIO Pins for flexible application
- ✓ Provide Power Saving Funtion (Comply ERP lot 6.0)
- ✓ Support Intel Cougar Point Timing Sequence
- ✓ 24/48 MHz clock input
- ✓ Packaged in 128-LQFP green package and powered by 3.3VCC

UART

- ✓ Two high-speed 16C550 compatible UART with 16-byte FIFOs
- ✓ Fully programmable serial-interface characteristics
- ✓ Baud rate up to 115.2K
- ✓ Support IRQ sharing

80-Port Interface

- ✓ Monitor 0x80 Port and output the value via signals defined for 7-segment display.
- ✓ High nibble and low nibble are outputted interleaved at 1KHz frequency.
- ✓ 80-Port output by COM2 interface.

Parallel Port

- ✓ One PS/2 compatible bi-directional parallel port
- ✓ Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- ✓ Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- ✓ Enhanced printer port back-drive current protection

Hardware Monitor Functions

- ✓ 3 dual current type (±3℃) thermal inputs for CPU thermal diode and 2N3906 transistors
- ✓ Temperature range -40℃~127℃
- ✓ 9 sets voltage monitoring (6 external and 3 internal powers)
- ✓ High limit signal (PME#) for Vcore level

- ✓ 3 fan speed monitoring inputs
- ✓ 3 fan speed PWM/DC control outputs(support 3 wire and 4 wire fans)
- ✓ Issue PME# and OVT# hardware signals output
- ✓ Case intrusion detection circuit
- ✓ WATCHDOG# comparison of all monitored values

Keyboard Controller

- ✓ Compatibility with the 8042
- ✓ Support PS/2 mouse
- ✓ Support both interrupt and polling modes
- ✓ Hardware Gate A20 and Hardware Keyboard Reset

GPIO

- ✓ GPIO 53 and GPIO 54 can control the duty of PWM pin
- ✓ 54 GPIO pins for flexible application

System Volume Control

- ✓ GPIO 50, GPIO 51 and GPIO 52 can control the system volume & mute function by LPC interface
- ✓ Windows OSD can detect the system volume control input without any driver installation.

Infrared

- ✓ Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

CIR

- ✓ Support Microsoft Windows Vista / Windows 7 IR Receiver
- ✓ Support RC6 and Quatro Pulse protocols
- ✓ Support Learning Function
- ✓ Provide Data Receiver LED
- ✓ 2 IR Receiver with Long Range Frequency and Another with Wideband Application

Integrate AMD TSI interface

Integrate Intel SST interface

Support Intel Cougar Point Timing (DSW)

Support PECI 3.0

Support IBX Protocol SMBus interface

- **5V Dual Voltage Switch**
  - ✓ Provide ACPI-compliant 5VDUAL voltage switch
  - ✓ 5VDUAL for USB/Keyboard/Mouse application

- **Adjustable Voltage Reference Outputs**
  - ✓ Enable pin for VREF2 and 3 Voltage Reference Output control
  - ✓ 0.9V default output on VREF1~3 pins
  - ✓ Adjustable voltage range from 0~2.295V

- **Power Saving Function**
  - ✓ G3-like Timing Control
  - ✓ Comply With ERP Lot 6.0
  - ✓ Three Control Pins for VSB Power Sources Control
  - ✓ Two Event Input Pins for Wakeup Devices

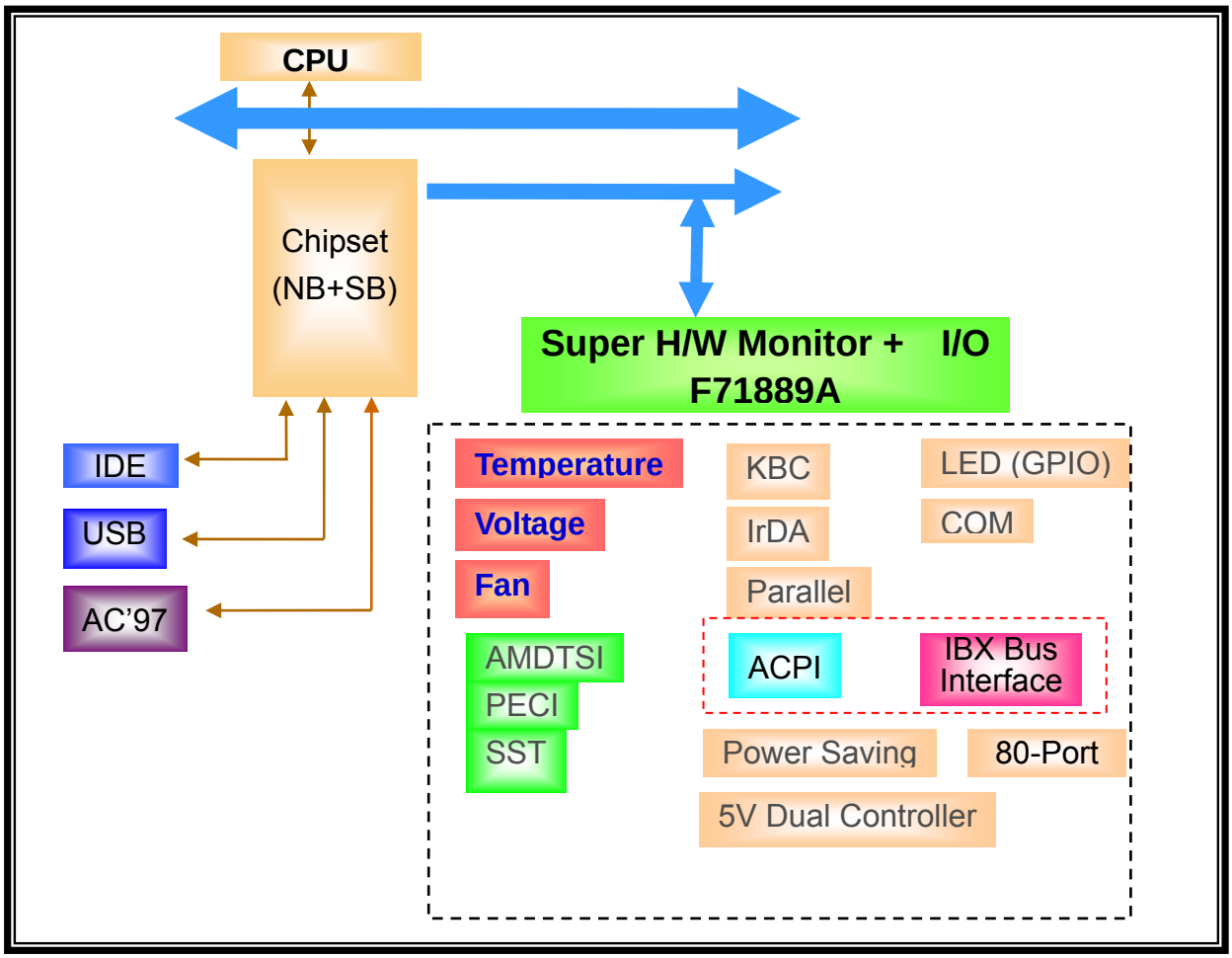
- **Package**
  - ✓ 128-pin LQFP (14mm * 14mm) green package

Noted: Patented TW207103 TW207104 TW220442 US6788131 B1 TWI235231 TW237183 TWI263778

3. Key Specification

Supply Voltage	3.0V to 3.6V
Operating Supply Current	10mA typ.

4. Block Diagram



5. Pin Configuration

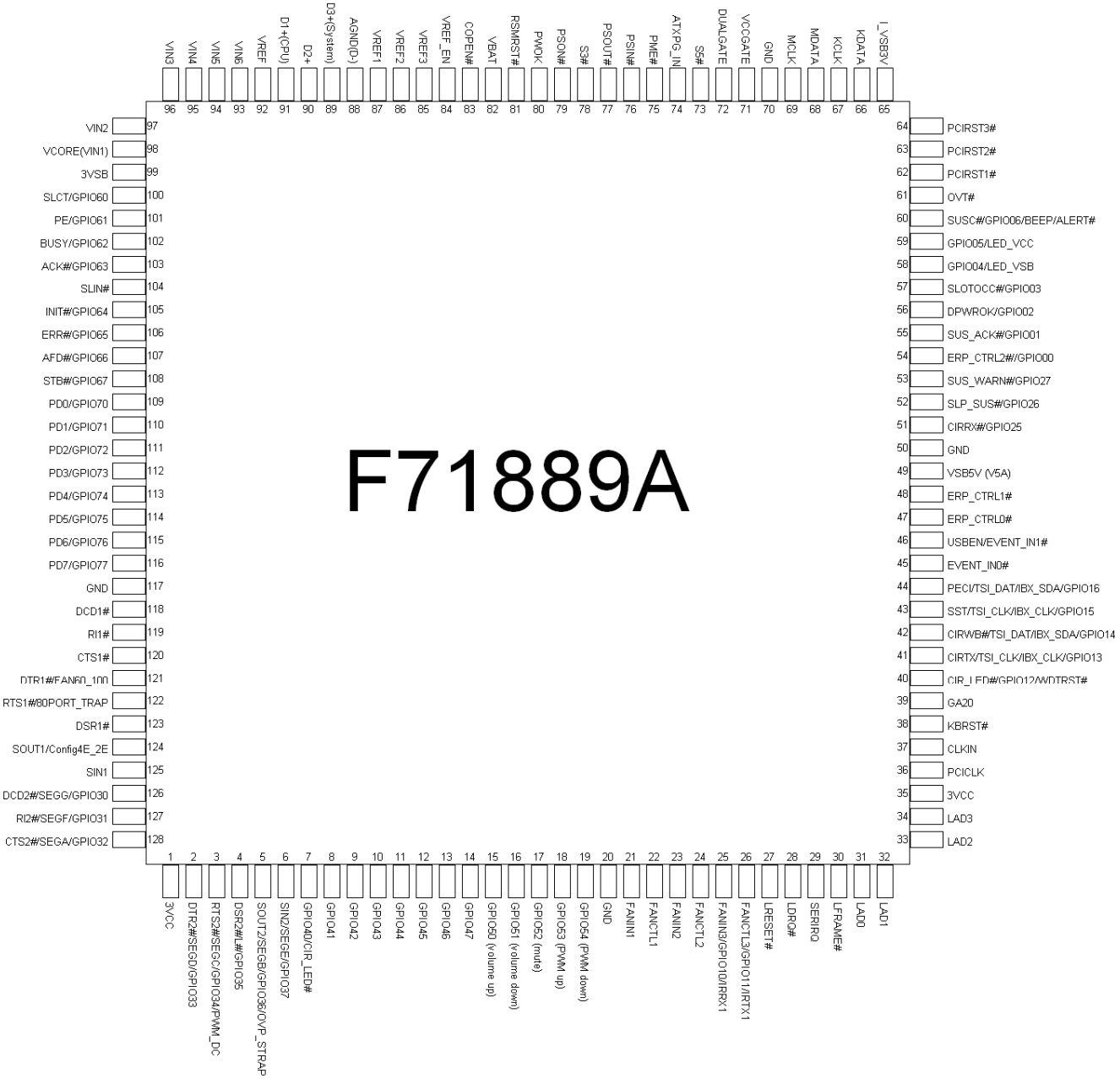


Figure1. F71889A pin configuration

6. Pin Description

I/O_{16t} - TTL level bi-directional pin with 16 mA source-sink cap ability.
I/OOD_{12t} - TTL level bi-directional pin, can select to OD or OUT by register, with 12 mA source-sink capability.
I/OOD_{18t} TTL level bi-directional pin, can select to OD or OUT by register, with 18 mA source-sink capability.
$I/OOD_{12st,lv}$ - Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.
$I/OOD_{12st,5v}$ - TTL bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability, 5V tolerance.
$I/OD_{16st,5v}$ - TTL level bi-directional pin and schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.
$OD_{16,u10,5v}$ - Open-drain output pin with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.
$I/O_{12st,5v}$ - TTL level bi-directional pin and schmitt trigger, output with 12 mA sink capability, 5V tolerance.
$I/O_{D8,st,lv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive
$I/O_{s1,D8st,lv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive and 1mA sink capability.
$I/OD_{12st,lv}$ - Low level bi-directional pin with schmitt trigger. Open-drain output with 12mA sink capability.
$O_{8,u47,5v}$ - Open-drain pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.
O_{12} - Output pin with 12 mA source-sink capability.
O_{16} - Output pin with 16 mA source-sink capability.
O_{18} - Output pin with 18 mA source-sink capability.
O_{30} - Output pin with 30 mA source-sink capability.
AOUT - Output pin(Analog).
OD_{12} - Open-drain output pin with 12 mA sink capability.
$OD_{12,5v}$ - Open-drain output pin with 12 mA sink capability, 5V tolerance.
O_{24} - Output pin with 24 mA sink capability.
I/OD_{14t} - TTL level bi-directional pin, Open-drain output with 14 mA sink capability.
$IN_{t,5v}$ - TTL level input pin,5V tolerance.
IN_{st} - TTL level input pin and schmitt trigger.
$IN_{st,5v}$ - TTL level input pin and schmitt trigger, 5V tolerance.
$IN_{st,lv}$ - TTL low level input pin (VIH → 0.9V, VIL → 0.6V.)
AIN - Input pin(Analog).
P - Power.

6.1 Power Pin

Pin No.	Pin Name	Type	Description
1,35	3VCC	P	3.3V power supply input which supports OVP & UVP.
49	VSB5V (V5A)	P	5V standby power supply input.
65	I_VSB3V	P	3.3V internal standby power regulates from VSB5V
82	VBAT	P	3.3V battery input
88	AGND(D-)	P	Analog GND
20, 50, 70, 117	GND	P	Digital GND
99	3VSB	P	Voltage Input for 3.3V VSB.

6.2 LPC Interface

Pin No.	Pin Name	Type	PWR	Description
27	LRESET#	$IN_{st,5v}$	3VCC	Reset signal. It can connect to PCIRST# signal on the host.
28	LDRQ#	O_{16}	3VCC	Encoded DMA Request signal.
29	SERIRQ	I/O_{16t}	3VCC	Serial IRQ input/Output.
30	LFRAME#	IN_{st}	3VCC	Indicates start of a new cycle or termination of a broken cycle.
31-34	LAD[0:3]	I/O_{16t}	3VCC	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
36	PCICLK	IN_{st}	3VCC	33MHz PCI clock input.
37	CLKIN	IN_{st}	3VCC	System clock input. According to the input frequency 24/48MHz.

6.3 UART, GPIO and 80-Port

Pin No.	Pin Name	Type	PWR	Description
7	GPIO40	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
	CIR_LED#	$OD_{12,\ 5v}$		LED for CIR to indicate receiver is receiving data.
8	GPIO41	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
9	GPIO42	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
10	GPIO43	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
11	GPIO44	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
12	GPIO45	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
13	GPIO46	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
14	GPIO47	OD_{16t}	I_VSB3V	General purpose IO. (Select by Register)
15	GPIO50	OD_{16t}	I_VSB3V	General purpose IO. Could be selected to Volume Up function via scan code register.
16	GPIO51	OD_{16t}	I_VSB3V	General purpose IO. Could be selected to Volume Down function via scan code register.
17	GPIO52	OD_{16t}	I_VSB3V	General purpose IO. Could be selected to MUTE function via scan code.
18	GPIO53	OD_{16t}	I_VSB3V	General purpose IO. Could be selected to PWM Up function via register.
19	GPIO54	OD_{16t}	I_VSB3V	General purpose IO. Could be selected to PWM Down function vis register.
118	DCD1#	$IN_{t,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
119	RI1#	$IN_{t,5v}$	3VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
120	CTS1#	$IN_{t,5v}$	3VCC	Clear To Send is the modem control input.
121	DTR1#	$O_{8,u47,5v}$	3VCC	UART 1 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.

	FAN60_100	$IN_{t,5v}$		Power on strapping pin: 1(Default): (Internal pull high) Power on fan speed default duty is 60%.(PWM) 0: (External pull down) Power on fan speed default duty is 100%.(PWM)
122	RTS1#	$O_{8,u47,5v}$	3VCC	UART 1 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	80PORT_TRAP	$IN_{t,5v}$		Power on strapping pin: 1(Default) : Default 80-port enable (Internal pull high) 80 port decode output from COM2 interface 0 : Disable 80-port function
123	DSR1#	$IN_{t,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
124	SOUT1	$O_{8,u47,5v}$	3VCC	UART 1 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	Config4E_2E	$IN_{t,5v}$		Power on strapping: (Internal pull high) 1(Default): Configuration register →4E 0 : Configuration register →2E
125	SIN1	$IN_{t,5v}$	3VCC	Serial Input. Used to receive serial data through the communication link.
126	DCD2#	$IN_{t,5v}$	3VCC	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
	SEGG	O_{18}		SEGG for 7-segment display. (Select by pin 122 power on strapping)
	GPIO30	I/OOD_{18t}		General purpose IO. (Select by register)
127	RI2#	$IN_{t,5v}$	3VCC	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
	SEGF	O_{18}		SEGF for 7-segment display. (Select by pin 122 power on strapping)
	GPIO31	I/OOD_{18t}		General purpose IO. (Select by register)
128	CTS2#	$IN_{t,5v}$	3VCC	Clear To Send is the modem control input.
	SEGA	O_{18}		SEGA for 7-segment display. (Select by pin 122 power on strapping)
	GPIO32	I/OOD_{18t}		General purpose IO. (Select by register)
2	DTR2#	$O_{8,u47,5v}$	3VCC	UART 2 Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate. Internal 47k ohms pulled high and disable after power on strapping.
	SEGD	O_{18}		SEGD for 7-segment display. (Select by pin 122 power on strapping)
	GPIO33	I/OOD_{18t}		General purpose IO. (Select by register)
3	RTS2#	$O_{8,u47,5v}$	3VCC	UART 2 Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. Internal 47k ohms pulled high and disable after power on strapping.
	SEGC	O_{18}		SEGC for 7-segment display. (Select by pin 122 power on strapping)
	GPIO34	I/OOD_{18t}		General purpose IO. (Select by register)

	PWM_DC	$IN_{t,5v}$		Power on strapping : 1 (Default): Fan control method will be in PWM Mode 0 Drive :Fan control method will be in Linear Mode
4	DSR2#	$IN_{t,5v}$	3VCC	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
	L#	O_{30}		L# for 7-segment display. (Select by pin 122 power on strapping)
	GPIO35	I/OOD_{12t}		General purpose IO. (Select by register)
5	SOUT2	$O_{8,u47,5v}$	3VCC	UART 2 Serial Output. Used to transmit serial data out to the communication link. Internal 47k ohms pulled high and disable after power on strapping.
	SEGB	O_{18}		SEGB for 7-segment display. (Select by pin 122 power on strapping)
	GPIO36	I/OOD_{18t}		General purpose IO. (Select by register)
	OVP_STRAP	$IN_{t,5v}$		Power on Strapping pin for OVP/UVP protection function. 1: default is disabled alarm mode. Voltage protection function is enabled via setting the related register. 0: Force mode which is always enabled after power on.
6	SIN2	$IN_{t,5v}$	3VCC	Serial Input. Used to receive serial data through the communication link.
	SEGE	O_{18}		SEGE for 7-segment display. (Select by pin 122 power on strapping)
	GPIO37	I/OOD_{18t}		General purpose IO. (Select by register)

6.4 Parallel Port

Pin No.	Pin Name	Type	PWR	Description
100	SLCT	$IN_{st,5v}$	3VCC	An active high input on this pin indicates that the printer is selected. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	GPIO60	I/OOD_{12t}		General purpose IO.
101	PE	INst,5v	3VCC	An active high input on this pin indicates that the printer has detected the end of the paper. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO61	I/OOD_{12t}		General purpose IO.
102	BUSY	$IN_{st,5v}$	3VCC	An active high input indicates that the printer is not ready to receive data. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
	GPIO62	I/OOD_{12t}		General purpose IO.
103	ACK#	$IN_{st,5v}$	3VCC	An active low input on this pin indicates that the printer has received data and is ready to accept more data. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO63	I/OOD_{12t}		General purpose IO.
104	SLIN#	$I/OOD_{12,5v}$	3VCC	Output line for detection of printer selection. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.

105	INIT#	$I/OOD_{12,5v}$	3VCC	Output line for the printer initialization. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO64	I/OOD_{12t}		General purpose IO.
106	ERR#	$IN_{st,5v}$	3VCC	An active low input on this pin indicates that the printer has encountered an error condition. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO65	I/OOD_{12t}		General purpose IO.
107	AFD#	$I/OOD_{12,5v}$	3VCC	An active low output from this pin causes the printer to auto feed a line after a line is printed. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO66	I/OOD_{12t}		General purpose IO.
108	STB#	$I/OOD_{12,5v}$	3VCC	An active low output is used to latch the parallel data into the printer. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO67	I/OOD_{12t}		General purpose IO.
109	PD0	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
	GPIO70	I/OOD_{12t}		General purpose IO.
110	PD1	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 1.
	GPIO71	I/OOD_{12t}		General purpose IO.
111	PD2	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 2.
	GPIO72	I/OOD_{12t}		General purpose IO.
112	PD3	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 3.
	GPIO73	I/OOD_{12t}		General purpose IO.
113	PD4	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 4.
	GPIO74	I/OOD_{12t}		General purpose IO.
114	PD5	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 5.
	GPIO75	I/OOD_{12t}		General purpose IO.
115	PD6	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 6.
	GPIO76	I/OOD_{12t}		General purpose IO.
116	PD7	$I/O_{12st,5v}$	3VCC	Parallel port data bus bit 7.
	GPIO77	I/OOD_{12t}		General purpose IO.

6.5 Hardware Monitor, SIR, CIR, ERP

Pin No.	Pin Name	Type	PWR	Description
93-94	VIN6~VIN5	AIN	I_VSB3V	Voltage Input 6 ~ 5. Support OVP & UVP function, and default is disable.
95-97	VIN4~VIN2	AIN	I_VSB3V	Voltage Input 4 ~ 2. *Please connect VIN3 (Pin96) to 5VCC if USBEN/VCCGATE were used.(Be careful of the voltage input range 0~2.048) *If VIN3 is not used, pull high (4.7k) to 3VCC.
98	Vcore(VIN1)	AIN	I_VSB3V	Voltage Input for Vcore.
21	FANIN1	$IN_{st,5v}$	3VCC	Fan 1 tachometer input.
22	FANCTL1	$OD_{12,5v}$ AOUT	3VCC	Fan 1 control output. This pin provides PWM duty-cycle output or a voltage output.

23	FANIN2	$IN_{st,5,4v}$	3VCC	Fan 2 tachometer input.
24	FANCTL2	$OD_{12,5v}$ AOUT	3VCC	Fan 2 control output. This pin provides PWM duty-cycle output or a voltage output.
25	FANIN3	$IN_{st,5v}$	3VCC	Fan 3 speed input.
	GPIO10	I/OOD_{12t}		General purpose IO. (Select by Register)
	IRRX1	IN_{st}		Infrared Receiver input. (Select by Register)
26	FANCTL3	$OD_{12,5v}$ AOUT	3VCC	Fan 3 control output. The PWM output frequency can be programmed to 220Hz for LCD backlight control.
	GPIO11	I/OOD_{12t}		General purpose IO. (Select by Register)
	IRTX1	O_{12}		Infrared Transmitter Output. (Select by Register)
89	D3+(System)	AIN	I_VSB3V	Thermal diode/transistor temperature sensor input for system use.
90	D2+	AIN	I_VSB3V	Thermal diode/transistor temperature sensor input.
91	D1+(CPU)	AIN	I_VSB3V	CPU thermal diode/transistor temperature sensor input. This pin is for CPU use.
92	VREF	AOUT	I_VSB3V	Voltage sensor output.
75	PME#	$OD_{12,5v}$	I_VSB3V	Generated PME event. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the S3 state.
45	EVENT_IN0#	$IN_{st,5v}$	I_VSB3V	Wake-up event input. The signal input wakes the system up from the sleep state.
46	USBEN	O_{12}	I_VSB3V	USB Power Control Signal. **If USBEN was used, please connect Pin96 to 5VCC (Be careful of the voltage input range 0~2.048V.)
	EVENT_IN1#	$IN_{st,5v}$		Wake-up event input. The signal input wakes the system up from the sleep state.
47	ERP_CTRL0#	OD_{12}	I_VSB3V	Standby power rail control pin 0. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
48	ERP_CTRL1#	OD_{12}	I_VSB3V	Standby power rail control pin 1. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.
61	OVT#	$OD_{12,5v}$	I_VSB3V	Over temperature signal output.
40	CIR_LED#	$OD_{12,5v}$	3VCC	LED for CIR to indicate receiver is receiving data.
	GPIO12	I/OOD_{12t}		General purpose IO.
	WDTRST#	$OD_{12,5v}$		Watch dog timer signal output. (Selecty by register)
41	CIRTX	O_{20}	3VCC	CIR Transmitter to transmit data.
	TSI_CLK	$I/OD_{12st,lv}$		Clock output for AMD TSI interface. (Select by register)
	IBX_CLK	$I/OD_{12st,lv}$		Clock output for INTEL PCH (IBX Peak) interface. (Select by register)
	GPIO13	I/OOD_{12t}		General purpose IO. (Selecty by register)

42	CIRWB#	$IN_{st,5V}$	3VCC	CIR wide-band receiver input for learning function.
	TSI_DAT	$I/OD_{12st,lv}$		AMD TSI data interface. (Select by register)
	IBX_SDA	$I/OD_{12st,lv}$		INTEL PCH (IBX Peak) data interface pin. (Select by register)
	GPIO14	I/OOD_{12t}		General purpose IO. (Selecty by register)
43	SST	$I/O_{D8,st,lv}$	3VCC	Intel SST hardware monitor interface. (Default)
	TSI_CLK	$I/OD_{12st,lv}$		Clock output for AMD TSI interface. (Select by register)
	IBX_CLK	$I/OD_{12st,lv}$		Clock output for INTEL PCH (IBX Peak) interface. (Select by register)
	GPIO15	$I/OOD_{12st,lv}$		General purpose IO. (Selecty by register)
44	PECI	$I/O_{s1,D8st,lv}$	3VCC	Intel PECI hardware monitor interface. (Default)
	TSI_DAT	$I/OD_{12st,lv}$		AMD TSI data interface. (Select by register)
	IBX_SDA	$I/OD_{12st,lv}$		INTEL PCH (IBX Peak) data interface pin. (Select by register)
	GPIO16	$I/OOD_{12st,lv}$		General purpose IO. (Selecty by register)

6.6 KBC Function

Pin No.	Pin Name	Type	PWR	Description
38	KBRST#	$OD_{16,u10,5v}$	3VCC	Keyboard reset. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P20)
39	GA20	$OD_{16,u10,5v}$	3VCC	Gate A20 output. This pin is high after system reset. Internal pull high 3.3V with 10k ohms. (KBC P21)
66	KDATA	$I/OD_{16st,5v}$	I_VSB3V	Keyboard Data.
67	KCLK	$I/OD_{16st,5v}$	I_VSB3V	Keyboard Clock.
68	MDAT	$I/OD_{16st,5v}$	I_VSB3V	PS2 Mouse Data.
69	MCLK	$I/OD_{16st,5v}$	I_VSB3V	PS2 Mouse Clock.

6.7 CIR, GPIO, Others Function

Pin No.	Pin Name	Type	PWR	Description
51	CIRRX#	$IN_{st,5v}$	I_VSB3V	CIR long-range receiver input
	GPIO25	$I/OOD_{12st,lv}$		General purpose pin.
52	SLP_SUS#	$IN_{st,lv}$	I_VSB3V	This pin asserts low which comes from PCH to shut off suspend power rails externally to enhance power saving function.
	GPIO26	$I/OOD_{12st,lv}$		General purpose pin.
53	SUS_WARN#	$IN_{st,lv}$	I_VSB3V	This pin asserts low when the PCH is planning to enter the DSW power state. It can detect 5VDUAL level with delay setting supported.The delay time is 1ms~8S (default 4s)
	GPIO27	$I/OOD_{12st,lv}$		General purpose pin.
54	ERP_CTRL2#	OD_{12}	I_VSB3V	Standby power rail control pin 2. This pin controls an external PMOS to turn on or off the standby power rail. In the S5 state, the default is set to 1 to cut off the standby power rail.

	GPIO00	$I/OOD_{12st,lv}$		General purpose pin.
55	SUS_ACK#	$OOD_{16,5v}$	I_VSB3V	This pin must wait SUSWARN# signal for entering DSW power state.
	GPIO01	I/OOD_{12t}		General purpose pin.
56	DPWROK	$OD_{12,5v}$	VBAT	Resume Reset# function, It is power good signal of 5VSB which is delayed 66ms as 5VSB arrives at 4.4V. Couple this pin to PCH when system supports Intel DSW state function.
	GPIO02	I/OOD_{12t}	I_VSB3V	General purpose pin.
57	SLOTOCC#	$IN_{st,5v}$	I_VSB3V	CPU SLOTOCC# input.
	GPIO03	I/OOD_{12t}		General purpose pin.
58	GPIO04	I/OOD_{12t}	I_VSB3V	General purpose pin.
	LED_VSB	OOD_{12}		Power LED for VSB
59	GPIO05	I/OOD_{12t}	I_VSB3V	General purpose pin.
	LED_VCC	OOD_{12}		Power LED for VCC
60	SUSC#	O_{12}	I_VSB3V	S5 latch signal.
	GPIO06	I/OOD_{12t}		General purpose pin.
	BEEP	OD_{12}		Beep pin.
	ALERT#	OD_{12}		Alert a signal when something issues.

6.8 ACPI Function Pins

Pin No.	Pin Name	Type	PWR	Description
62	PCIRST1#	$OD_{12,5v}$	I_VSB3V	It is an output buffer of LRESET#.
63	PCIRST2#	O_{24}	I_VSB3V	It is an output buffer of LRESET#.
64	PCIRST3#	O_{24}	I_VSB3V	It is an output buffer of LRESET#.
71	VCCGATE	O_{12}	I_VSB3V	Driver output for 5VCC. Connect this pin to the gate of a suitable NMOS. **If VCCGATE was used, please connect Pin96 to 5VCC (Be careful of voltage input range 0~2.048V).
72	DUALGATE	OD_{12}	I_VSB3V	Driver output for 5VSB. Connect this pin to the gate of a suitable PMOS..
73	S5#	$IN_{st,5v}$	I_VSB3V	S5# input. This pin companies with S3# to indicate operating state from S0 to S3 and S4/S5 sleep states.
74	ATXPG_IN	$IN_{st,5v}$	I_VSB3V	ATX Power Good input.
76	PSIN#	$IN_{st,5v}$	I_VSB3V	Main power switch button input.
77	PSOUT#	$OD_{12,5v}$	I_VSB3V	Panel Switch Output. This pin is low active and pulse output. It is power on request output.
78	S3#	$IN_{st,5v}$	I_VSB3V	S3# Input: Main power on-off switch input.
79	PSON#	$OD_{12,5v}$	I_VSB3V	Power supply on-off control output. Connect to ATX power supply PS_ON# signal.
80	PWOK	$OD_{12,5v}$	VBAT	PWROK function, It is power good signal of VCC, which is delayed 100ms (default) as VCC arrives at 2.8V. It falls when S3# gets low.
81	RSMRST#	$OD_{12,5v}$	VBAT	Resume Reset# function, It is power good signal of 5VSB and 3VSB, which is delayed 66ms as 3VSB arrives at 2.95V. There is an option to set RSMRST#

				falls when 3VSB drops to 2.3V.
83	COPEN#	$IN_{st,5v}$	VBAT	Case Open Detection #. This pin is connected to a specially designed low power CMOS flip-flop back by the battery for case open state preservation during power loss.
84	VREF_EN	$IN_{st,5v}$	I_VSB3V	Reference Voltage DAC output enable pin. Input high to this pin to enable VREF2 and VREF3. On the contrary, VREF2 and VREF3 will be disabled when input low to this pin.
85	VREF3	AOUT	I_VSB3V	Deafault 0.9V reference voltage output. The on/off sequence of this pin can be controlled by S3#, S5#, and VREF_EN.
86	VREF2	AOUT	I_VSB3V	Deafault 0.9V reference voltage output. The on/off sequence of this pin can be controlled by S3#, S5#, and VREF_EN.
87	VREF1	AOUT	I_VSB3V	Deafault 0.9V reference voltage output. Deafault 0.9V reference voltage output. The on/off sequence of this pin can be controlled by S3# and S5#.

7. Function Description

7.1. Power on Strapping Option

The F71889A provides five pins for power on hardware strapping to select functions. Power on strapping value follows TTL voltage level. Below table describes how to set the functions you want.

Table1. Power on trap configuration

Pin No.	Symbol	Value	Description
3	PWM_DC	1	Fan control mode: PWM mode. (Default)
		0	Fan control mode: DAC mode.
5	OVP_STRAP	1	Default is disabled alarm mode. Voltage protection function is enabled via setting the related register.
		0	Force mode which is always enabled after power on.
121	FAN60_100	1	Fan full duty is 60%.(Default)
		0	Fan full duty is 100%.
122	80PORT_TRAP	1	Enable the 80 port function. (Default)
		0	Disable the 80 port function.
124	Config4E_2E	1	Configuration Register I/O port is 4E/4F. (Default)
		0	Configuration Register I/O port is 2E/2F.

7.2. Hardware Monitor

7.2.1 Voltage

For the 8-bit ADC has the 8mv LSB, the maximum input voltage of the analog pin is 2.048V. Therefore the voltage under 2.048V (ex:1.5V) can be directly connected to these analog inputs. The voltage higher than 2.048V should be reduced by a factor with external resistors so as to obtain the input range. Only 3Vcc is an exception for it is main power of the F71889A. Therefore 3Vcc can directly connect to this chip's power pin and need no external resistors. There are two functions in this pin with 3.3V. The first function is to supply internal analog power of the F71889A and the second function is that voltage with 3.3V is connected to internal serial resistors to monitor the +3.3V voltage. The internal serial resistors are two 150K ohm, so that the internal reduced voltage is half of +3.3V.

There are four voltage inputs in the F71889A and the voltage divided formula is shown as follows:

$$VIN = V_{+12V} \times \frac{R_2}{R_1 + R_2}$$ where V_{+12V} is the analog input voltage, for example as figure 1.

If we choose R1=27K, R2=5.1K, the exact input voltage for V+12v will be 1.907V, which is within the tolerance. As for application circuit, it can be refer to the figure shown as follows.

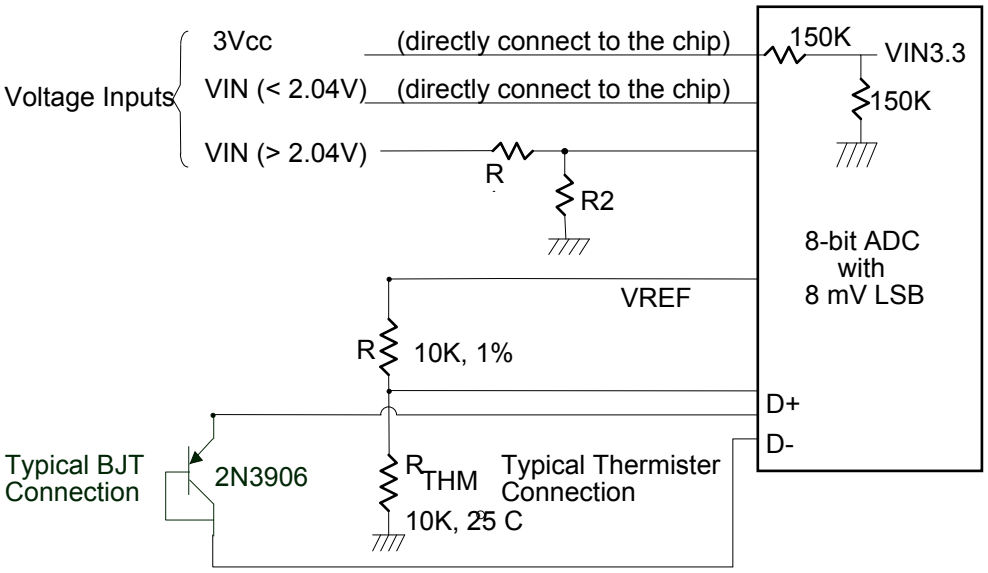


Figure 1. Hardware monitor configuration

PME# interrupt for voltage is shown as figure 2. Voltage exceeding or going below high limit will cause an interrupt if the previous interrupt has been reset by writing “1” all the interrupt Status Register. Voltage exceeding or going below low limit will result the same condition as voltage exceeding or going below high limit.

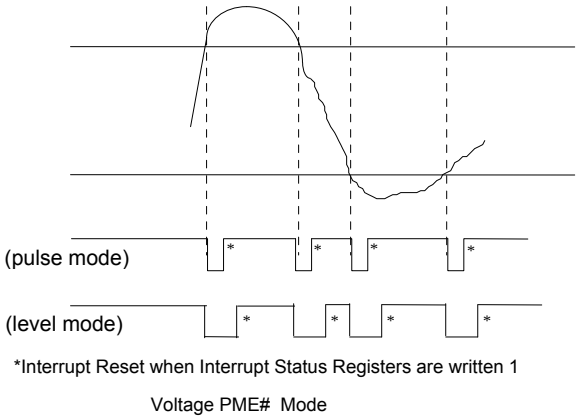


Figure 2

7.2.2 Temperature

The F71889A monitors three remote temperature sensors. These sensors can be measured from -40°C to 127°C. More detail please refer to the register description.

Table 1. Remote-sensor transistor manufacturers

Manufacturer	Model Number
Panasonic	2SB0709 2N3906
Philips	PMBT3906

Table 2. Display range is from -40°C to 127°C in 2's complement format.

Temperature	Digital Output
-40°C	1101 1000
-1°C	1111 1111
1°C	0000 0001
90°C	0101 1010
127°C	1111 1111
Open	1000 0000

Monitor Temperature from "thermistor"

The F71889A can connect three thermistors to measure environment temperature or remote temperature. The specification of thermistor should be considered to (1) value is 3435K (2) resistor value is 10K ohm at 25°C. In the Figure 7-1, the thermistor is connected by a serial resistor with 10K ohm, thenand then connected to VREF.

Monitor Temperature from "thermal diode"

Also, if the CPU, GPU or external circuits provide thermal diode for temperature measurement, the F71889A is capable to these situations. The build-in reference table is for PNP 2N3906 transistor, and each different kind of thermal diode should be matched with specific offset and BJT gain. In the Figure 7-1, the transistor is directly connected into temperature pins.

ADC Noise Filtering

The ADC is integrating type with inherently good noise rejection. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PCB board layout and suitable external filtering are required for high-accuracy remote measurement in electronically noisy environment. High frequency EMI is best filtered at D+ and D- with an external 2200pF or 3300pF capacitor. Too high capacitance may introduce errors due to the rise time of the switched current source. Nearly all noise sources tested cause the ADC measurement to be higher than the actual temperature, depending on the frequency and amplitude.

Monitor Temperature from "SMBus device"

F71889A provides SMBus block read/write compatible Platform Control Hub (PCH) EC SMBus protocol, and provides byte read/write protocol to read CPU and chipset thermal temperature

information. For byte read /write protocol, F71889A supports 4-suit device address to read or write from the device information. For block read/write, F71889A supports 1 suit of device address and maximum 17 byte count for read protocol to read from the device information, and 4 byte count for write protocol to write information to device.

Monitor Temperature from "PECI"

F71889A supports Intel PECI3.0 interface to read temperature from PECI device.

Over Temperature Signal (OVT#)

OVT# alert for temperature is shown as figure 7-3. When monitored temperature exceeds the over-temperature threshold value, OVT# will be asserted until the temperature goes below the hysteresis temperature.

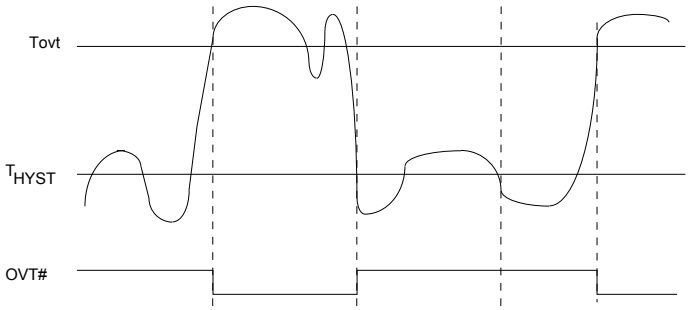
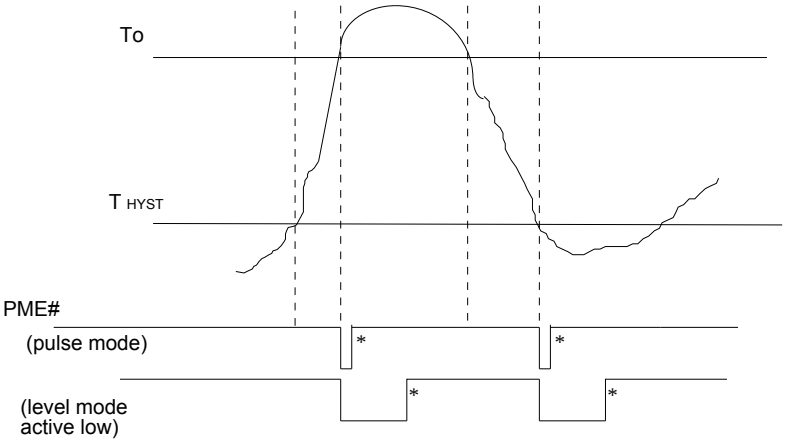


Figure 3

Temperature PME#

PME# interrupt for temperature is shown as figure 7-4. Temperature exceeding high limit or going below hysteresis will cause an interrupt if the previous interrupt has been reset by writing "1" all the interrupt Status Register.



*Interrupt Reset when Interrupt Status Registers are written 1

Figure 4

7.2.3 FAN

Fan speed count

Inputs are provided by the signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage cannot be over 5V. If the input signals from the tachometer outputs are over the 5V, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as follows:

Determine the fan counter according to:

$$\text{Count} = \frac{1.5 \times 10^6}{\text{RPM}}$$

In other words, the fan speed counter (12 bit resolution) has been read from register, the fan speed can be evaluated by the following equation.

$$\text{RPM} = \frac{1.5 \times 10^6}{\text{Count}}$$

As for fan, it would be best to use 2 pulses (4 phases fan) tachometer output per round. So the parameter “Count” under 5 bit filter is 4096~64 and RPM is 366~23438 based on above equation. If using 8 phases fan, RPM would be from 183~11719.

Fan speed control

The F71889A provides 2 fan speed control methods:

1. DAC FAN CONTROL 2. PWM DUTY CYCLE

DAC Fan Control

The range of DC output is 0~VCC, controlled by 8-bit register. 1 LSB is about 0.013V (VCC=3.3V). The output DC voltage is amplified by external OP circuit, thus to reach maximum FAN OPERATION VOLTAGE, 12V. The output voltage will be given as followed:

$$\text{Output\_voltage (V)} = \text{Vcc} \times \frac{\text{Programmed 8bit Register Value}}{256}$$

And the suggested application circuit for linear fan control would be:

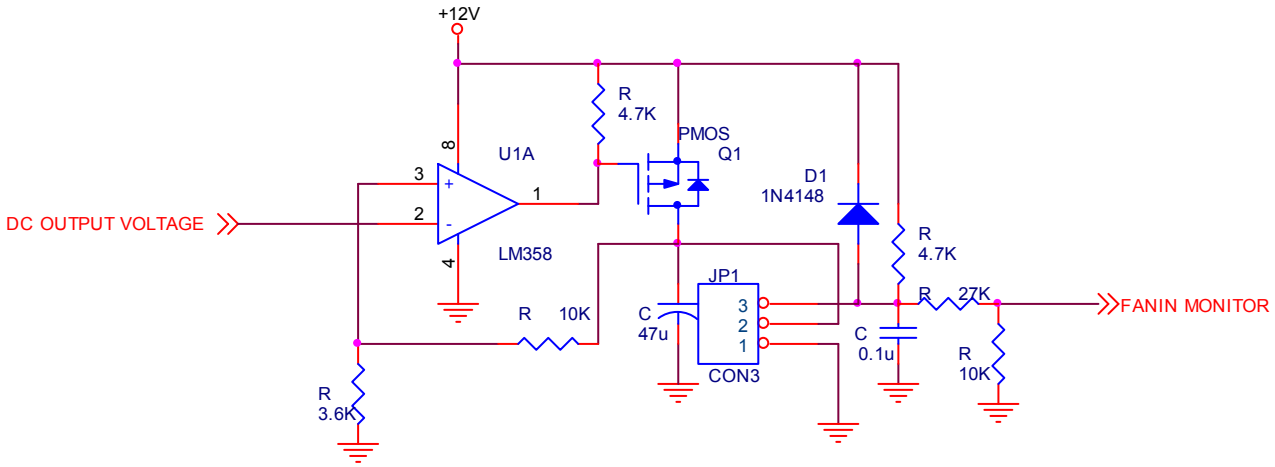


Figure 5 DAC fan control application circuit

PWM duty Fan Control

The duty cycle of PWM can be programmed by an 8-bit register. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty\_cycle(\%)} = \frac{\text{Programmed 8bit Register Value}}{255} \times 100\%$$

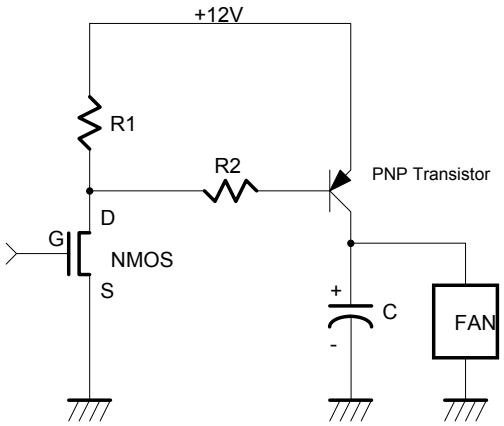


Figure 6 +12/5V PWM fan control application circuit

Fan speed control mechanism

There are some modes to control fan speed and they are 1.Manual mode, 2. Auto mode (Stage & Linear). More detail, please refer to the description of registers & below figure.

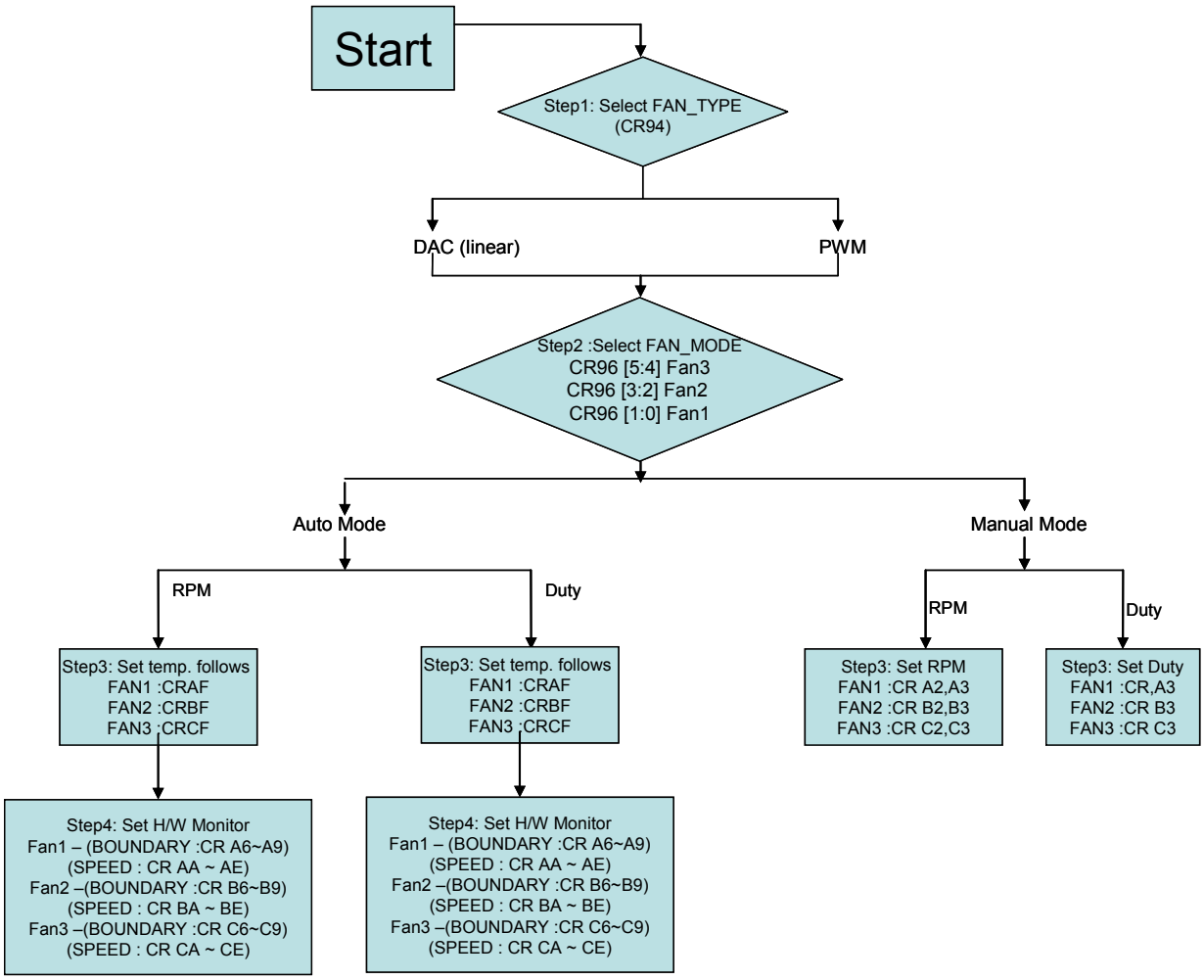


Figure 7 Fan type & mode selection flow

◆ **Manual mode**

For manual mode, it generally acts as software fan speed control.

◆ **Auto mode**

In auto mode, the F71889A provides automatic fan speed control related to temperature variation of CPU/GPU or the system. The F71889A can provide four temperature boundaries and five intervals, and each interval has its related fan speed count. All these values should be set by BIOS first. Take FAN1 for example, the 4 temperature boundaries could be set from register 0xA6 to 0xA9 and the five intervals for fan speed control could be set from register 0xAA to 0xAE. And the hysteresis setting (0 ~ 15°C) could also be found in register 0x98.

There are two kinds of auto mode: stage auto mode and linear auto mode.

The “FAN1_INTERPOLATION_EN” in register 0xAFh is used for linear auto mode enable. The following examples explain the differences for stage auto mode and linear auto mode.

- **Stage auto mode**

In this mode, the fan keeps in a same speed for each temperature interval. And there are two types of fan speed setting: PWM Duty and RPM %.

A. Stage auto mode (PWM Duty)

Set temperature as 70°C, 60°C, 50°C, 40°C and the duty as 100%, 90%, 80%, 70%, 60%

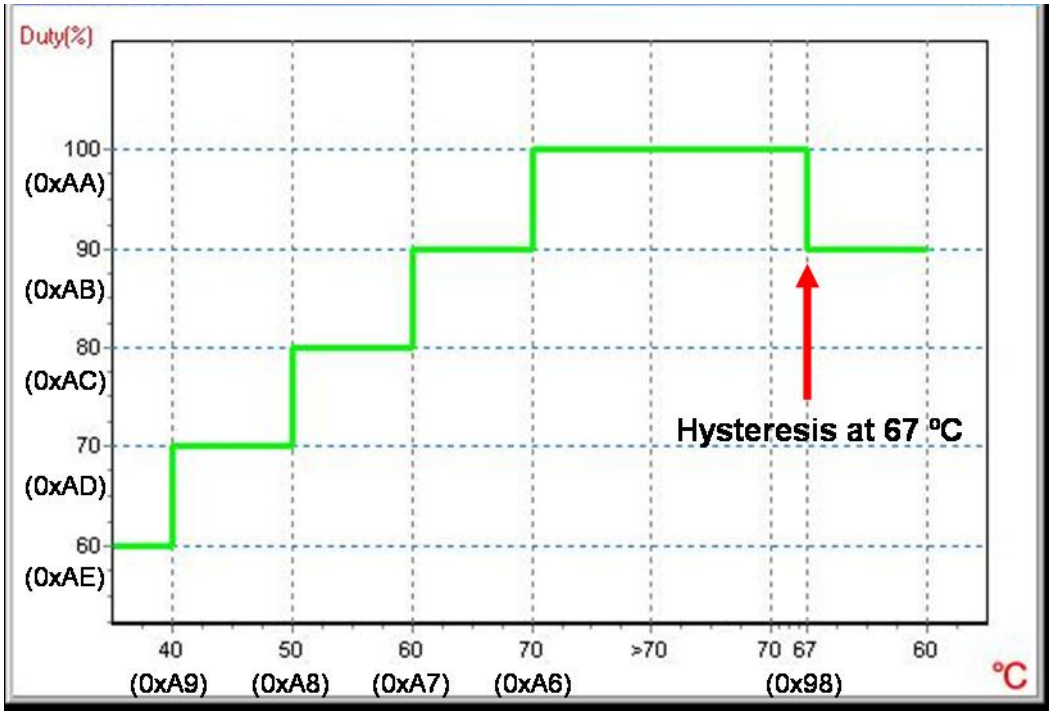


Figure 8 Stage mode fan control illustration-2

a. Once the temperature is under 40°C, the lowest fan speed keeps in the 60% PWM duty.

b. Once the temperature is over 40°C, 50°Cand 60°C, the fan speed will vary from 70%, 80% to 90% PWM duty and increasing with the temperature level.

c. For the temperature higher than 70°C, the fan speed keeps in 100% PWM duty.

d. If set the hysteresis is 3°C (default 4°C), once the temperature becomes lower than 67°C, the fan speed would reduce to 90% PWM duty.

B. Stage auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 RPM, 5,400 RPM, 4,800 RPM, 4,200 RPM, and 3,600 RPM (assume the Max Fan Speed is 6,000 RPM).

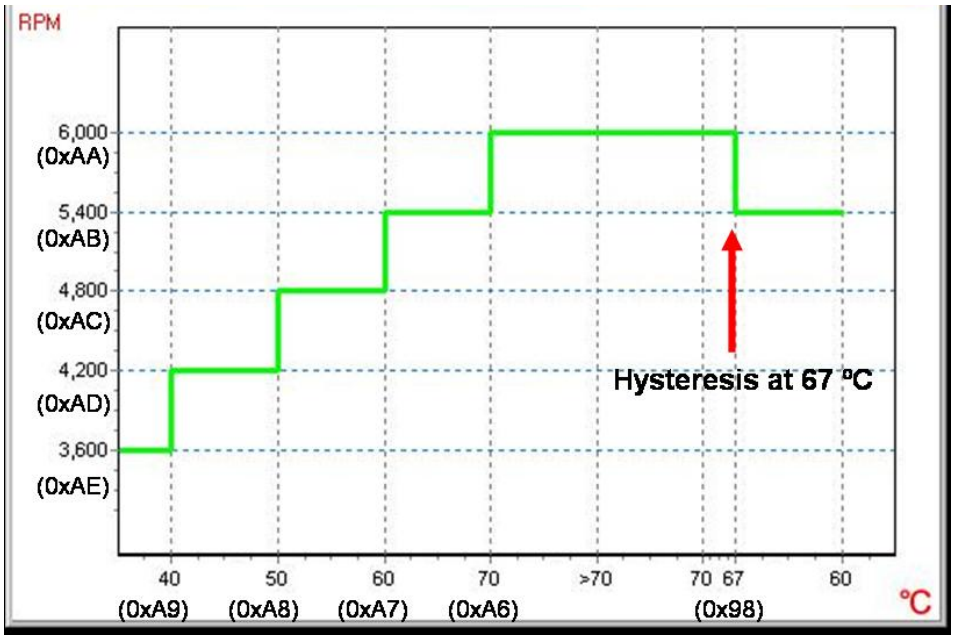


Figure 9 Stage mode fan control illustration-3

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,600 RPM (60% of full speed).

b. Once the temperature is higher than 40°C, 50°C and 60°C, the fan speed will vary from 4,200 RPM to 5,400 RPM and increasing with the temperature level.

c. For the temperature higher than 70°C, the fan speed keeps in the full speed 6,000 RPM.

d. If the hysteresis is set as 3°C (default 4°C), once temperature gets lower than 67°C, the fan speed would reduce to 5,400 RPM.

- **Linear auto mode**

F71889A also supports linear auto mode. The fan speed would increase or decrease linearly with the temperature. There are also PWM Duty and RPM% modes for it.

A. Linear auto mode (PWM Duty)

Set the temperature as 70°C, 60°C, 50°C and 40°C and the duty is 100%, 80%, 70%, 60% and 50%.

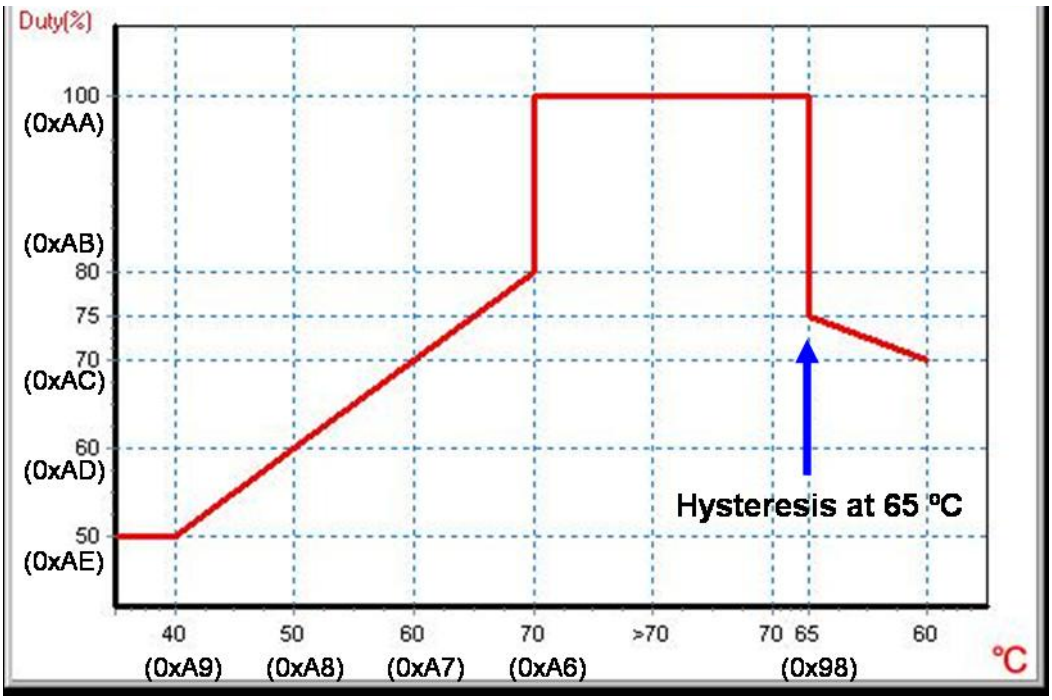


Figure 10 Linear mode fan control illustration-1

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in the 50% PWM duty
b. Once the temperature becomes higher than 40°C, 50°C and 60°C, the fan speed will vary from 50% to 80% PWM duty linearly with the tempreature variation. The temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to 100% PWM duty (full speed).
d. If set the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed will reduce from 100% PWM duty and decrease linearly with the temperature.

B. Linear auto mode (RPM%)

Set the temperature as 70°C, 60°C, 50°C, 40°C and the corresponding fan speed is 6,000 RPM, 4,800 RPM, 4,200 RPM, 3,600 RPM and 3,000 RPM (assume the Max Fan Speed is 6,000 RPM).

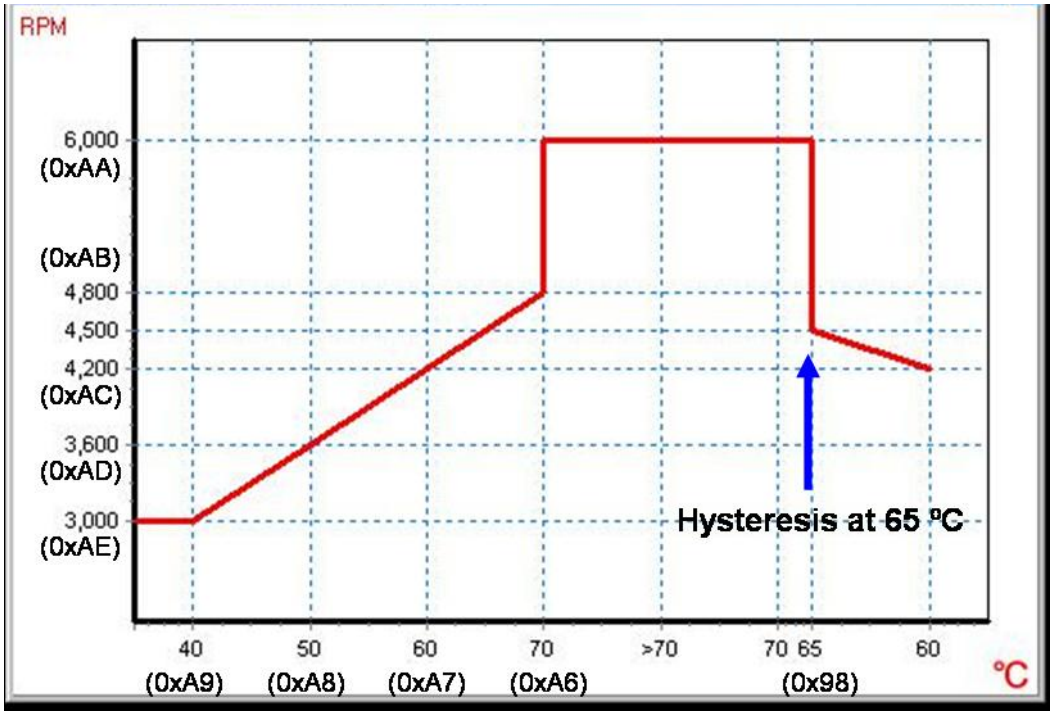


Figure 11 Linear mode fan control illustration-2

a. Once the temperature is lower than 40°C, the lowest fan speed keeps in 3,000 RPM (50% of full speed).
b. Once the temperature is over 40°C,50°C and 60°C, the fan speed will vary from 3,000 to 4,800 RPM almost linearly with the temperature variation because the temp.-fan speed monitoring flash interval is 1sec.
c. Once the temperature goes over 70°C, the fan speed will directly increase to full speed 6,000 RPM.
d. If the hysteresis is 5°C (default is 4°C), once the temperature becomes lower than 65°C (instead of 70°C), the fan speed wull reduce from full speed and decrease linearly with the temperature.

PWMOUT Duty-cycle operating process

In both “Manual RPM” and “Temperature RPM” modes, the F71889A adjust PWMOUT duty-cycle according to current fan count and expected fan count. It will operate as follows:

(1). When expected count is 0xFFF, PWMOUT duty-cycle will be set to 0x00 to turn off fan.
(2). When expected count is 0x000, PWMOUT duty-cycle will be set to 0xFF to turn on fan with full speed.
(3). If both (1) and (2) are not true,
(4). When PWMOUT duty-cycle decrease to MIN_DUTY(≠ 00h), obviously the duty-cycle will decrease to 00h. Then the F71889A will keep duty-cycle at 00h for 1.6 seconds. After that,

the F71889A starts to compare current fan count and expected count in order to increase or decrease its duty-cycle. This ensures that if there is any glitch during the period, the F71889A will ignore it.

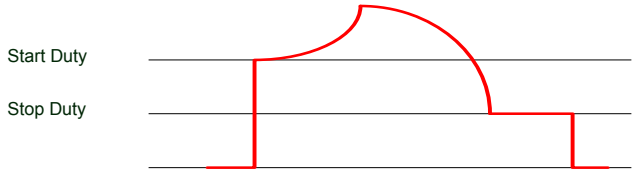


Figure 12

Fan Speed Control with Multi-temperature.

F71889A supports Multi-temperature for one Fan control. Each fan can be controlled up to 8 kinds of temperature inputs: (1) D1+ temperature (2) D2+ temperature (3) D3+ temperature (4) PECI temperature (5) 4 suits IBX temperatures. Each fan would make the maximum temperature comparison form those inputs with the expected speed, and decide the suitable fan speed. Please refer below figure 7-13.

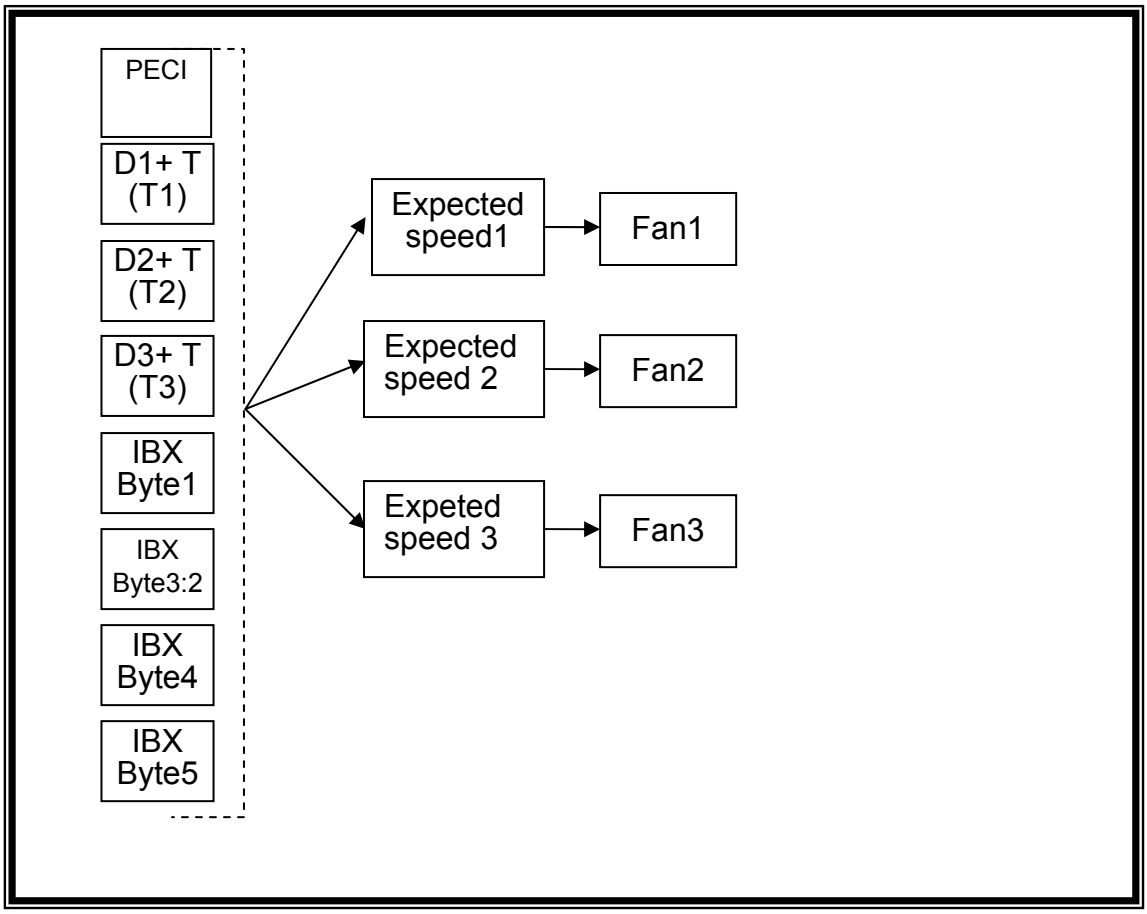


Figure 13 Relative temperature fan control

This function works with linear auto mode which can extend to two linear slopes for one Fan control (for Fan 1 only). As below graph shows, this machine can support more silence fan

control in low temperature and high fan speed in high temperature segment. More detail setting please refers to the related registers.

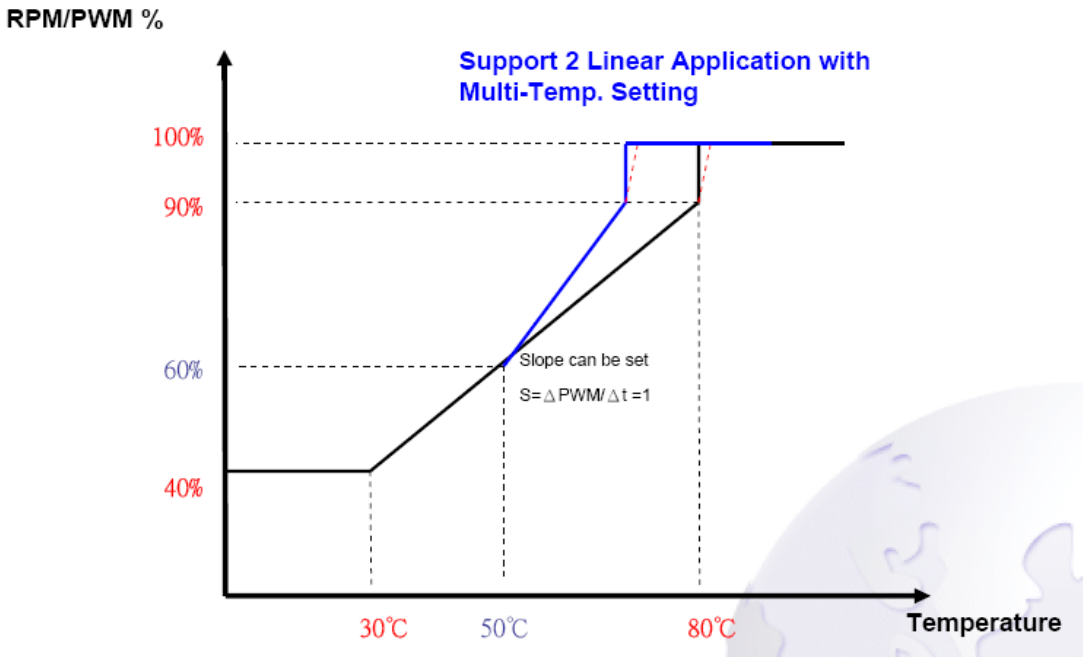


Figure 14

In the figure below, TFan1 is the scaled temperature for fan1. T1 is the real temperature for the fan1 sensor. Ta is another temperature data which can be used for linearly scale up or scale down the fan1 speed curve. Tb would be the point which starts the temperature scaling. The slope for the temperature curve over and under Tb would be Ctup and Ctdn.

TFan1= T1 + (Ta-Tb)*Ctup

TFan1= T1 + (Ta-Tb)*Ctdn

1. **Ctup**, **Ctdn** Can be Programmed to **1, ½, ¼, 0**
2. **Ta** Can be Selected to the Same Temp. Source (Ex:T1)

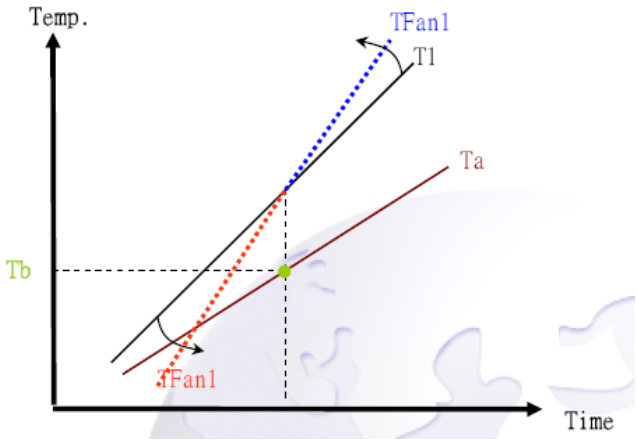


Figure 15

In application, we can set the Ta as the 2nd sensor temperature and Tb as the temperature which starts the scaling. So if the 2nd sensor temperature Ta is higher or lower than Tb, the fan1 speed would be changed with it.

EX: Ta = T1, Tb = 60, Ctu = 1, Ctd = 1/4

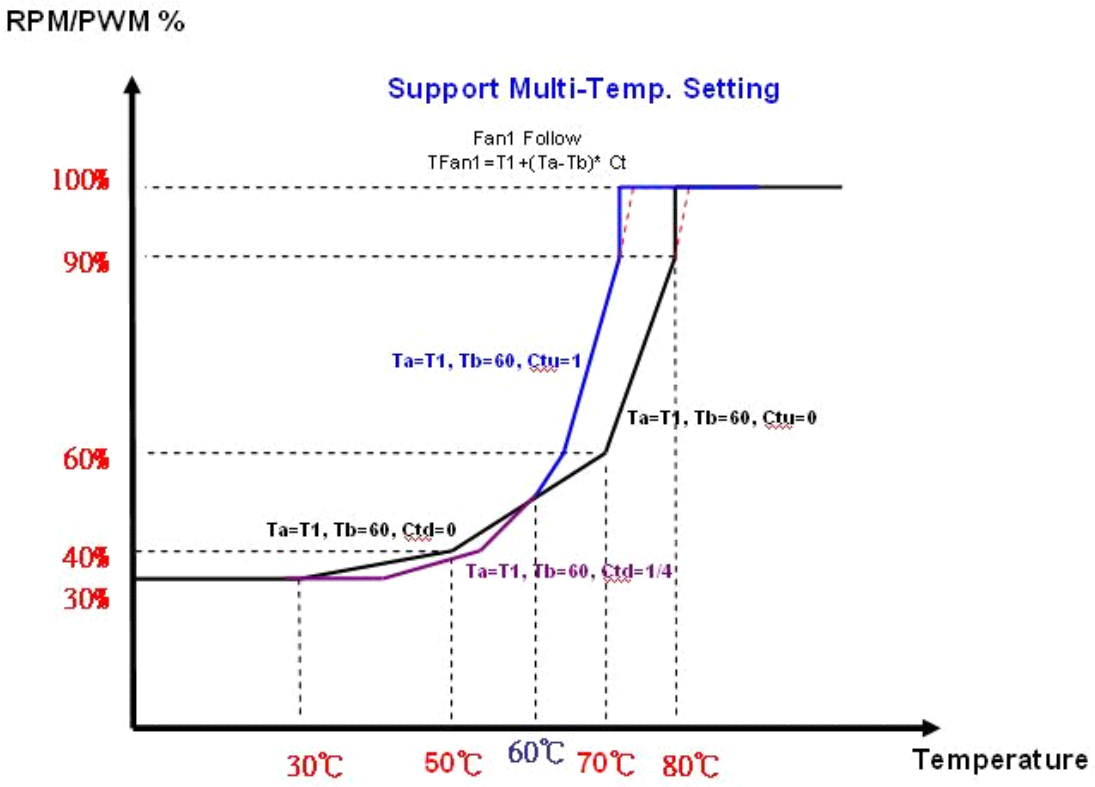


Figure 16

FAN_FAULT#

Fan_Fault# will be asserted when the fan speed doesn't meet the expected fan speed within a programmable period (default is 11 seconds) or when fan stops with respect to PWM duty-cycle which should be able to turn on the fan. There are two conditions may cause the FAN_FAULT# event.

(1). When PWM_Duty reaches 0xFF, the fan speed count can't reach the fan expected count in time.

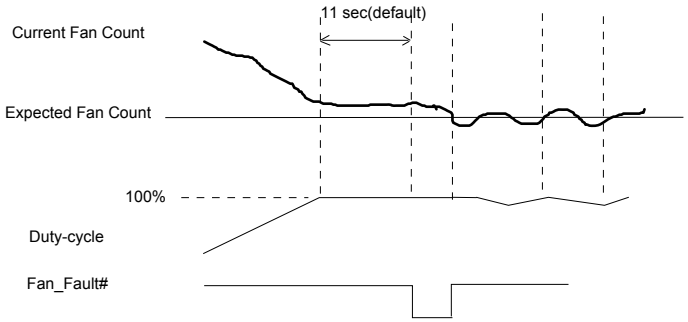


Figure 17 FAN_FAULT# event

(2). After the period of detecting fan full speed, when PWM_Duty > Min. Duty, and fan count still in 0xFFF.

Over Voltage Protection

F71889A OVP/UVP protection function could protect the damage from voltage spikes via over voltage & under voltage protection (OVP & UVP) function. Hardware strapping pin 5 default is disabled alarm mode. Voltage protection function is enabled via setting the related register. When force mode occurs, the system would shut down and then can not boot at all. Only re-plugging the power code (cut off VSB) could re-activate or re-boot the system at the force mode. Please see below table for detail information:

7.3. Hardware Monitor Register

The F71889A implement the Intel PECI/SST interface and AMD TSI interface to collect the CPU temperature for fan control. The CPU temperature source could be programmed to be from external diode, Intel PECI interface or AMD TSI interface.

Device registers: the following is a register map order which shows a summary of all registers. Please refer to each register if you need more detail information.

Register CR01 → Configuration Registers

Register CR02 ~ CR03 → Protection Mode & Case Open Status Registers

Register CR04 → Debug Port Temp. Registers

Register CR07 → PECI/SST/TSI Configuration Registers

Register CR08 →TSI Control Registers

Register CR09 →TSI Offset Registers

Register CR0A ~ CR0F → PECI/SST/Voltage Registers

Register CR10 ~ CR3F → Voltage Setting Registers

Register CR40 ~ CR4F → PECI 3.0 Command & Registers

Register CR60 ~ CR8E → Temperature Setting Registers

Register CR90 ~ CRCF → Fan Control Setting Registers

→Fan1 Detail Setting CRA0 ~ CRAF

→Fan2 Detail Setting CRB0 ~ CRBF

→Fan3 Detail Setting CRC0 ~ CRCF

Register CRE0 ~ CREF → TSI Temperature Registers

Register CR5A ~ CR5D → HW Chip ID and Vender ID Registers

Configuration Register – Index 01h

Bit	Name	R/W	Default	Description
7	BETA_EN	R/W	1	0: disable the T1 beta compensation. 1: enable the T1 beta compensation.
6	INTEL_MODEL	R/W	1	0: AMD TSI model. 1: Intel model.
5	TSI_EN	R/W	0	0: Disable the TSI function via PECI/SST pins. 1: Enable the TSI function via PECI/SST pins. This bit accompanying with INTEL_MODEL and SST_EN will determine the availability of AMD TSI, Intel PCH SMBus, PECI and SST (This bit is cleared by LRESET#). See below table:

Setting (CR07[1]-- NEW_MODE_EN = 0)						Results			
INTEL_MODEL (CR01, bit6)	TSI_EN (CR01, bit5)	SST_EN (CR0A, bit4)	TSI_ALT_EN (CR07, bit3)	PECI_EN (CR07, bit2)	NEW_TSI_EN (CR07, bit0)	PECI	SST	AMD TSI	Intel PCH SMBus
0	0	X	X	X	X	N	N	N	N
0	1	X	X	X	X	N	N	Y	N
1	0	0	X	X	X	Y	N	N	N
1	0	1	X	X	X	Y	Y	N	N
1	1	X	X	X	X	N	N	N	Y

Setting (CR07[1]-- NEW_MODE_EN = 1)						Results			
INTEL_MODEL (CR01, bit6)	TSI_EN (CR01, bit5)	SST_EN (CR0A, bit4)	TSI_ALT_EN (CR07, bit3)	PECI_EN (CR07, bit2)	NEW_TSI_EN (CR07, bit0)	PECI	SST	AMD TSI	Intel PCH SMBus
0	0	X	X	X	X	N	N	N	N
0	1	X	X	X	0	N	N	Y	N
1	1	0	X	0	1	N	N	Y	N
1	1	1	1	1	1	Y	Y	Y	N
1	1	1	1	1	0	Y	Y	N	Y
0	1	X	0	X	1	N	N	N	Y
1	X	1	X	1	X	Y	Y	N	N

4-3	Reserved	-	-	Reserved
2	POWER_DOWN	R/W	0	Hardware monitor function power down.
1	FAN_START	R/W	1	Set one to enable startup of fan monitoring operations; a zero puts the part in standby mode.
0	V_T_START	R/W	1	Set one to enable startup of temperature and voltage monitoring operations; a zero puts the part in standby mode.

Protection Mode Configuration Register — Index 02h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Dummy register.
6	CASE_BEEP_EN	R/W	0	0: Disable case open event output via BEEP. 1: Enable case open event output via BEEP.

5-4	OVT_MODE	R/W	0	00: The OVT# will be low active level mode. 01: The OVT# will be low pulse mode. (200us low pulse). 10: The OVT# will indicate by 1Hz LED function. 11: The OVT# will indicate by (400/800HZ) BEEP output.
3	SST_ Invert	R/W	0	0:Normal SST 1:SST_Invert
2	CASE_SMI_EN	R/W	0	0: Disable case open event output via PME. 1: Enable case open event output via PME.
1-0	ALERT_MODE	R/W	0	00: The ALERT# will be low active level mode. 01: The ALERT# will be high active level mode. 10: The ALERT# will indicate by 1Hz LED function. 11: The ALERT# will indicate by (400/800HZ) BEEP output.

Case Status Register — Index 03h

Bit	Name	R/W	Default	Description
7-1	Reserved	R/W	0	Return 0 when read.
0	CASE_STS	R/W	1	Case open event status, write 1 to clear if case open event cleared.

Debug Port Temp Register — Index 04h

Bit	Name	R/W	Default	Description
7-2	Reserved	R/W	0	Return 0 when read.
1-0	DPORT_TEMP_SEL	R/W	01	Debug port temperature source select: 00: 0xff. 01: T1 reading. 10: T2 reading. 11: T3 reading.

PECI/SST/TSI Configuration Register — Index 07h

Bit	Name	R/W	Default	Description
7-5	Reserved	R/W	0	Return 0 when read.
4	DIG_T1_SEL	R/W	0	This bit is used to select AMD TSI/Intel IBX or PECI to be the T1 temperature when NEW_MODE_EN is set to 1.
3	IBX_ALT_EN	R/W	0	This bit is used to control the AMD TSI/Intel IBX/PECI function. (see configuration register 0x00)
2	PECI_EN	R/W	0	This bit is used to control the AMD TSI/Intel IBX/PECI function. (see configuration register 0x00)
1	NEW_MODE_EN	R/W	0	This bit is used to control the AMD TSI/Intel IBX/PECI function. (see configuration register 0x00)
0	NEW_TSI_EN	R/W	0	This bit is used to control the AMD TSI/Intel IBX/PECI function. (see configuration register 0x00)

TSI Control Register — Index 08h

Bit	Name	R/W	Default	Description
7	Reserved	-	0	Reserved.
6	TSI_OFFSET_SEL	R/W	0	Set this bit to select the offset of AMD TSI/Intel IBX. 0: TCC_TEMP in CR0C 1: TSI_OFFSET in CR09
5-4	Reserved	-	0	Reserved.

3	TSI 02_SEL	R/W	0	If this bit is set to 1, CR7B is able to be written and can also be used to control fan.
2	TSI 01_SEL	R/W	0	If this bit is set to 1, CR7A is able to be written and can also be used to control fan.
1-0	Reserved	-	0	Reserved.

TSI Offset Register — Index 08h

Bit	Name	R/W	Default	Description
7-0	TSI_OFFSET	R/W	0	When PECI and AMD TSI/Intel IBX are enabled at the same time, this byte is used as the offset to be added to the CPU temperature reading of AMD_TSI/Intel IBX. To using this byte as offset of AMD TSI/Intel IBX CPU temperature reading, the TSI_OFFSET_SEL in CR08 must be set to 1. The range of this register is -128 ~ 127.

SST and VTT_SEL Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-5	Reserved	-	0	Reserved.
4	SST_EN_REG	R/W	0	Set this bit “1” and select Intel model will enable SST interface. Otherwise will disable SST interface This bit is cleared by LRESET#.
3-2	VTT_SEL	R/W	0	PECI (Vtt) voltage select. 00: Vtt is 1.23V 01: Vtt is 1.13V 10: Vtt is 1.00V 11: Vtt is 1.00V
1	DIG_T1_EN	R/W	0	0: Disable the digital interface of T1 (PECI/TSI). 1: Enable the digital interface of T1.
0	DIODE_T1_EN	R/W	1	0: Disable the D1+ measurement. 1: Enable the D1+ measurement.

PECI Address Register — Index 0Bh

Bit	Name	R/W	Default	Description
7-4	CPU_SEL	R/W	0	Select the Intel CPU socket number. 0000: no CPU presented. PECI host will use Ping() command to find CPU address. 0001: CPU is in socket 0, i.e. PECI address is 0x30. 0010: CPU is in socket 1, i.e. PECI address is 0x31. 0100: CPU is in socket 2, i.e. PECI address is 0x32. 1000: CPU is in socket 3, i.e. PECI address is 0x33. Otherwise are reserved.
3-1	Reserved	-	0	Reserved.
0	DOMAIN1_EN	R/W	0	If the CPU selected is dual core. Set this register 1 to read the temperature of domain1.

TCC TEMP Register — Index 0Ch

Bit	Name	R/W	Default	Description
7-0	TCC_TEMP/TSI_OFFSET	R/W	8'h55	TCC Activation Temperature/TSI Offset. When PECI is enabled, the absolute value of CPU temperature is calculated by the equation: CPU_TEMP = TCC_TEMP + PECI Reading. The range of this register is -128 ~ 127. When AMD TSI or Intel PCH SMBus is enabled, this byte is used as the offset to be added to the reading.

SST ADDR Register — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	SST_ADDR/ SMBUS_ADDR	R/W	8'h4C	When AMD TSI or Intel PCH SMBus is enabled, this byte is used as SMBUS_ADDR. SMBUS_ADDR [7:1] is the slave address sent by the embedded master to fetch the temperature. Otherwise, this byte is used as SST_ADDR if SST is enabled.

Voltage DIV Register — Index 0Eh

Bit	Name	R/W	Default	Description
7-6	VIN4_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN4. 01: voltage source is divided by 2 and connected to VIN4. 10: voltage source is divided by 4 and connected to VIN4. 11: voltage source is divided by 16 and connected to VIN4.
5-4	VIN3_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN3. 01: voltage source is divided by 2 and connected to VIN3. 10: voltage source is divided by 4 and connected to VIN3. 11: voltage source is divided by 16 and connected to VIN3.
3-2	VIN2_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN2. 01: voltage source is divided by 2 and connected to VIN2. 10: voltage source is divided by 4 and connected to VIN2. 11: voltage source is divided by 16 and connected to VIN2.
1-0	VIN1_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN1. 01: voltage source is divided by 2 and connected to VIN1. 10: voltage source is divided by 4 and connected to VIN1. 11: voltage source is divided by 16 and connected to VIN1. Above is available only if SST is enabled. Otherwise, bit 7-1 will be used as I2C_ADDR if Intel PCH SMBus is enabled.

PECI Config. and Voltage Register — Index 0Fh

Bit	Name	R/W	Default	Description
7-4	Reserved			Reserved.
3-2	VIN6_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN6. 01: voltage source is divided by 2 and connected to VIN6. 10: voltage source is divided by 4 and connected to VIN6. 11: voltage source is divided by 16 and connected to VIN6.

1-0	VIN5_DIV	R/W	0	The value indicates the divisor of the voltage source. 00: voltage source is directly connected to VIN5. 01: voltage source is divided by 2 and connected to VIN5. 10: voltage source is divided by 4 and connected to VIN5. 11: voltage source is divided by 16 and connected to VIN5. VIN6_DIV[0] and VIN5_DIV are used as TSI_TEMP_SEL[2:0] if Intel PCH SMBus is enabled. TSI_TEMP_SEL is used to select the temperature source for fan control.

TSI_TEMP_SEL	Temperature Source
000	Maximum of MCH or CPU
001	PCH
010	CPU
011	MCH
100	DIMM0
101	DIMM1
110	DIMM2
111	DIMM3

7.3.1 Voltage Setting

Voltage PME# Enable Register — Index 10h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
6	V6_VP_EN	R/W	0	Set this bit 1 to enable V6 voltage-protection event.
5	V5_VP_EN	R/W	0	Set this bit 1 to enable V5 voltage-protection event.
4-2	Reserved	--	0	Reserved
1	EN_V1_PME	R/W	0	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for VIN1.
0	3VCC_VP_EN	R/W	0	Set this bit 1 to enable 3VCC voltage protection event.

Voltage1 Interrupt Status Register — Index 11h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	V1_ EXC _STS	R/W	0	This bit is set when the VIN1 is over the high limit. Write 1 to clear this bit, write 0 will be ignored.
0	VP_STS	WC	0	This bit is voltage-protection status. Once one of the monitored voltages (3VCC, VIN5, VIN6) over its related over-voltage limits or under its related under-voltage limits, if the related voltage-protection shut down enable bit is set, this bit will be set to 1. Write 1 to this bit will clear it to 0. (This bit is powered by VBAT)

Voltage1 Exceeds Real Time Status Register 1 — Index 12h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	V1_EXC	RO	0	A one indicates VIN1 exceeds the high or low limit. A zero indicates VIN1 is in the safe region.
0	Reserved	--	0	Reserved

Voltage1 BEEP Enable Register — Index 13h

Bit	Name	R/W	Default	Description
7-2	Reserved	--	0	Reserved
1	EN_V1_BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP output of VIN1.
0	Reserved	--	0	Reserved

Voltage-Protection Enable Register — Index 14h

Bit	Name	R/W	Default	Description
7	Reserved	--	0	Reserved
6	V6_VP_EN	R	0	Set this bit 1 to enable V6 voltage-protection event.
5	V5_VP_EN	R	0	Set this bit 1 to enable V5 voltage-protection event.
4-1	Reserved	--	0	Reserved
0	3VCC_VP_EN	R	0	Set this bit 1 to enable 3VCC voltage-protection event.

Voltage Protection Event Status Register — Index 15h

Bit	Name	R/W	Default	Description
7-1	Reserved	--	0	Reserved
0	V_EXC_VP	R/WC	0	This bit is voltage-protection status. Once one of the monitored voltages (3VCC, VIN5, VIN6) over its related over-voltage limits or under its related under-voltage limits, if the related voltage-protection shut down enable bit is set, this bit will be set to 1. Write 1 to this bit will clear it to 0. (This bit is powered by VBAT)

Voltage-Protection Configuration Register (Powered by VBAT) — Index 16h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-2	PU_TIME	R/W	01	PSON# de-active time select in alarm mode of voltage protection. 00: PSON# tri-state 0.5 sec and then inverted of S3# when over voltage or under voltage occurs. 01: PSON# tri-state 1 sec and then inverted of S3# when over voltage or under voltage occurs. 10: PSON# tri-state 2 sec and then inverted of S3# when over voltage or under voltage occurs. 11: PSON# tri-state 4 sec and then inverted of S3# when over voltage or under voltage occurs.

1-0	VP_EN_DELAY	R/W	10	VP_EN_DELAY could set the delay time to start voltage protecting after VDD power is ok when OVP_MODE is 1. (OVP_MODE is strapped by SOUT2 pin) 00: bypass 01: 50ms 10: 100ms 11: 200ms

Voltage Protection Power Good Select Register – Index 3Fh

Bit	Name	R/W	Default	Description
7-1	Reserved	--	0	Reserved
0	OVP_RST_SEL	R/W	0	0: OVP/UVP power good signal is VDD3VOK (VCC3V > 2.8V) 1: OVP/UVP power good signal is PWROK. OVP/UVP function wont' start detecting until power good is ready.

Voltage reading and limit— Index 20h- 3Fh

Address	Attribute	Default Value	Description
20h	RO	--	3VCC reading. The unit of reading is 8mV.
21h	RO	--	VIN1 (Vcore) reading. The unit of reading is 8mV.
22h	RO	--	VIN2 reading. The unit of reading is 8mV.
23h	RO	--	VIN3 reading. The unit of reading is 8mV.
24h	RO	--	VIN4 reading. The unit of reading is 8mV.
25h	RO	--	VIN5 reading. The unit of reading is 8mV.
26h	RO	--	VIN6 reading. The unit of reading is 8mV.
27h	RO	--	I_VSB3V reading. The unit of reading is 8mV.
28h	RO	--	VBAT reading. The unit of reading is 8mV.
29~2Ch	RO	FF	Reserved
2Dh	RO	--	This byte indicates current fan1 duty.
2Eh	RO	--	This byte indicates current fan2 duty.
2Fh	RO	--	This byte indicates current fan3 duty.
30h	R/W	7A	3VCC under-voltage limit (V0_UVV_LIMIT). The unit is 9mv (This byte is powered by VBAT)
31h	R/W	D7	3VCC over-voltage protection limit. The unit is 9 mV
32h	R/W	FF	V1 High Limit setting register. The unit is 8mV.
33~35h	RO	FF	Reserved.
36h	R/W	C9	V5 over-voltage protection limit. The unit is 9 mV
37h	R/W	C8	V6 over-voltage protection limit. The unit is 9 mV
38h	R/W	75	VIN5 under-voltage limit (V5_UVV_LIMIT). The unit is 9mv (This byte is powered by VBAT)
39h	R/W	85	VIN6 under-voltage limit (V6_UVV_LIMIT). The unit is 9mv (This byte is powered by VBAT)
38-3Eh	RO	FF	Reserved.
3Fh	R/W	0	Set bit 0 to "1" to select OVP start monitor after PWROK ready.

7.3.2 PECI 3.0 Command and Register

PECI Configuration Register — Index 40h

Bit	Name	R/W	Default	Description
7	RDIAMSR_CMD_EN	R/W	0	When PECI temperature monitoring is enabled, set this bit 1 will generate a RdIAMSR () command before a GetTemp () command.
6	C3_UPDATE_EN	R/W	0	If RDIAMSR_CMD_EN is not set to 1, the temperature data is not allowed to be updated when the completion code of RdIAMSR () is 0x82.
5-4	Reserved	R	-	Reserved
3	C3_PTEMP_EN	R/W	0	Set this bit 1 to enable updateing positive value of temperature if the completion code of RdIAMSR () is 0x82.
2	C0_PTEMP_EN	R/W	0	Set this bit 1 to enable updating positive value of temperature if the completion code of RdIAMSR () is not 0x82 and the bit 8 of completion code is not 1 either.
1	C3_ALL0_EN	R/W	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR () is 0x82.
0	C0_ALL0_EN	R/W	0	Set this bit 1 to enable updating temperature value 0x0000 if the completion code of RdIAMSR () is not 0x82 and the bit 8 of completion code is not 1 either.

PECI Master Control Register — Index 41h

Bit	Name	R/W	Default	Description
7	PECI_CMD_START	W	-	Write 1 to this bit to start a PECI command when using as a PECI master. (PECI_PENDING must be set to 1)
6-5	Reserved	R	-	Reserved
4	PECI_PENDING	R/W	0	Set this bit 1 to stop monitoring PECI temperature.
3	Reserved	R	-	Reserved
2-0	PECI_CMD	R/W	3'h0	PECI command to be used by PECI master. 000: PING() 001: GetDIB() 010: GetTemp() 011: RdIAMSR() 100: RdPkgConfig() 101: WrPkgConfig() others: Reserved

PECI Master Status Register — Index 42h

Bit	Name	R/W	Default	Description
7-3	Reserved	R	-	Reserved
2	ABORT_FCS	R/WC	-	This bit is the Abort FCS status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
1	PECI_FCS_ERR	R/WC	-	This bit is the FCS error status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.
0	PECI_FINISH	R/WC	-	This bit is the Command Finish status of PECI master commands. Write this bit 1 or read this byte will clear this bit to 0.

PECI Master DATA0 Register — Index 43h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA0	R/W	0	For RdIAMSR (), RdPkgConfig () and WrPkgConfig () command, this byte represents "Host ID [7:1] & Retry [0]". Please refer to PECI interface specification for more detail.

PECI Master DATA1 Register — Index 44h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA1	R/W	0	For RdIAMSR (), this byte represents "Processor ID". For RdPkgConfig () and WrPkgConfig (), this byte represents "Index". Please refer to PECI interface specification for more detail.

PECI Master DATA2 Register — Index 45h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA2	R/W	0	For RdIAMSR (), this byte is the least significant byte of "MSR Address". For RdPkgConfig () and WrPkgConfig (), this byte is the least significant byte of "Parameter". Please refer to PECI interface specification for more detail.

PECI Master DATA3 Register — Index 46h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA3	R/W	0	For RdIAMSR (), this byte is the most significant byte of "MSR Address". For RdPkgConfig () and WrPkgConfig (), this byte is the most significant byte of "Parameter". Please refer to PECI interface specification for more detail.

PECI Master DATA4 Register — Index 47h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA4	R/W	0	For GetDIB() , this byte represents "Device Info" For GetTemp (), this byte represents the least significant byte of temperature. For RdIAMSR () and RdPkgConfig () , this byte is "Completion Code". For WrPkgConfig (), this byte represents "DATA[7:0]"

PECI Master DATA5 Register — Index 48h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA5	R/W	0	For GetDIB () , this byte represents "Revision Number" For GetTemp (), this byte represents the most significant byte of temperature. For RdIAMSR () and RdPkgConfig () , this byte represents "DATA[7:0]" For WrPkgConfig (), this byte represents "DATA[15:8]"

PECI Master DATA6 Register — Index 49h

Bit	Name	R/W	Default	Description
7-0	PECI_DATA6	R/W	0	For RdIAMSR () and RdPkgConfig (), this byte represents "DATA[15:8]". For WrPkgConfig (), this byte represents "DATA [23:16]"

PECI Master DATA7 Register — Index 4Ah

Bit	Name	R/W	Default	Description
7-0	PECI_DATA7	R/W	0	For RdIAMSR () and RdPkgConfig (), this byte represents "DATA[23:16]". For WrPkgConfig (), this byte represents "DATA[31:24]"

PECI Master DATA8 Register — Index 4Bh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA8	R/W	0	For RdIAMSR () and RdPkgConfig () , this byte represents "DATA[31:24]". For WrPkgConfig(), this byte represents "AW FCS"

PECI Master DATA9 Register — Index 4Ch

Bit	Name	R/W	Default	Description
7-0	PECI_DATA9	R/W	0	For RdIAMSR (), this byte represents "DATA [39:32]". For WrPkgConfig(), this byte represents "Completion Code"

PECI Master DATA10 Register — Index 4Dh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA10	R/W	0	For RdIAMSR (), this byte represents "DATA [47:40]".

PECI Master DATA11 Register — Index 4Eh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA11	R/W	0	For RdIAMSR (), this byte represents "DATA [55:48]".

PECI Master DATA12 Register — Index 4Fh

Bit	Name	R/W	Default	Description
7-0	PECI_DATA12	R/W	0	For RdIAMSR (), this byte represents "DATA [63:56]".

7.3.3 Temperature Setting

Temperature PME# Enable Register — Index 60h

Bit	Name	R/W	Default	Description
7	EN_ T3_OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds OVT setting.
5	EN_ T1_ OVT_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds OVT setting.
4	Reserved	R/W	0	Reserved
3	EN_ T3_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_PME	R/W	0	If set this bit to 1, PME# signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

Temperature Interrupt Status Register — Index 61h

Bit	Name	R/W	Default	Description
7	T3_OVT_STS	R/W	0	A one indicates TEMP3 temperature sensor has exceeded OVT limit or below the "OVT limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
6	T2_OVT _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded OVT limit or below the "OVT limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
5	T1_OVT _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded OVT limit or below the "OVT limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.
4	Reserved	R/W	0	Reserved
3	T3_EXC _STS	R/W	0	A one indicates TEMP3 temperature sensor has exceeded high limit or below the "high limit –hysteresis". Write 1 to clear this bit, write 0 will be ignored.

2	T2_EXC _STS	R/W	0	A one indicates TEMP2 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
1	T1_EXC _STS	R/W	0	A one indicates TEMP1 temperature sensor has exceeded high limit or below the “high limit –hysteresis” limit. Write 1 to clear this bit, write 0 will be ignored.
0	Reserved	R/W	0	Reserved

Temperature Real Time Status Register — Index 62h

Bit	Name	R/W	Default	Description
7	T3_OVT	R/W	0	Set when the TEMP3 exceeds the OVT limit. Clear when the TEMP3 is below the “OVT limit –hysteresis” temperature.
6	T2_OVT	R/W	0	Set when the TEMP2 exceeds the OVT limit. Clear when the TEMP2 is below the “OVT limit –hysteresis” temperature.
5	T1_OVT	R/W	0	Set when the TEMP1 exceeds the OVT limit. Clear when the TEMP1 is below the “OVT limit –hysteresis” temperature.
4	Reserved	R/W	0	Reserved
3	T3_EXC	R/W	0	Set when the TEMP3 exceeds the high limit. Clear when the TEMP3 is below the “high limit –hysteresis” temperature.
2	T2_EXC	R/W	0	Set when the TEMP2 exceeds the high limit. Clear when the TEMP2 is below the “high limit –hysteresis” temperature.
1	T1_EXC	R/W	0	Set when the TEMP1 exceeds the high limit. Clear when the TEMP1 is below the “high limit –hysteresis” temperature.
0	Reserved	R/W	0	Reserved

Temperature BEEP Enable Register — Index 63h

Bit	Name	R/W	Default	Description
7	EN_ T3_OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds OVT limit setting.
6	EN_ T2_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds OVT limit setting.
5	EN_ T1_ OVT_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds OVT limit setting.
4	Reserved	R/W	0	Reserved
3	EN_ T3_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP3 exceeds high limit setting.
2	EN_ T2_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP2 exceeds high limit setting.
1	EN_ T1_EXC_BEEP	R/W	0	If set this bit to 1, BEEP signal will be issued when TEMP1 exceeds high limit setting.
0	Reserved	R/W	0	Reserved

OVT Output Enable Register 1 — Index 66h

Bit	Name	R/W	Default	Description
7	EN_T3_ALERT	R	0	Enable temperature 3 alert event (asserted when temperature over high limit)
6	EN_T2_ALERT	R	0	Enable temperature 2 alert event (asserted when temperature over high limit)
5	EN_T1_ALERT	R	0	Enable temperature 1 alert event (asserted when temperature over high limit)

4	Reserved	R	0	Reserved.
3	EN_T3_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature3.
2	EN_T2_OVT	R/W	0	Enable over temperature (OVT) mechanism of temperature2.
1	EN_T1_OVT	R/W	1	Enable over temperature (OVT) mechanism of temperature1.
0	Reserved	R	0h	Reserved.

Temperature Sensor Type Register — Index 6Bh

Bit	Name	R/W	Default	Description
7-4	Reserved	RO	0	Reserved
3	T3_MODE	R/W	1	0: TEMP3 is connected to a thermistor 1: TEMP3 is connected to a BJT (default).
2	T2_MODE	R/W	1	0: TEMP2 is connected to a thermistor. 1: TEMP2 is connected to a BJT (default).
1	T1_MODE	R/W	1	0: TEMP1 is connected to a thermistor 1: TEMP1 is connected to a BJT (default).
0	Reserved	R	0h	--

TEMP1 Limit Hystersis Select Register -- Index 6Ch

Bit	Name	R/W	Default	Description
7-4	TEMP1_HYS	R/W	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	Reserved	R	0h	--

TEMP2 and TEMP3 Limit Hystersis Select Register -- Index 6Dh

Bit	Name	R/W	Default	Description
7-4	TEMP3_HYS	R/W	2h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).
3-0	TEMP2_HYS	R/W	4h	Limit hysteresis. (0~15°C) Temperature and below the (boundary – hysteresis).

DIODE OPEN Status Register -- Index 6Fh

Bit	Name	R/W	Default	Description
7-4	Reserved	RO	0h	Reserved
3	T3_DIODE_OPEN	RO	0h	External diode 3 is open or short
2	T2_DIODE_OPEN	RO	0h	External diode 2 is open or short
1	T1_DIODE_OPEN	RO	0h	This register indicates the abnormality of temperature 1 measurement. When TSI interface is enabled, it indicates the error of not receiving NACK bit or a timeout occurred. When PECI interface is enabled, it indicates an error code (0x0080 or 0x0081) is received from PECI slave. When external diode is used, it indicates the BJT is open or short.
0	Reserved	R	0h	--

Temperature — Index 70h- 8Fh

Address	Attribute	Default Value	Description
70h	Reserved	FFh	Reserved
71h	Reserved	FFh	Reserved
72h	RO	--	Temperature 1 reading. The unit of reading is 1°C.At the moment of reading this register.

73h	RO	--	Reserved
74h	RO	--	Temperature 2 reading. The unit of reading is 1°C.At the moment of reading this register.
75h	RO	--	Reserved
76h	RO	--	Temperature 3 reading. The unit of reading is 1°C.At the moment of reading this register.
77h	RO	--	Reserved
78h	RO	--	PECI temperature reading
79h	RO	--	AMD TSI or Intel IBX temperature reading
7Ah	RO	--	The raw data of T3 read from digital interface. (Only available if Intel IBX interface is enabled)
7Bh	RO	--	The raw data of T2 read from digital interface. (Only available if Intel IBX interface is enabled)
7Ch	RO	--	The data of T1 read from digital interface.
7Dh	RO	--	The raw data of T1 read from D1+.
7Eh	R/W	00h-	T1 Slope Adjust.
7Fh	R/W	00h	T1 Source Select.
80h	Reserved	FFh	Reserved
81h	Reserved	FFh	Reserved
82h	R/W	64h	Temperature sensor 1 OVT limit. The unit is 1°C.
83h	R/W	55h	Temperature sensor 1 high limit. The unit is 1°C.
84h	R/W	64h	Temperature sensor 2 OVT limit. The unit is 1°C.
85h	R/W	55h	Temperature sensor 2 high limit. The unit is 1°C.
86h	R/W	55h	Temperature sensor 3 OVT limit. The unit is 1°C.
87h	R/W	46h	Temperature sensor 3 high limit. The unit is 1°C.
88-8Bh	RO	--	Reserved
8C~8Dh	RO	FFH	Reserved

T1 Slope Adjust Register -- Index 7Eh

Bit	Name	R/W	Default	Description
7	DIG_T1_ADD	R/W	0h	This bit is the sign bit for digital T1 reading slope adjustment. See DIG_T1_SCALE below for detail.

<table>
<tr><td>6-4</td><td>DIG_T1_SCALE</td><td>R/W</td><td>0h</td><td>Accompanying with DIG_T1_ADD, the slope adjustment of digital T1 is listed.
<table>
<tr><th>DIG_T1_ADD</th><th>DIG_T1_SCALE</th><th>Slope</th></tr>
<tr><td>0</td><td>000</td><td>No adjustment</td></tr>
<tr><td>0</td><td>001</td><td>1/2</td></tr>
<tr><td>0</td><td>010</td><td>3/4</td></tr>
<tr><td>0</td><td>011</td><td>7/8</td></tr>
<tr><td>0</td><td>100</td><td>15/16</td></tr>
<tr><td>0</td><td>101</td><td>31/32</td></tr>
<tr><td>0</td><td>110</td><td>63/64</td></tr>
<tr><td>0</td><td>111</td><td>127/128</td></tr>
<tr><td>1</td><td>000</td><td>No adjustment</td></tr>
<tr><td>1</td><td>001</td><td>3/2</td></tr>
<tr><td>1</td><td>010</td><td>5/4</td></tr>
<tr><td>1</td><td>011</td><td>9/8</td></tr>
<tr><td>1</td><td>100</td><td>17/16</td></tr>
<tr><td>1</td><td>101</td><td>33/32</td></tr>
<tr><td>1</td><td>110</td><td>65/64</td></tr>
<tr><td>1</td><td>111</td><td>129/128</td></tr>
</table></td></tr>
<tr><td>3</td><td>DIODE_T1_ADD</td><td>R/W</td><td>0h</td><td>The function of this bit is the same as DIG_T1_ADD expect that it is for D1+ reading.</td></tr>
<tr><td>2-0</td><td>DIODE_T1_SCALE</td><td>R/W</td><td>0h</td><td>The function of this bit is the same as DIG_T1_SCALE expect that it is for D1+ reading.</td></tr>
</table>

Temperature Filter Select Register -- Index 7Fh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7-2</td><td>Reserved</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>1-0</td><td>T1_SRC_SEL_REG</td><td>R/W</td><td>00</td><td>The bits are used when DIODE_T1_EN and DIG_T1_EN are both enabled. The real select bits T1_SCR_SEL are fixed to 2’b01 if DIODE_T1_EN is “0” and 2’b00 if DIG_T1_EN is “0”. The T1 source is listed.
<table>
<tr><th>T1_SRC_SEL</th><th>T1 source</th></tr>
<tr><td>00</td><td>From D1+ only</td></tr>
<tr><td>01</td><td>From Digital reading (PECI/TSI)</td></tr>
<tr><td>10</td><td>Average</td></tr>
<tr><td>11</td><td>Maximum</td></tr>
</table></td></tr>
</table>

Temperature Filter Select Register -- Index 8Eh

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7-6</td><td>IIR-QUEUR3</td><td>R/W</td><td>2’b10</td><td>The queue time for third filter to quickly update values.
00: 8 times.
01: 12 times.
10: 16 times. (default)
11: 24 times.</td></tr>
<tr><td>5-4</td><td>IIR-QUEUR2</td><td>R/W</td><td>2’b10</td><td>The queue time for second filter to quickly update values.
00: 8 times.
01: 12 times.
10: 16 times. (default)
11: 24 times.</td></tr>
<tr><td>3-2</td><td>IIR-QUEUR1</td><td>R/W</td><td>2’b10</td><td>The queue time for first filter to quickly update values.
00: 8 timers.
01: 12 times.
10: 16 times. (default)
11: 24 times.</td></tr>
<tr><td>0</td><td>Reserved</td><td>R</td><td>-</td><td>--</td></tr>
</table>

7.3.4 Fan Control Setting

FAN PME# Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7-3	Reserved	RO	0h	Reserved
2	EN_FAN3_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan3.
1	EN_FAN2_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan2.
0	EN_FAN1_PME	R/W	0h	A one enables the corresponding interrupt status bit for PME# interrupt. Set this bit 1 to enable PME# function for Fan1.

FAN Interrupt Status Register — Index 91h

Bit	Name	R/W	Default	Description
7-3	Reserved	RO	0	Reserved
2	FAN3_STS	R/W	--	This bit is set when the fan3 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
1	FAN2_STS	R/W	--	This bit is set when the fan2 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.
0	FAN1_STS	R/W	--	This bit is set when the fan1 count exceeds the count limit. Write 1 to clear this bit, write 0 will be ignored.

FAN Real Time Status Register — Index 92h

Bit	Name	R/W	Default	Description
7-3	Reserved	--	0	Reserved
2	FAN3_EXC	RO	--	This bit set to high mean that fan3 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.
1	FAN2_EXC	RO	--	This bit set to high mean that fan2 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.
0	FAN1_EXC	RO	--	This bit set to high mean that fan1 count can't meet expect count over than SMI time (CR9F) or when duty not zero but fan stop over then 3 sec.

FAN BEEP# Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	FULL_WITH_T3_EN	R/W	0	Set one will enable FAN to force full speed when T3 over high limit.
6	FULL_WITH_T2_EN	R/W	0	Set one will enable FAN to force full speed when T2 over high limit.
5	FULL_WITH_T1_EN	R/W	0	Set one will enable FAN to force full speed when T1 over high limit.
4	Reserved	R/W	0	Reserved.
3	Reserved	-	-	Reserved.
2	EN_FAN3_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.
1	EN_FAN2_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.
0	EN_FAN1_ BEEP	R/W	0	A one enables the corresponding interrupt status bit for BEEP.

Fan Type Select Register -- Index 94h (FAN_PROG_SEL = 0)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.

5-4	FAN3_TYPE	R/W	2'b 0S	00: Output PWM mode (pushpull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by RTS2# 0: RTS2# is pull up by internal 47K resistor. 1: RTS2# is pull down by external resistor.
3-2	FAN2_TYPE	R/W	2'b 0S	00: Output PWM mode (pushpull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by RTS2# 0: RTS2# is pull up by internal 47K resistor. 1: RTS2# is pull down by external resistor.
1-0	FAN1_TYPE	R/W	2'b 0S	00: Output PWM mode (push pull) to control fans. 01: Use linear fan application circuit to control fan speed by fan's power terminal. 10: Output PWM mode (open drain) to control Intel 4-wire fans. 11: Reserved. Bit 0 is power on trap by RTS2# 0: RTS2# is pull up by internal 47K resistor. 1: RTS2# is pull down by external resistor.

S: Register default values are decided by trapping.

Fan1 Base Temperature Register – Index 94h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7-0	FAN1_BASE_TEMP	R/W	8'h0	This register is used to set the base temperature for FAN1 temperature adjustment. The FAN1 temperature is calculated according to the equation: Tfan1 = Tnow + (Ta – Tb)*Ct Where Tnow is selected by FAN1_TEMP_SEL_DIG and FAN1_TEMP_SEL. Tb is this register, Ta is selected by TFAN1_ADJ_SEL and Ct is selected by TFAN1_ADJ_UP_RATE/TFAN1_ADJ_DN_RATE. To access this register, FAN_PROG_SEL (CR9F[7]) must set to "1".

Fan1 Temperature Adjustment Rate Register – Index 95h (FAN_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6-4	TFAN1_ADJ_UP_RATE	R/W	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is higher than Tb. 3'h1: 1 (Ct = 1) 3'h2: 1/2 (Ct= 1/2) 3'h3: 1/4 (Ct = 1/4) 3'h4: 1/8 (Ct = 1/8) otherwise: 0
2	Reserved	-	-	Reserved.

2-0	TFAN1_ADJ_DN_RATE	R/W	3'h0	This selects the weighting of the difference between Ta and Tb if Ta is lower than Tb. 3'h1: 1 (Ct = 1) 3'h2: 1/2 (Ct= 1/2) 3'h3: 1/4 (Ct = 1/4) 3'h4: 1/8 (Ct = 1/8) otherwise: 0 To access this byte, FAN_PROG_SEL must set to "1".

Fan mode Select Register -- Index 96h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that defines in 0xC6-0xCE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defines in 0xC6-0xCE. 10: Manual mode fan control, user can write expected **RPM** count to 0xC2-0xC3, and F71889A will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xC3, and F71889A will output this value duty or voltage to control fan speed.
3-2	FAN2_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that defines in 0xB6-0xBE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** (voltage) that defines in 0xB6-0xBE. 10: Manual mode fan control, user can write expected **RPM** count to 0xB2-0xB3, and F71889A will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xB3, and F71889A will output this value duty or voltage to control fan speed.
1-0	FAN1_MODE	R/W	1h	00: Auto fan speed control, fan speed will follow different temperature by different **RPM** that defines in 0xA6-0xAE. 01: Auto fan speed control, fan speed will follow different temperature by different **duty cycle** that defines in 0xA6-0xAE. 10: Manual mode fan control, user can write expected **RPM** count to 0xA2-0xA3, and F71889A will auto control duty cycle (PWM fan type) or voltage (linear fan type) to control fan speed. 11: Manual mode fan control, user can write expected **duty cycle** (PWM fan type) or voltage (linear fan type) to 0xA3, and F71889A will output this value duty or voltage to control fan speed.

Auto Fan1 and Fan2 Boundary Hystersis Select Register -- Index 98h

Bit	Name	R/W	Default	Description
7-4	FAN2_HYS	R/W	4h	0000: Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).
3-0	FAN1_HYS	R/W	4h	0000: Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Auto Fan3 Boundary Hystersis Select Register -- Index 99h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_HYS	R/W	2h	0000: Boundary hysteresis. (0~15°C) Segment will change when the temperature over the boundary temperature and below the (boundary – hysteresis).

Fan3 Control Register — Index 9Ah

Bit	Name	R/W	Default	Description
7-6	FAN3_FREQ_SEL	-	-	Select the PWM3 frequency 00: 23.5 KHz 01: 11.75 KHz 10: 5.875 KHz 11: 220 Hz
5-4	Reserved	R/W	0	Reserved (Keep the value of these two bits “0”)
3-1	Reserved	R/W	0	Reserved.
0	FAN3_EXT_EN	R/W	0	Set this bit 1 to enable the function that FAN3 output duty could be adjusted by GPIO53/GPIO54.

Auto Fan Up Speed update Rate Select Register -- Index 9Bh (FAN_RATE_PROG_SEL = 0)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_UP_RATE	R/W	1h	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
3-2	FAN2_UP_RATE	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_UP_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

Auto Fan Down Speed update Rate Select Register -- Index 9Bh (FAN_RATE_PROG_SEL = 1)

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5-4	FAN3_DOWN_RATE	R/W	1h	Fan3 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

3-2	FAN2_DOWN_RATE	R/W	1h	Fan2 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz
1-0	FAN1_DOWN_RATE	R/W	1h	Fan1 duty update rate: 00: 2Hz 01: 5Hz (default) 10: 10Hz 11: 20Hz

FAN1 and FAN2 START UP DUTY-CYCLE/VOLTAGE — Index 9Ch

Bit	Name	R/W	Default	Description
7-4	FAN2_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL2 will increase duty-cycle from 0 to this (value x 8) directly. And if fan speed is down, the FAN_CTRL 2 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).
3-0	FAN1_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL1 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL1 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN3 START UP DUTY-CYCLE/VOLTAGE — Index 9Dh

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	FAN3_STOP_DUTY	R/W	5h	When fan start, the FAN_CTRL 3 will increase duty-cycle from 0 to this (value x 8 directly. And if fan speed is down, the FAN_CTRL 3 will decrease duty-cycle to 0 when the PWM duty cycle is less than this (value x 4).

FAN PROGRAMMABLE DUTY-CYCLE/VOLTAGE LOADED AFTER POWER-ON — Index 9Eh

Bit	Name	R/W	Default	Description
7-0	PROG_DUTY_VAL	R/W	99h	This byte will be immediately loaded as Fan duty value after VDD is powered on if it has been programmed before shut down.

Fan Fault Time Register -- Index 9Fh

Bit	Name	R/W	Default	Description
7	FAN_RATE_PROG_SEL	R/W	0	0: Index 9Bh is the fan up speed update rate select register. 1: Index 9Bh is the fan down speed update rate select register.
6	Reserved	--	--	Reservd
5	FAN_NEG_TEMP_EN	R/W	0	0: Disable the negative temperature compare of fan expected value. 1: Enable the negative temperature compare of fan expected value.
4	FULL_DUTY_SEL	R/W	--	0: the full duty is 100%. (pull down by external resistor) 1: the full duty is 60% (default, pull up by internal 47K resistor). This register is power on trap by DTR1#.
3-0	F_FAULT_TIME	R/W	Ah	This register determines the time of fan fault. The condition to cause fan fault event is: When PWM_Duty reaches FFh, if the fan speed count can't reach the fan expected count in time. The unit of this register is 1 second. The default value is 11 seconds. (Set to 0, means 1 second; Set to 1, means 2 second; Set to 2, means 3 second…) Another condition to cause fan fault event is fan stop and the PWM duty is greater than the minimum duty programmed by the register index 9C-9Dh.

Fan1 Index A0h- AFh

Address	Attribute	Default Value	Description
A0h	RO	8'h0f	FAN1 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A1h	RO	8'hff	FAN1 count reading (LSB).
A2h	R/W	8'h00	**RPM mode (CR96 bit0=0):** FAN1 expected speed count value (MSB), in auto fan mode (CR96 bit1➔0) this register is auto updated by hardware. **Duty mode (CR96 bit0=1):** This byte is reserved byte.
A3h	R/W	8'h01	**RPM mode (CR96 bit0=0):**FAN1 expected speed count value (LSB) or expected PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode (CR96 bit0=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit1➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
A4h	R/W	8'h03	FAN1 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
A5h	R/W	8'hff	FAN1 full speed count reading (LSB).

VT1 BOUNDARY 1 TEMPERATURE – Index A6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP1	R/W	3Ch (60°C)	The 1st BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expect value will load from segment 1 register (index AAh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 2 register (index ABh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT1 BOUNDARY 2 TEMPERATURE – Index A7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP1	R/W	32 (50°C)	The 2nd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 2 register (index ABh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 3 register (index ACh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT1 BOUNDARY 3 TEMPERATURE – Index A8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP1	R/W	28h (40°C)	The 3rd BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 3 register (index ACh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 4 register (index ADh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT1 BOUNDARY 4 TEMPERATURE – Index A9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP1	R/W	1Eh (30°C)	The 4th BOUNDARY temperature for VT1 in temperature mode. When VT1 temperature is exceed this boundary, FAN1 expected value will load from segment 4 register (index ADh). When VT1 temperature is below this boundary – hysteresis, FAN1 expected value will load from segment 5 register (index AEh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

FAN1 SEGMENT 1 SPEED COUNT – Index AAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED1	R/W	FFh (100%)	The meaning of this register is depending on the FAN1_MODE (CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%:full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 2 SPEED COUNT – Index ABh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED1	R/W	D9h (85%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 3 SPEED COUNT – Index ACh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED1	R/W	B2h (70%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 4 SPEED COUNT – Index ADh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED1	R/W	99h (60%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 SEGMENT 5 SPEED COUNT – Index AEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED1	R/W	80h (50%)	The meaning of this register is depending on the FAN1_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN1 Temperature Mapping Select – Index AFh

Bit	Name	R/W	Default	Description
7	FAN1_TEMP_SEL_DIG	R/W	0	This bit companying with FAN1_TEMP_SEL select the temperature source for controlling FAN1.
6	Reserved	--	0	Reserved
5	FAN1_UP_T_EN	R/W	0	Set 1 to force FAN1 to full speed if any temperature over its high limit.
4	FAN1_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table.
3	FAN1_JUMP_HIGH_EN	R/W	0	This register controls the FAN1 duty movement when temperature over highest boundary. 0: The FAN1 duty will increases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC1SPEED1 register. This bit only activates in duty mode.
2	FAN1_JUMP_LOW_EN	R/W	0	This register controls the FAN1 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN1 duty will decreases with the slope selected by FAN1_RATE_SEL register. 1: The FAN1 duty will directly jumps to the value of SEC2SPEED1 register. This bit only activates in duty mode.
1-0	FAN1_TEMP_SEL	R/W	1	This registers companying with FAN1_TEMP_SEL_DIG select the temperature source for controlling FAN1. The following value is comprised by {FAN1_TEMP_SEL_DIG, FAN1_TEMP_SEL} 000: fan1 follows PECI temperature (CR78h) 001: fan1 follows temperature 1 (CR72h). 010: fan1 follows temperature 2 (CR74h). 011: fan1 follows temperature 3 (CR76h). 100: fan1 follows AMD TSI or Intel IBX temperature (CR79h) 101: fan1 follows digital temperature 1 (CR7Ch). 110: fan1 follows digital temperature 2 (CR7Bh). 111: fan1 follows digital temperature 3 (CR7Ah). Otherwise: reserved.

Fan2 Index B0h- BFh

Address	Attribute	Default Value	Description
B0h	RO	8'h0f	FAN2 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B1h	RO	8'hff	FAN2 count reading (LSB).
B2h	R/W	8'h00	**RPM mode (CR96 bit2=0):** FAN2 expect speed count value (MSB), in auto fan mode (CR96 bit3➔0) this register is auto updated by hardware. **Duty mode (CR96 bit2=1):** This byte is reserved byte.
B3h	R/W	8'h01	**RPM mode (CR96 bit2=0):** FAN2 expect speed count value (LSB) or expect PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode (CR96 bit2=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit3➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255➔ 100%
B4h	R/W	8'h03	FAN2 full speed count reading (MSB). At the moment of reading this register, the

			LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
B5h	R/W	8'hff	FAN2 full speed count reading (LSB).

VT2 BOUNDARY 1 TEMPERATURE – Index B6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP2	R/W	3Ch (60°C)	The 1st BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 1 register (index BAh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 2 register (index BBh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT2 BOUNDARY 2 TEMPERATURE – Index B7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP2	R/W	32 (50°C)	The 2nd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 2 register (index BBh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 3 register (index BCh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT2 BOUNDARY 3 TEMPERATURE – Index B8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP2	R/W	28h (40°C)	The 3rd BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 3 register (index BCh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 4 register (index BDh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT2 BOUNDARY 4 TEMPERATURE – Index B9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP2	R/W	1Eh (30°C)	The 4th BOUNDARY temperature for VT2 in temperature mode. When VT2 temperature is exceed this boundary, FAN2 expected value will load from segment 4 register (index BDh). When VT2 temperature is below this boundary – hysteresis, FAN2 expected value will load from segment 5 register (index BEh). This byte is a 2's complement value ranging from -128°C ~ 127°C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

FAN2 SEGMENT 1 SPEED COUNT – Index BAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED2	R/W	FFh (100%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expected fan speed % of the full speed in this temperature section. Ex: 100%: full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ((100-X)*32/X 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 2 SPEED COUNT – Index BBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED2	R/W	D9h (85%)	The meaning of this register is depending on the FAN2_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 3 SPEED COUNT – Index BCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED2	R/W	B2h (70%)	The meaning of this register is depending on the FAN2_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 4 SPEED COUNT – Index BDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED2	R/W	99h (60%)	The meaning of this register is depending on the FAN2_MODE(CR96) 2'b00: The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. 2'b01: The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 SEGMENT 5 SPEED COUNT – Index BEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED2	R/W	80h (50%)	The meaning of this register is depending on the FAN2_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN2 Temperature Mapping Select – Index BFh

Bit	Name	R/W	Default	Description
7	FAN2_TEMP_SEL_DIG	R/W	0	This bit companying with FAN2_TEMP_SEL select the temperature source for controlling FAN2.
6	Reserved	–	0	Reserved
5	FAN2_UP_T_EN	R/W	0	Set 1 to force FAN2 to full speed if any temperature over its high limit.
4	FAN2_INTERPOLATION_EN	R/W	0	Set 1 will enable the interpolation of the fan expect table.
3	FAN2_JUMP_HIGH_EN	R/W	0	This register controls the FAN2 duty movement when temperature over highest boundary. 0: The FAN2 duty will increases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC1SPEED2 register. This bit only activates in duty mode.
2	FAN2_JUMP_LOW_EN	R/W	0	This register controls the FAN2 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN2 duty will decreases with the slope selected by FAN2_RATE_SEL register. 1: The FAN2 duty will directly jumps to the value of SEC2SPEED2 register. This bit only activates in duty mode.

1-0	FAN2_TEMP_SEL	R/W	1	This registers companying with FAN2_TEMP_SEL_DIG select the temperature source for controlling FAN2. The following value is comprised by {FAN2_TEMP_SEL_DIG, FAN2_TEMP_SEL} 000: fan2 follows PECI temperature (CR78h) 001: fan2 follows temperature 1 (CR72h). 010: fan2 follows temperature 2 (CR74h). 011: fan2 follows temperature 3 (CR76h). 100: fan2 follows AMD TSI or Intel IBX temperature (CR79h) 101: fan2 follows digital temperature 1 (CR7Ch). 110: fan2 follows digital temperature 2 (CR7Bh). 111: fan2 follows digital temperature 3 (CR7Ah). Otherwise: reserved.

Fan3 Index C0h- CFh

Address	Attribute	Default Value	Description
C0h	RO	8'h0F	FAN3 count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C1h	RO	8'hff	FAN3 count reading (LSB).
C2h	R/W	8'h00	**RPM mode (CR96 bit4=0):** FAN3 expect speed count value (MSB), in auto fan mode (CR96 bit5➔0) this register is auto updated by hardware. **Duty mode (CR96 bit4=1):**This byte is reserved byte.
C3h	R/W	8'h01	**RPM mode (CR96 bit4=0):** FAN3 expected speed count value (LSB) or expected PWM duty, in auto fan mode this register is auto updated by hardware and read only. **Duty mode (CR96 bit4=1):** The Value programming in this byte is duty value. In auto fan mode (CR96 bit5➔0) this register is updated by hardware. Ex: 5➔ 5*100/255 % 255 ➔ 100%
C4h	R/W	8'h03	FAN3 full speed count reading (MSB). At the moment of reading this register, the LSB will be latched. This will prevent from data updating when reading. To read the fan count correctly, read MSB first and followed read the LSB.
C5h	R/W	8'hff	FAN3 full speed count reading (LSB).

VT3 BOUNDARY 1 TEMPERATURE – Index C6h

Bit	Name	R/W	Default	Description
7-0	BOUND1TMP3	R/W	3Ch ($60^{o}C$)	The 1st BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 1 register (index CAh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 2 register (index CBh). This byte is a 2's complement value ranging from -128 ^{o}C ~ 127 ^{o}C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT3 BOUNDARY 2 TEMPERATURE – Index C7

Bit	Name	R/W	Default	Description
7-0	BOUND2TMP3	R/W	32 (50°C)	The 2nd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 2 register (index CBh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 3 register (index CCh). This byte is a 2's complement value ranging from -128 °C ~ 127 °C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT3 BOUNDARY 3 TEMPERATURE – Index C8h

Bit	Name	R/W	Default	Description
7-0	BOUND3TMP3	R/W	28h (40°C)	The 3rd BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 3 register (index CCh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 4 register (index CDh). This byte is a 2's complement value ranging from -128 °C ~ 127 °C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

VT3 BOUNDARY 4 TEMPERATURE – Index C9

Bit	Name	R/W	Default	Description
7-0	BOUND4TMP3	R/W	1Eh (30°C)	The 4th BOUNDARY temperature for VT3 in temperature mode. When VT3 temperature is exceed this boundary, FAN3 expected value will load from segment 4 register (index CDh). When VT3 temperature is below this boundary – hysteresis, FAN3 expected value will load from segment 5 register (index CEh). This byte is a 2's complement value ranging from -128 °C ~ 127 °C. Bit 7 will always be "0" (always positive) if FAN_NEG_TEMP_EN is "0".

FAN3 SEGMENT 1 SPEED COUNT – Index CAh

Bit	Name	R/W	Default	Description
7-0	SEC1SPEED3	R/W	FFh (100%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. Ex: 100%: full speed: User must set this register to 0. 60% full speed: (100-60)*32/60, so user must program 21 to this reg. X% full speed: The value programming in this byte is ➔ (100-X)*32/X **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 2 SPEED COUNT – Index CBh

Bit	Name	R/W	Default	Description
7-0	SEC2SPEED3	R/W	D9h (85%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expected fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte means the expected PWM duty-cycle in this temperature section.

FAN3 SEGMENT 3 SPEED COUNT – Index CCh

Bit	Name	R/W	Default	Description
7-0	SEC3SPEED3	R/W	B2h (70%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 4 SPEED COUNT – Index CDh

Bit	Name	R/W	Default	Description
7-0	SEC4SPEED3	R/W	99h (60%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 SEGMENT 5 SPEED COUNT – Index CEh

Bit	Name	R/W	Default	Description
7-0	SEC5SPEED3	R/W	80h (50%)	The meaning of this register is depending on the FAN3_MODE(CR96) **2'b00:** The value that set in this byte is the relative expect fan speed % of the full speed in this temperature section. **2'b01:** The value that set in this byte is mean the expect PWM duty-cycle in this temperature section.

FAN3 Temperature Mapping Select – Index CFh

Bit	Name	R/W	Default	Description
7	FAN3_TEMP_SEL _DIG	R/W	0	This bit companying with FAN3_TEMP_SEL select the temperature source for controlling FAN3.
6	Reserved	--	0	Reserved
5	FAN3_UP_T_EN	R/W	0	Set 1 to force FAN3 to full speed if any temperature over its high limit.
4	FAN3_INTERPOLATION_ EN	R/W	0	Set 1 will enable the interpolation of the fan expect table.
3	FAN3_JUMP_HIGH_EN	R/W	0	This register controls the FAN3 duty movement when temperature over highest boundary. 0: The FAN3 duty will increases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC1SPEED3 register. This bit only activates in duty mode.
2	FAN3_JUMP_LOW_EN	R/W	0	This register controls the FAN3 duty movement when temperature under (highest boundary – hysteresis). 0: The FAN3 duty will decreases with the slope selected by FAN3_RATE_SEL register. 1: The FAN3 duty will directly jumps to the value of SEC2SPEED3 register. This bit only activates in duty mode.

1-0	FAN3_TEMP_SEL	R/W	1	This registers companying with FAN3_TEMP_SEL_DIG select the temperature source for controlling FAN3. The following value is comprised by {FAN3_TEMP_SEL_DIG, FAN3_TEMP_SEL} 000: fan3 follows PECI temperature (CR78h) 001: fan3 follows temperature 1 (CR72h). 010: fan3 follows temperature 2 (CR74h). 011: fan3 follows temperature 3 (CR76h). 100: fan3 follows AMD TSI or Intel IBX temperature (CR79h) 101: fan3 follows digital temperature 1 (CR7Ch). 110: fan3 follows digital temperature 2 (CR7Bh). 111: fan3 follows digital temperature 3 (CR7Ah). Otherwise: reserved.

TSI Temperature 0 – Index E0h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP0	R/W	8'h00	This byte is used as multi-purpose as follows: 1. AMD TSI reading if AMD TSI enable (0~255 °C). 2. Highest temperature among CPU, MCH and PCH if Intel IBX enable (0~255 ° C). 3. The 1st byte of read block protocol. To access this byte, MCH_BANK_SEL must set to "0".
	SMB_DATA0	R/W	8'h00	This byte is used as multi-purpose: 1. The received data of receive protocol. 2. The first received byte of read word protocol. 3. The 10th received byte of read block protocol. 4. The sent data for send byte protocol and write byte protocol. 5. The first send byte for write word protocol. 6. The first send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 1 – Index E1h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP1	R	8'h00	This byte is used as multi-purpose as follows: 1. The PCH temperature reading (0~255 °C). This byte is only valid if Intel IBX is enabled. 2. The 2nd byte of read block protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA1	R/W	8'h00	This byte is used as multi-purpose: 1. The second received byte of read word protocol. 2. The 11th received byte of read block protocol. 3. The second send byte for write word protocol. 4. The second send byte for write block protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 2 Low Byte – Index E2h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_LO	R	8'h00	This byte is used as multi-purpose as follows: 1. The low byte of Intel temperature interface CPU reading. The reading is the fraction part of CPU temperature. Bit 0 indicates the error status. Logic "1" indicates an error code. This byte is only valid if Intel IBX is enabled. 2. The 3rd byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA2	R/W	8'h00	This is the 12th byte of the block read protocol. This byte is also used as the 3rd byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 2 High Byte – Index E3h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP2_HI	R	8'h00	This byte is used as multi-purpose as follows: 1. The high byte of Intel temperature interface CPU reading. The reading is the decimal part of CPU temperature. This byte is only valid if Intel IBX is enabled. 2. The 4th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA3	R/W	8'h00	This is the 13th byte of the block read protocol. This byte is also used as the 4th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 3 – Index E4h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP3	R	8'h00	This byte is used as multi-purpose as follows: 1. The MCH temperature reading (0~255 °C). This byte is only valid if Intel IBX is enabled. 2. The 5th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA4	R/W	8'h00	This is the 14th byte of the block read protocol. This byte is also used as the 5th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 4 – Index E5h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP4	R	8'h00	This byte is used as multi-purpose as follows: 1. The DIMM0 temperature reading (0~255 °C). This byte is only valid if Intel IBX is enabled. 2. The 6th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA5	R/W	8'h00	This is the 15th byte of the block read protocol. This byte is also used as the 6th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 5 – Index E6h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP5	R	8'h00	This byte is used as multi-purpose: 1. The DIMM1 temperature reading (0~255 °C). This byte is only valid if Intel IBX is enabled. 2. The 7th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA6	R/W	8'h00	This is the 16th byte of the block read protocol. This byte is also used as the 7th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 6 – Index E7h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP6	R	8'h00	This byte is used as multi-purpose as follows: 1. The DIMM2 temperature reading (0~255 °C). This byte is only valid if Intel IBX is enabled. 2. The 8th byte of the block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA7	R/W	8'h00	This is the 17th byte of the block read protocol. This byte is also used as the 8th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

TSI Temperature 7 – Index E8h

Bit	Name	R/W	Default	Description
7-0	TSI_TEMP7	R	8'h00	This byte is used as multi-purpose: 1. The DIMM3 temperature reading (0~255 °C). The byte is only valid if Intel IBX is enabled. 2. The 9th byte of block read protocol. To access this byte, MCH_BANK_SEL should be set to "0".
	SMB_DATA8	R/W	8'h00	This is the 18th byte of the block read protocol. This byte is also used as the 9th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

SMB Data Buffer 9 – Index E9h (MCH_BANK_SEL = 1)

Bit	Name	R/W	Default	Description
7-0	SMB_DATA9	R/W	0	This is the 19th byte of the block read protocol. This byte is also used as the 10th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

SMB Data Buffer 10 – Index EAh (MCH_BANK_SEL = 1)

Bit	Name	R/W	Default	Description
7-0	SMB_DATA10	R/W	0	This is the 20th byte of the block read protocol. This byte is also used as the 11th byte of block write protocol. To access this byte, MCH_BANK_SEL should be set to "1".

Block Write Count Register – Index ECh

Bit	Name	R/W	Default	Description
7	MCH_BANK_SEL	R/W	0	This bit is used to select the register in index E0h to E9h. Set "0" to read the temperature bank and "1" to access the data bank.
6	Reserved	-	0	Reserved
5-0	BLOCK_WR_CNT	R/W	0	Use the register to specify the byte count of block write protocol. Support up to 10 bytes.

SMB Command Byte/TSI Comamdn Byte – Index EDh (TSI_CMD_PROG = 0)

Bit	Name	R/W	Default	Description
7-0	SMB_CMD	R/W	8'h0	Command code for write byte/word, read byte/word, block write/read and process call protocol.

SMB Command Byte/TSI Comamdn Byte – Index EDh (TSI_CMD_PROG = 1)

Bit	Name	R/W	Default	Description
7-0	TSI_CMD	R/W	8'h1	The command code for Intel temperature interface block read protocol and the data byte for AMD TSI send byte protocol.

SMB Status – Index EEh

Bit	Name	R/W	Default	Description
7	TSI_PENDING	R/W	0	Set 1 to pending auto TSI accessing. (In AMD model, auto accessing will issue a send-byte followed a receive-byte; In Intel model, auto accessing will issue a block read). To use the TSI_SCL/TSI_SDA as a SMBus master, set this bit to "1" first.
6	TSI_CMD_PROG	R/W	0	Set 1 to program TSI_CMD.
5	PROC_KILL	R/W	0	Kill the current SMBus transfer and return the state machine to idle. It will set a fail status if the current transfer is not completed.
4	FAIL_STS	R	0	This is set when PROC_KI LL kill an un-completed transfer. It will be auto cleared by next SMBus transfer.

3	SMB_ABT_ERR	R	0	This is the arbitration lost status if a SMBus command is issued. Auto cleared by next SMBus command.
2	SMB_TO_ERR	R	0	This is the timeout status if a SMBus command is issued. Auto cleared by next SMBus command.
1	SMB_NAC_ERR	R	0	This is the NACK error status if a SMBus command is issued. Auto cleared by next SMBus command.
0	SMB_READY	R	1	0: SMBus transfer is in process. 1: Ready for next SMBus command.

SMB Protocol Select – Index EFh

Bit	Name	R/W	Default	Description
7	SMB_START	W	0	Write "1" to trigger a SMBus transfer with the protocol specified by SMB_PROTOCOL.
6-4	Reserved	-	-	Reserved.
3-0	SMB_PROTOCOL	R/W	0	Select what protocol if SMBus transfer is triggered. 0001b: send byte. 0010b: write byte. 0011b: write word. 0100b: process call. 0101b: block write. 0111b: quick command (write). 1001b: receive byte. 1010b: read byte. 1011b: read word. 1101b: block read. 1111b: quick command (read). Otherwise: reserved.

7.3.5 HW Chip ID and Vender ID Information

HM Chip ID 1 Register — Index 5Ah

Bit	Name	R/W	Default	Description
7-0	HM_CHIP_ID1	R	03h	Chip ID 1 of HM Device.

HM Chip ID 2 Register — Index 5Bh

Bit	Name	R/W	Default	Description
7-0	HM_CHIP_ID2	R	04h	Chip ID 2 of HM Device.

HM Vendor ID 1 Register — Index 5Dh

Bit	Name	R/W	Default	Description
7-0	HM_VENDOR_ID1	R	19h	Vendor ID 1 of HM Device.

HM Vendor ID 2 Register — Index 5Eh

Bit	Name	R/W	Default	Description
7-0	HM_VENDOR_ID2	R	34h	Vendor ID 2 of HM Device.

7.4. Keyboard Controller

The KBC provides the functions included a keyboard and a PS/2 mouse, and can be used with IBM-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. The controller will assert an interrupt to the system when data are placed in its output buffer.

The below content is about the KBC device register descriptions. All the registers are for software porting reference.

Status Register

The status register is an 8 bits register at I/O address 64h that provides information about the status of the KBC

Bit	Name	R/W	Default	Description
7	Parity error	R	0	0:odd parity 1:even parity
6	Time out	R	0	0:no time out error 1:time out error
5	Auxiliary device OBF	R	0	0: Auxiliary output buffer empty 1: Auxiliary output buffer full
4	Inhinit	R	0	0:keyboard is inhibited 1: keyboard is not inhibited
3	Command/data	R	0	0:data byte 1:command byte
2	SYSTEM_FLAG	R	0	This bit is set or clear by command byte of KBC
1	IBF	R	0	0:input buffer empty 1: input buffer full
0	OBF	R	0	0:output buffer empty 1: output buffer full

Command register

The internal KBC operation is controlled by the KBC command byte (KCCB). The KCCB resides in I/O address 64h that is read with a 20h command and written with a 60h command data.

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	Translate code	R/W	1	0: Pass un-translated scan code. 1: Translate scan code to IBM PC standard.
5	Disable Auxiliary Device	R/W	0	1: Disable Auxiliary inhibit function.
4	Disable Keyboard	R/W	0	1: Disable keyboard inhibit function.
3	Reserved	-	-	Reserved
2	System flag	R/W	1	0: The system is executing POST as a result of a cold boot. 1: The system is executing POST as a result of a shutdown or warm boot.

1	Enable Auxiliary Interrupt	R/W	1	0: Ao interrupt 1: A system interrupt is generated when a byte is placed in output buffer (IRQ12).
0	Enable keyboard Interrupt	R/W	1	0:No interrupt 1: A system interrupt is generated when a byte is placed in output buffer (IRQ1).

DATA register

The DATA register is an 8 bits register at I/O address 60h. the KBC used the output buffer to send the scan code received from keyboard and data byte replay by command to the system.

Power on default <7:0> = 00000000 binary

Commands

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte</td></tr>
<tr><td>60h</td><td>Write Command Byte
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
<tr><td>1</td><td>Enable Mouse Interrupt</td></tr>
<tr><td>2</td><td>System flag</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>4</td><td>Disable Keyboard Interface</td></tr>
<tr><td>5</td><td>Disable Mouse interface</td></tr>
<tr><td>6</td><td>IBM keyboard Translate Mode</td></tr>
<tr><td>7</td><td>Reserve</td></tr>
</table></td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Auxiliary Interface Test
8’h00: indicate Auxiliary interface is ok.
8’h01: indicate Auxiliary clock is low.
8’h02: indicate Auxiliary clock is high
8’h03: indicate Auxiliary data is low
8’h04: indicate Auxiliary data is high</td></tr>
<tr><td>AAh</td><td>Self-test
Returns 055h if self test succeeds</td></tr>
<tr><td>ABh</td><td>keyboard Interface Test
8’h00: indicate keyboard interface is ok.
8’h01: indicate keyboard clock is low.
8’h02: indicate keyboard clock is high.
8’h03: indicate keyboard data is low.
8’h04: indicate keyboard data is high.</td></tr>
<tr><td>ADh</td><td>Disable Keyboard Interface</td></tr>
</table>

AEh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into STATUS register
C2h	Continuously puts the upper four bits of Port1 into STATUS register
CAh	Read the data written by CBh command.
CBh	Written a scratch data. This byte could be read by CAh command.
D0h	Send Port2 value to the system
D1h	Only set/reset GateA20 line based on the system data bit 1
D2h	Send data back to the system as if it came from Keyboard
D3h	Send data back to the system as if it came from Muse
D4h	Output next received byte of data from system to Mouse
FEh	Pulse only RC (the reset line) low for 6μS if Command byte is even

KBC Command Description

PS2 wakeup function

The KBC supports keyboard and mouse wakeup function, keyboard wakeup function has 8 kinds of conditions, when key is pressed combinational key (1) CTRL +ESC (2) CTRL+F1 (3) CTRL+SPACE (4) ANY KEY (5) windows 98 wakeup up key (6) windows 98 Power key (7) CTRL + ALT + Backspace (8) CTRL + Alt + Space. Mouse wakeup function has 2 kinds of conditions, when mouse is pressed via (1) BUTTON CLICKING or (2) BUTTON CLICKING AND MOVEMENT, KB/MO will assert PME signal. Those wakeup conditions are controlled by the configuration register.

7.5. 80 Port

Monitor the value of 0x80 port and output the value via the signals defined for 7-segment display. High nibble and low nibble are output interleaved at 1KHz frequency.

7.6. ACPI Function

The Advanced Configuration and Power Interface (ACPI) is a system for controlling the use of power in a computer. It lets computer manufacturer and user to determine the computer's power usage dynamically.

There are three ACPI states that are of primary concern to the system designer and they are designated S0, S3 and S5. S0 is a full-power state; the computer is being actively used in this state. The other two are called sleep states and reflect different power consumption when power-down. S3 is a state that the processor is powered down but the last procedural state is being stored in memory which is still active. S5 is a state that memory is off and the last procedural state of the processor has been stored to the hard disk. Take S3 and S5 as comparison, since memory is fast, the computer can quickly come back to full-power state, the disk is slower than the memory and the computer takes longer time to come back to

full-power state. However, since the memory is off, S5 draws the minimal power comparing to S0 and S3.

It is anticipated that only the following state transitions may happen:

S0→S3, S0→S5, S5→S0, S3→S0 and S3→S5.

Among them, S3→S5 is illegal transition and won't be allowed by state machine. It is necessary to enter S0 first in order to get to S5 from S3. As for transition S5→S3 will occur only as an immediate state during state transition from S5→S0. It isn't allowed in the normal state transition.

The below diagram described the timing, the always on and always off, keep last state could be set in control register. In keep last state mode, one register will keep the status of before power loss. If it is power on before power loss, it will remain power on when power is resumed (system would send the PSOUT# automatically), otherwise, if it is power off before power loss, it will remain power off when power is resumed.

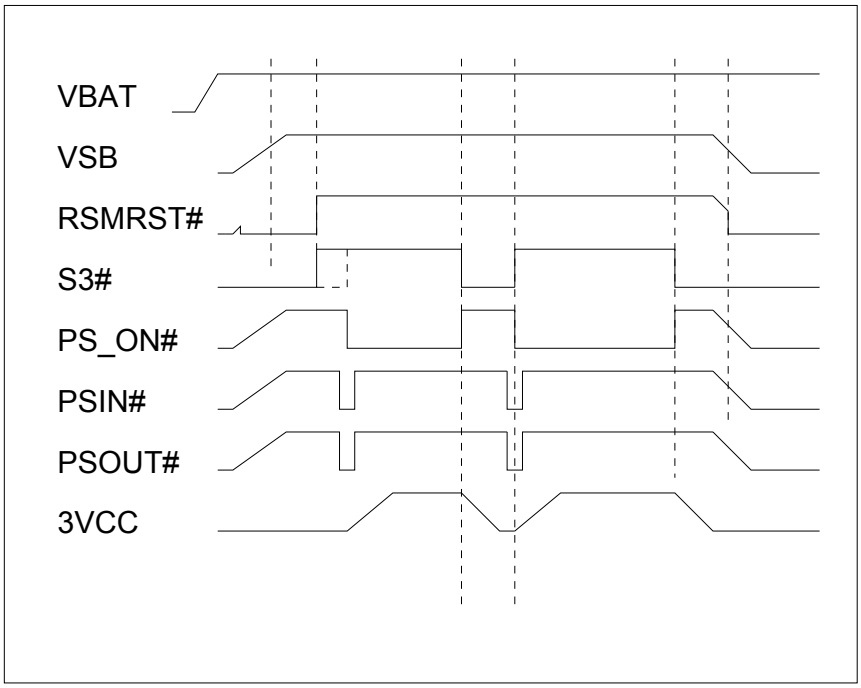


Figure 18 Default timing: Always off

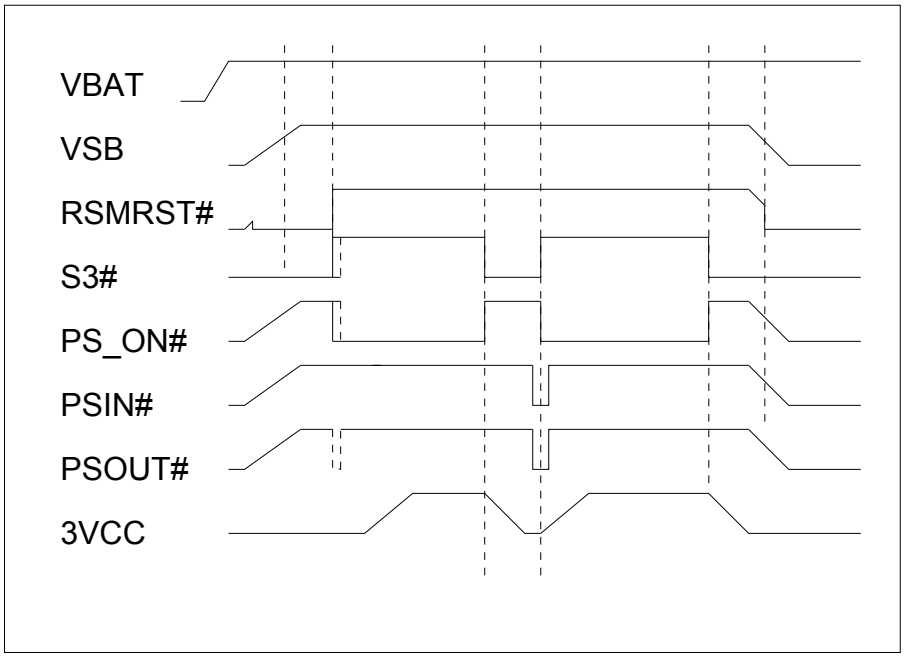
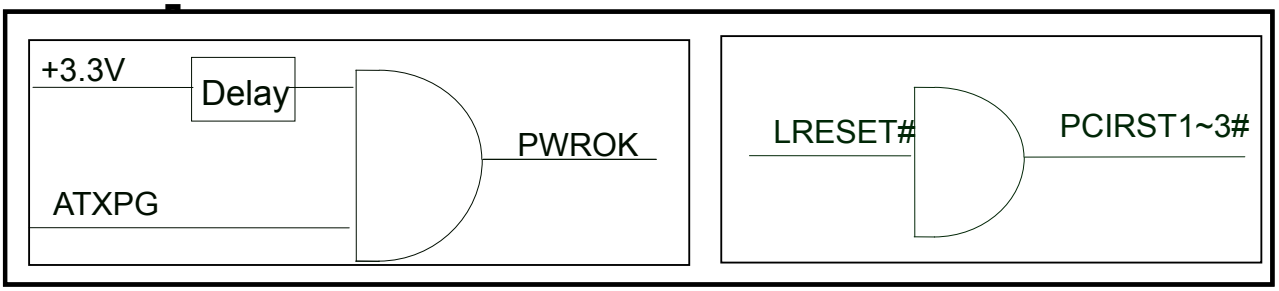


Figure 19 Optional timing: Always on

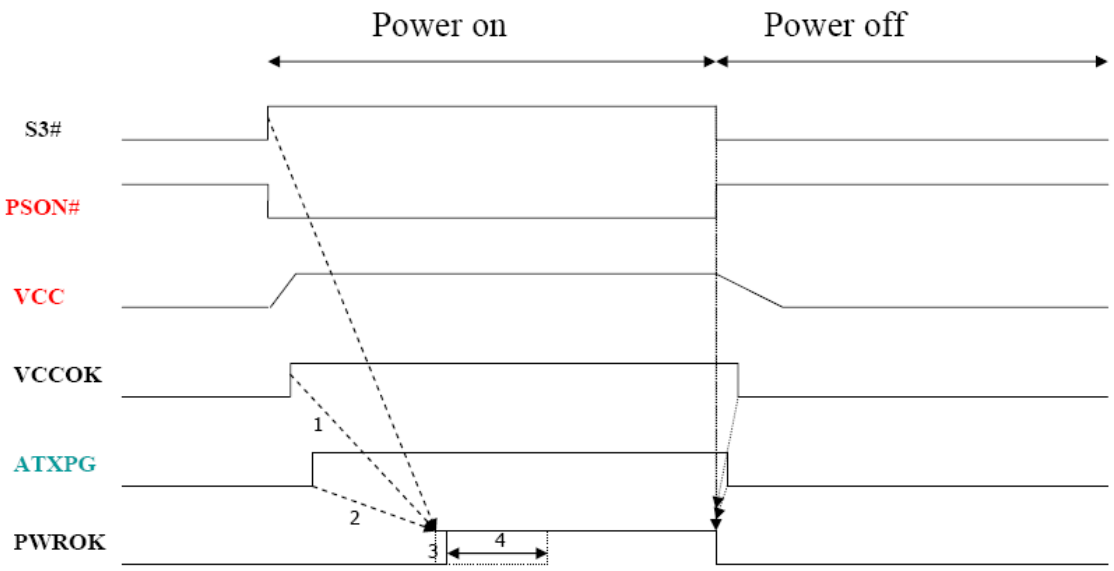
PCI Reset and PWROK Signals

The F71889A supports 3 output buffers for 3 reset signals. The result of PCIRST# outcome will be affected by conditions as below:

PCIRST1# → Output buffer of LRESET#.
PCIRST2# → Output buffer of LRESET#.
PCIRST3# → Output buffer of LRESET#.



PWROK



1. VCCOK delay 100/200/300/400ms (default)
2. Delay 100~120ms
3. Delay 1ms
4. Extra delay: 0 (default) /100/200/400ms

So far as the PWROK issue is as the figure above. PWROK is delayed 100ms (default) as 3VCC arrives 2.8V, and the delay timing can be programmed by register. (100ms ~ 400ms)

The F71889A also supports 3 output voltages for VREF1~3. The output is generated from DACs which is powered by trimmed 2.304V reference voltage. One LSB is 2.304V/256.

Below is the timing sequence between VREF1~3 pins:

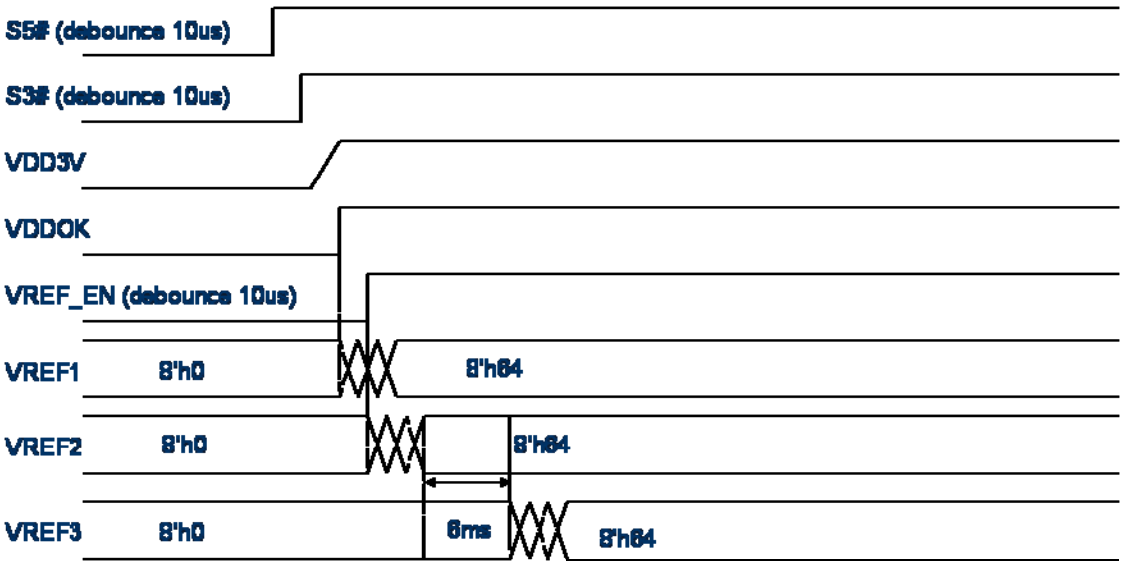


Figure 20 VREF timing: S5→S0

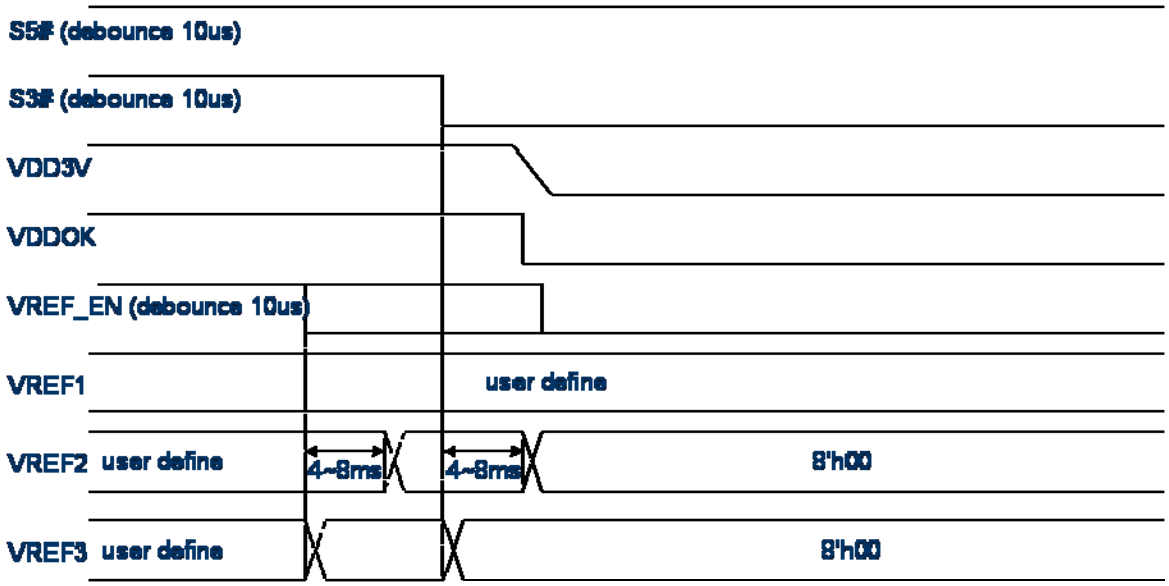


Figure 21 VREF timing: S0→S3

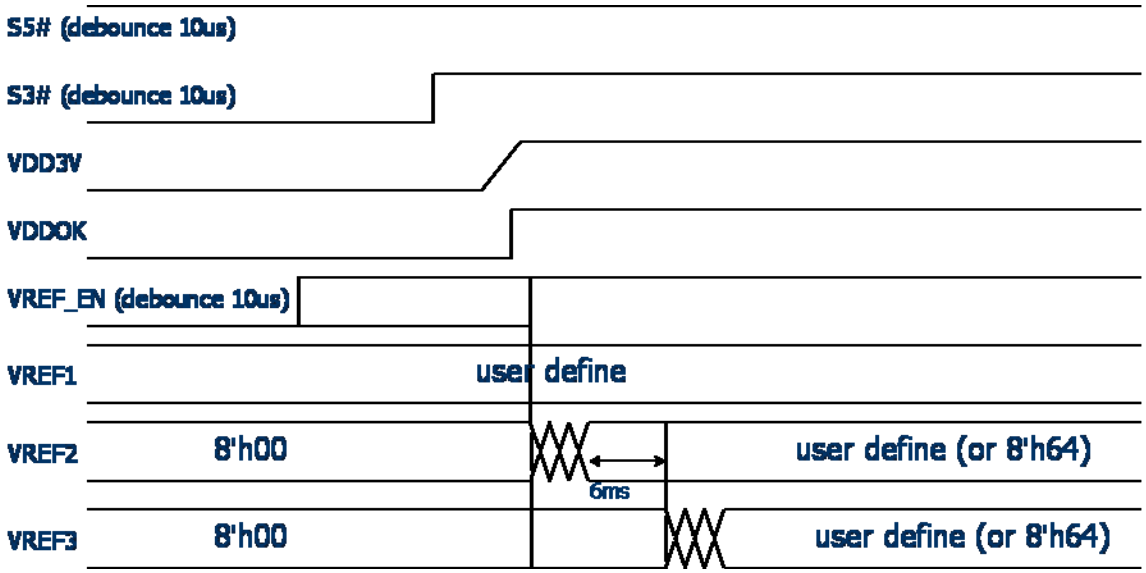
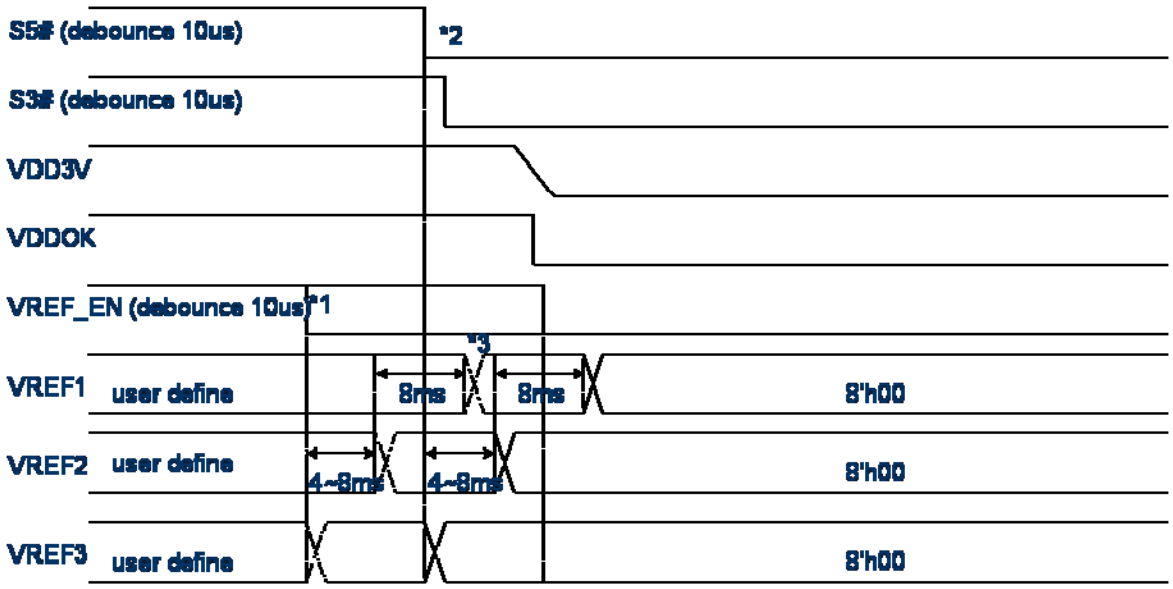


Figure 22 VREF timing: S3→S0



*1: VREF_EN de-active before S5# active.
*2: S5# active before VREF_EN de-active.
*3: VRAM power down after 8ms of VSYS power down and S5# active.

Figure 23 VREF timing: S0→S5

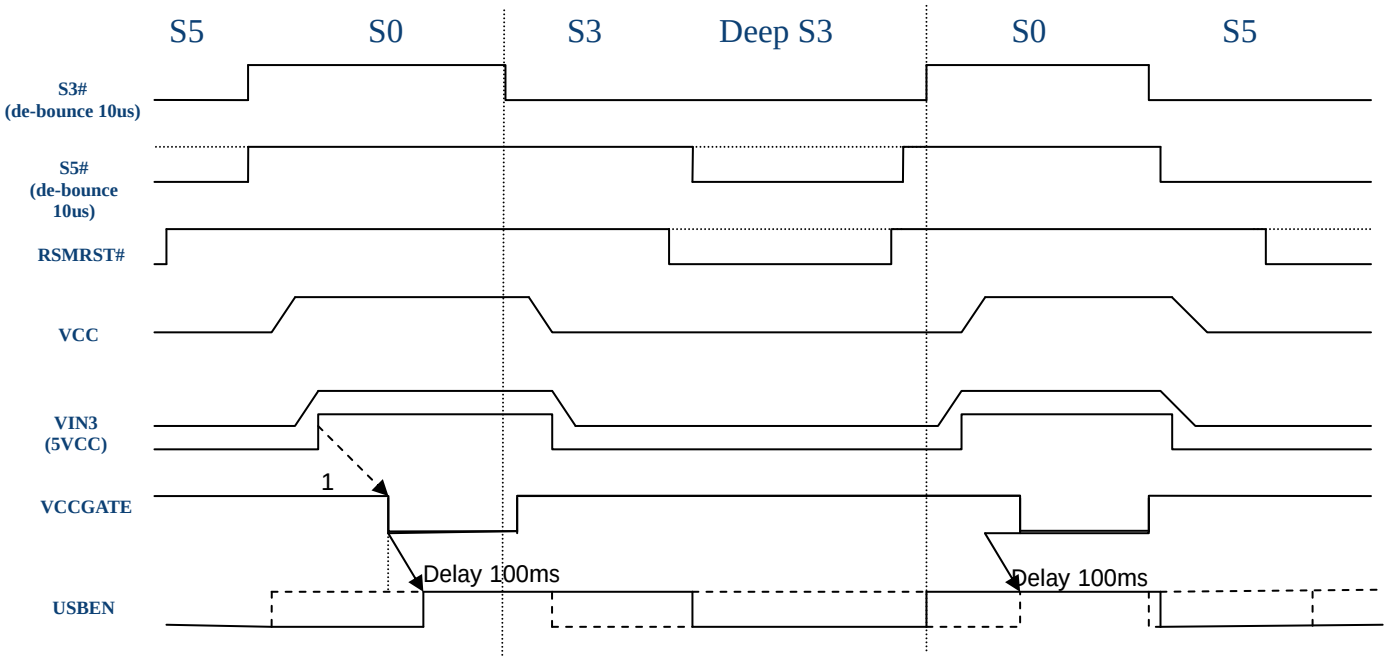


Figure 24 VCCGATE & USBEN timing

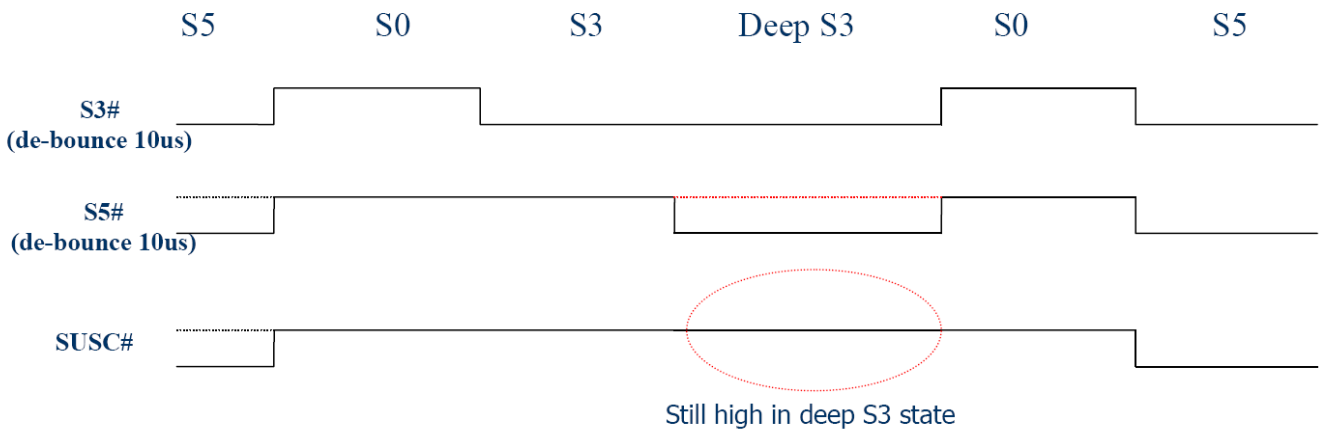


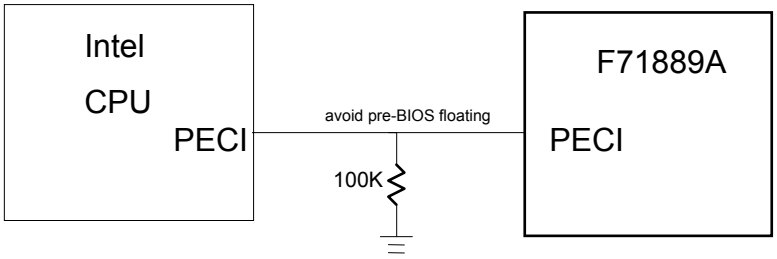
Figure 25 SUSC# timing

7.7. PECI Function

The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked on-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic '0' or login '1'. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

F71889A can connect to CPU & read the temperature data from CPU directly. Then the fan control machine of F71889A can implement the fan to cool down CPU temperature. The application circuit is as below.



INTEL PECI Typical Application

The F71889A integrated most of PECI 3.0 commands for the future advantage application. More detail, please refer to the register descriptions.

F71889A Support	PECI 3.0 Command Name	PECI 1.0 Command Name	Status
V	Ping( )	Ping( )	
V	GetTemp( )	GetTemp( )	
V	GetDIB( )		
V	RdIAMSR( )		
-	WrIAMSR( )		
-	RdPCIConfigLocal( )		Not Available in Mobile/DT
-	WrPCIConfigLocal( )		Not Available in Mobile/DT
-	RdPCIConfig( )		Not Available in Mobile/DT
-	WrPCIConfig( )		Not Available in Mobile/DT
V	RdPkgConfig( )		
V	WrPkgConfig( )		

7.8. SST Function

The Simple Serial Transfer (SST) temperature sensor provides a mean to digitize an analog signal and send that information over a digital bus enabling remote temperature sensing in areas previously not monitored in the PC. The temperature sensor supports an internal and external thermal diode.

The Simple Serial Transfer (SST) interface provides sensed temperatures and voltages. The sensed temperatures are T1, T2, and T3 whose reading values stored in CR72h, CR74h, and CR76h. The sensed voltages are V1~V6 whose reading values stored in CR21h~26h.

7.9. TSI Function

The Temperature Sensor Interface (TSI) was a simple SMBUS master to communicate with AMD CPU or Intel CPU to getting the temperature of CPU. It supports byte sending, byte reveiving, read/write byte, read/write block and quick command of SMBus protocol. When power on the hardware automatically fetch the temperature use the protocol per the specification of AMD/Intel. User can use the provided registers to control the SCL/SDA as a SMBus master. For Intel platform, the SMBUS supports next generational IBX protocol for temperature reading.

7.10. Power Saving Function

ERP Power Saving Function

ERP_CTRL0#, ERP_CTRL1#, and ERP_CTRL2# control the standby power rail on/off to fulfill the purpose to decrease the power consumption when the system is under the sleep state or the soft-off state. Those three pins are connected to the external PMOSs with the default high in the

sleep state in order to cut off all the standby power rails to save the power consumption. If the system needs to support wake-up function, those three pins can be programmable to set which power rail is needed to be turned on. The programmable register is powered by battery. So, the setting will be kept even the AC power is lost after the register is set. At the power saving state (FINTEK calls it G3-like state), the F71889A consumes 5VSB power rail only to realize a low power consumption system. F71889A supports wake up events via EVENT_IN0#, EVENT_IN1#, KB/MO & CIR function from S3/S5 state.

Intel Cougar Point Timing (CPT)

The F71889A supports Intel Cougar Point Chipset (CPT) timing for Sandy Bridge Platform. There are 4 pins for CPT control: SUS_WARN#, SUS_ACK#, SLP_SUS# and DPWROK.

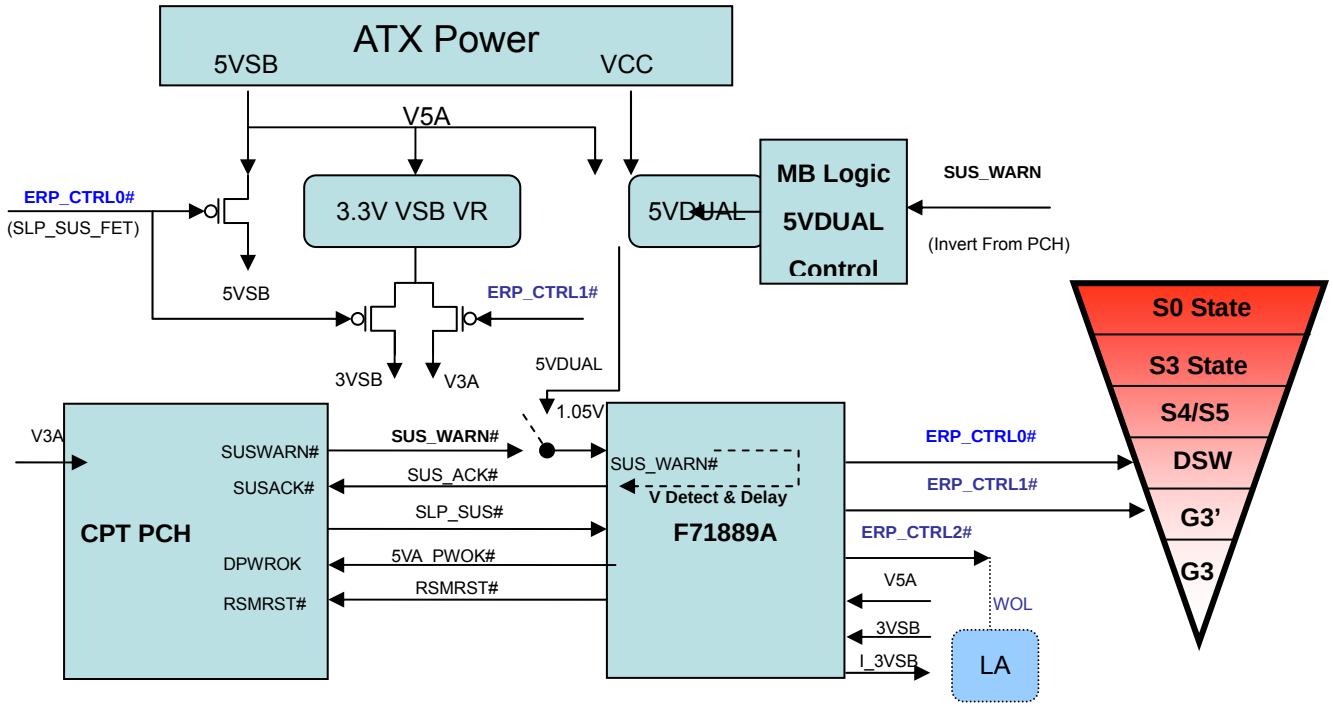
For entering Intel Deep Sleep Well (DSW) state, the PCH will assert SUS_WARN# and turn off 5VDUAL. After the level of 5VDUAL is lower than 1.05V, F71889A will assert SUS_ACK# to inform PCH to ready for entering DSW. Finally, PCH will ramp down the internal VccSUS and assert SLP_SUS# to F71889A. F71889A will turn off the 5VSB and 3VSB by ERP_CTRL0# and enter the DSW state.

To exit DSW state, PCH will de-assert SLP_SUS#, turn on the SUS rail FETs and ramp up internal 1.05V VccSUS. After the SUS rails voltages are up, RSMRST# will be desserted and the PCH will release SUS_WARN# so that the 5VDUAL will ramp up.

Because the DSW function is controlled by F71889A instead of controlled by PCH directly, there will be more wakeup events such as LAN, KB/Mouse, SIO RI# wake up rather than the 3 wakeup events (RTC, Power Button and GPIO27) for Intel DSW.

In order to achieve lower power consumption, F71889A provides the ERP_CTRL1# to turn off the V3A so that the system can enter the Fintek G3' state. If it's required to provide wake on LAN (WOL) or other wake on devices functions, F71889A also support one extra ERP_CTRL2# pin to realize this function.

The block diagram below shows how the connection and control method for F71889A and PCH.



7.11. CIR Function

The F71889A is compatible with Microsoft Windows Vista and Windows 7 IR Receiver or Transceiver Emulation Device which supports RC6 & QP protocol. It Supports 1 IR transceiver functions for blaster application and 1 IR receiver with long range frequency and another with wide band application. The wide-band receiver is necessary to support IR learning, IR-blasting and set-top box control.

The long-range receiver is a receiver which has the following characteristics:

1. Works at a distance of 10 meters.
2. Demodulates the signal inside the receiver part
3. Has a BPF which works with carriers from 32-60 kHz.

The wide-band receiver is a receiver part which has the following characters:

1. Works at a distance of approximately 5 centimeters.
2. Does not demodulate the signal inside the receiver part
3. Works with carriers from 32-60 kHz (Probably doesn't have a BPF, but still has the same or wider range).

In power function, The F71889A supports Vista and Windows 7 wakeup programming function when the PC is in the S3 state. The F71889A decodes IR protocol via the same Vista and Windows 7

wakeup programming key. The F71889A is asserted PME or PSOUT to wakeup PC system.The wake up programming function is reference from Microsoft Vista and windows 7 remote controller specification.

Please reference Microsoft Windows Vista / 7 IR receiver or transceiver emulation device spec. for further detail.

7.12. Scan Code Function

F71889A three GPIO pins, GPIO 50/51/52, can emulate KBC command and then assert make/break scan code. Those pins can not only be set to volume up/down, and mute but also any function keys on keyboard. Because the protocol for those pins is scan code, so it doesn't require a driver to connect this function to OS. If the button for the GPIO has been pressed continuesly over nearly 1 second (delay time), the GPIO will repeatedly sending this function in an interval of 50 ms (repeat time). The delay time could be set from 0.5 to 1 sec (Unit: 0.5s).

8 Register Description

The configuration register is used to control the behavior of the corresponding devices. To configure the register, using the index port to select the index and then writing data port to alter the parameters. The default index port and data port are 0x4E and 0x4F respectively. Pull down the SOUT1 pin to change the default value to 0x2E/0x2F. To enable configuration, the entry key 0x87 must be written to the index port. To disable configuration, write exit key 0xAA to the index port. Following is a example to enable configuration and disable configuration by using debug.

-o 4e 87
-o 4e 87 (enable configuration)
-o 4e aa (disable configuration)

The Following is a register map (total devices) grouped in hexadecimal address order, which shows a summary of all registers and their default value. Please refer each device chapter if you want more detail information.

"-" Reserved or Tri-State

Global Control Registers									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
02	Software Reset Register	0	-	-	-	-	-	-	0
07	Logic Device Number Register (LDN)	0	0	0	0	0	0	0	0
20	Chip ID Register	0	0	0	1	0	0	0	0
21	Chip ID Register	0	0	0	0	0	1	0	1
23	Vender ID Register	0	0	0	1	1	0	0	1
24	Vender ID Register	0	0	1	1	0	1	0	0
25	Software Power Down Register	-	-	-	0	0	0	0	0
26	UART IRQ Sharing Register	0	-	0	-	-	0	0	0
27	Configuration Port Select Register	1/0	-	-	1/0	-	-	1/0	1/0
28	80 Port Enable Register	-	0	0/1	0	-	-	-	-
29	Multi Function Select 4 Register	0	0	0	0	0	0	0	0
2A	Multi Function Select 1 Register	1	1	1	1	0	0	0	0
2B	Multi Function Select 2 Register	0	0	1	1	0	0	0	0
2C	Multi Function Select 3 Register	0	0	0	1	0	0	0	0
2D	Wakeup Control Register	0	0	0	0	1	0	0	0

"-" Reserved or Tri-State

UART1 Device Configuration Registers (LDN CR01)									
Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART1 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	1	1	1	1	1	0	0	0

70	IRQ Channel Select Register	-	-	-	-	0	1	0	0
F0	RS485 Enable Register	-	-	-	0	-	-	-	-

UART2 Device Configuration Registers (LDN CR02)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	UART2 Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	0	1	1
F0	RS485 Enable Register	-	-	-	0	0	0	-	-
F1	SIR Mode Control Register	-	-	-	0	0	1	0	0

Parallel Port Device Configuration Registers (LDN CR03)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	Parallel Port Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	1
61	Base Address Low Register	0	1	1	1	1	0	0	0
70	IRQ Channel Select Register	-	-	-	-	0	1	1	1
74	DMA Channel Select Register	-	-	-	0	-	0	1	1
F0	PRT Mode Select Register	0	1	0	0	0	0	1	0

Hardware Monitor Device Configuration Registers (LDN CR04)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	H/W Monitor Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	1	0
61	Base Address Low Register	1	0	0	1	0	1	0	1
70	IRQ Channel Select Register	-	-	-	-	0	0	0	0

KBC Device Configuration Registers (LDN CR05)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	KBC Device Enable Register	-	-	-	-	-	-	-	1
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	1	1	0	0	0	0	0
70	KB IRQ Channel Select Register	-	-	-	-	0	0	0	1
72	Mouse IRQ Channel Select Register	-	-	-	-	1	1	0	0
FE	Auto Swap Register	1	-	-	0	0	0	0	1
FF	User Wakeup Code Register	0	0	1	0	1	0	0	1

GPIO Device Configuration Registers (LDN CR06)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
F0	GPIO Output Enable Register	-	0	0	0	0	0	0	0
F1	GPIO Output Data Register	-	1	1	1	1	1	1	1
F2	GPIO Pin Status Register	-	-	-	-	-	-	-	-
F3	GPIO Drive Enable Register	-	0	0	0	0	0	0	0
FE	LED_VSB Control Register	-	0	0	0	0	0	0	0
FF	LED_VCC Control Register	0	0	0	0	0	0	0	0
E0	GPIO1 Output Enable Register	-	0	0	0	0	0	0	0
E1	GPIO1 Output Data Register	-	1	1	1	1	1	1	1
E2	GPIO1 Pin Status Register	-	-	-	-	-	-	-	-
E3	GPIO1 Drive Enable Register	-	0	0	0	0	0	0	0
D0	GPIO2 Output Enable Register	0	0	0	-	-	-	-	-
D1	GPIO2 Output Data Register	1	1	1	-	-	-	-	-
D2	GPIO2 Pin Status Register	-	-	-	-	-	-	-	-

D3	GPIO2 Drive Enable Register	0	0	0	-	-	-	-	-
C0	GPIO3 Output Enable Register	0	0	0	0	0	0	0	0
C1	GPIO3 Output Data Register	1	1	1	1	1	1	1	1
C2	GPIO3 Pin Status Register	-	-	-	-	-	-	-	-
C3	GPIO3 Drive Enable Register	0	0	0	0	0	0	0	0
B0	GPIO4 Output Enable Register	0	0	0	0	0	0	0	0
B1	GPIO4 Output Data Register	1	1	1	1	1	1	1	1
B2	GPIO4 Pin Status Register	-	-	-	-	-	-	-	-
A0	GPIO5 Output Enable Register	-	-	-	0	0	0	0	0
A1	GPIO5 Output Data Register	-	-	-	1	1	1	1	1
A2	GPIO5 Pin Status Register	-	-	-	-	-	-	-	-
A4	GPIO5 PME Enable Register	-	-	-	0	0	0	0	0
A5	GPIO5 Input Event Detection Select Register	-	-	-	0	0	0	0	0
A6	GPIO5 Event Status Register	-	-	-	0	0	0	0	0
AB	GPIO52 KBC Emulation Make Code Register	0	0	0	0	0	0	0	0
AC	GPIO51 KBC Emulation Make Code Register	0	0	0	0	0	0	0	0
AD	GPIO50 KBC Emulation Make Code Register	0	0	0	0	0	0	0	0
AE	GPIO5 KBC Emulation Prefix Code Register	1	1	1	0	0	0	0	0
AF	GPIO5 KBC Emulation Control Register	0	0	0	0	0	0	0	0
90	GPIO6 Output Enable Register	0	0	0	0	0	0	0	0
91	GPIO6 Output Data Register	1	1	1	1	1	1	1	1
92	GPIO6 Pin Status Register	-	-	-	-	-	-	-	-
93	GPIO6 Drive Enable Register	0	0	0	0	0	0	0	0
80	GPIO7 Output Enable Register	0	0	0	0	0	0	0	0
81	GPIO7 Output Data Register	1	1	1	1	1	1	1	1
82	GPIO7 Pin Status Register	-	-	-	-	-	-	-	-
83	GPIO7 Drive Enable Register	0	0	0	0	0	0	0	0

VID Device Configuration Registers (LDN CR07)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	VID Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0
61	Base Address Low Register	0	0	0	0	0	0	0	0
F0	Watchdog Timer Configuration Register 1	0	-	-	-	-	-	-	0
F2	BUS Manual Register	0	-	0	0	0	0	0	0
F3	Key Data Register	0	0	0	0	0	0	0	0
F4	BUSIN Status Register	0	0	0	0	0	-	-	-
F5	WDT (Watchdog Timer) Configuration Register 2	-	0	0	0	0	0	0	0
F6	WDT (Watchdog Timer) Configuration Register 3	0	0	0	0	0	0	0	0
F7	NB Offset Register	0	0	0	0	0	0	0	0
F8	VDD0 Offset Register	0	0	0	0	0	0	0	0
F9	VDD1 Offset Register	0	0	0	0	0	0	0	0
FA	Watchdog Timer PME Register	0	0	0	0	0	0	0	0
FB	VDD NB Manaul Register	0	0	0	0	0	0	0	0
FC	VDD0 Manaul Register	0	0	0	0	0	0	0	0
FD	VDD1 Manaul Register	0	0	0	0	0	0	0	0
FE	PSI Control Register	0	0	0	0	1	1	1	0

CIR Device Configuration Registers (LDN CR08)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	CIR Device Enable Register	-	-	-	-	-	-	-	0
60	Base Address High Register	0	0	0	0	0	0	0	0

61	Base Address Low Register	0	0	0	0	0	0	0	0
70	CIR IRQ Channel Select Register	-	-	-	-	0	0	0	0
F0	Reserved	-	-	-	-	-	-	-	-
F1	Reserved	-	-	-	-	-	-	-	-
F8	Reserved	0	0	0	0	0	0	0	0
F9	Reserved	0	0	0	0	0	0	0	0
FA	Reserved	1	0	0	0	0	0	0	0
FB	Reserved	0	0	1	1	1	0	1	1
FC	Reserved	0	0	0	0	0	0	0	0
FD	Reserved	0	0	0	0	0	0	0	0
FE	Reserved	0	0	0	0	0	0	0	0

PME, ACPI and ERP Device Configuration Registers (LDN CR0A)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
30	PME Device Enable Register	-	-	-	-	-	-	-	0
F0	PME Event Enable 1 Register	-	0	0	0	0	0	0	0
F1	PME Event Status 1 Register	-	-	-	-	-	-	-	-
F2	PME Event Enable 2 Register	-	-	-	0	-	0	0	0
F3	PME Event Status 2 Register	-	-	-	-	-	-	-	-
F4	ACPI Control Register1	0	0	1	0	0	1	1	0
F5	ACPI Control Register2	0	0	0	0	0	1	0	0
F6	ACPI Control Register3	0	-	0	0	0	1	1	1
F7	ACPI Control Register 4	0	0	-	1	-	-	0	0
FA	LED Mode Select Register	-	0	0	0	-	0	0	0
FC	Intel DSW Delay Register	-	-	-	0	0	0	0	0
FD	Trim Data Register (Fintek test mode)	-	-	-	0	-	0	0	0
FE	RI De-bounce Select Register	-	-	-	0	-	-	0	0
E0	ERP Enable Register	1	0	-	-	0	0	0	0
E1	ERP control register 1	1	1	0	0	1	1	0	0
E2	ERP control register 2	-	-	0	0	1	1	0	0
E3	ERP PSIN deb-register	0	0	0	1	0	0	1	1
E4	ERP RSMRST deb-register	0	0	0	0	1	0	0	1
E5	ERP PSOUT deb-register	1	1	0	0	0	1	1	1
E6	ERP PSON deb-register	0	0	0	0	1	0	0	1
E7	ERP S5 deb-register	0	1	1	0	0	0	1	1
E8	ERP Wakeup Event Enable Register	0	-	0	1	-	0	0	0
E9	ERP Deep S3 Delay Register	0	0	0	0	1	1	1	1
EC	ERP Control Register 3	0	0	0	0	1	0	1	0
ED	ERP Watchdog Control Register	-	-	-	0	-	-	0	0
EE	ERP Watchdog Time Register	0	0	0	0	0	0	0	0

Vref Control Device Configuration Registers (LDN CR0B)

Register 0x[HEX]	Register Name	Default Value MSB							LSB
F0	VREF3 output value	0	1	1	0	0	1	0	0
F1	VREF2output value	0	1	1	0	0	1	0	0
F2	VREF1 output value	0	1	1	0	0	1	0	0
F3	Voltage LSB	-	-	-	-	-	0	0	0
FF	WDT Reset Enable	-	-	-	-	-	-	-	0

8.1 Global Control Registers

8.1.1 Software Reset Register — Index 02h

Bit	Name	R/W	Default	Description
7	Temp_Update_Rate	R/W	0	0: Digital interface (PECI/TSI/IBX) transmits when every temperature updates 1: Digital interface (PECI/TSI/IBX) transmits when every four times temperature updates
6-1	Reserved	-	-	Reserved
0	SOFT_RST	R/W	0	Write 1 to reset the register and device powered by VDD (3VCC).

8.1.2 Logic Device Number Register (LDN) — Index 07h

Bit	Name	R/W	Default	Description
7-0	LDN	R/W	00h	00h: Reserved. 01h: Select UART 1 device configuration registers. 02h: Select UART 2 device configuration registers. 03h: Select Parallel Port device configuration registers. 04h: Select Hardware Monitor device configuration registers. 05h: Select KBC device configuration registers. 06h: Select GPIO device configuration registers. 07h: Select VID device configuration registers. 07h: CIR device configuration registers. 0Ah: Select PME, ACPI & ERP device configuration registers. 0Bh: Select VREF Control device configuration registers.

8.1.3 Chip ID Register — Index 20h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	10h	Chip ID1.

8.1.4 Chip ID Register — Index 21h

Bit	Name	R/W	Default	Description
7-0	CHIP_ID2	R	05h	Chip ID2.

8.1.5 Vendor ID Register — Index 23h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID1 of Fintek devices.

8.1.6 Vendor ID Register — Index 24h

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID2 of Fintek devices.

8.1.7 Software Power Down Register — Index 25h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved

4	SOFTPD_HM	R/W	0	Power down the Hardware Monitor device. This will stop the Hardware Monitor clock.
3	SOFTPD_PRT	R/W	0	Power down the Parallel Port device. This will stop the Parallel Port clock.
2	SOFTPD_UR2	R/W	0	Power down the UART 2 device. This will stop the UART 2 clock.
1	SOFTPD_UR1	R/W	0	Power down the UART 1 device. This will stop the UART 1 clock.
0	SOFTPD_FDC	R/W	0	Power down the FDC device. This will stop the FDC clock.

8.1.8 UART IRQ Sharing Register — Index 26h

Bit	Name	R/W	Default	Description
7	CLK24M_SEL	R/W	0	0: CLKIN is 48MHz 1: CLKIN is 24MHz
6	Reserved	-	-	Reserved.
5	DPORT_DEC_SEL	R/W	0	0: The 80 Port address is decoded as 0x0080. 1: The 80 port address is decoded as the SCR of UART2. This bit is powered by VBAT.
4-3	Reserved	-	-	Reserved.
2	TX_DEL_1BIT	R/W	0	0: UART TX transmits data immediately after write THR. 1: UART TX transmits data delay 1 bit time after write THR.
1	IRQ_MODE	R/W	0	0: PCI IRQ sharing mode (low level). 1: ISA IRQ sharing mode (low pulse).
0	IRQ_SHAR	R/W	0	0: disable IRQ sharing of two UART devices. 1: enable IRQ sharing of two UART devices.

8.1.9 ROM Address Select Register — Index 27h

Bit	Name	R/W	Default	Description
7	OVP_MODE	R/W	-	1: Alarm mode voltage protection. Voltage protection is enabled by register. 0: Force mode voltage protection. Voltage protection is enabled after power on. The default value is determined by OVP_STRAP pin on power on.
6-5	Reserved	-	-	Reserved.
4	PORT_4E_EN	R/W	-	0: The configuration register port is 2E/2F. 1: The configuration register port is 4E/4F. This register is power on trapped by SOUT1/ Config4E_2E. Pull down to select port 2E/2F.
3-2	Reserved	-	-	Reserved.
1-0	LPT_FUNC_SEL	R/W	-	00: The parallel port pins function as LPT. 01: Reserved. 10: The parallel port pins function as GPIOs.

8.1.10 80 Port Enable Register — Index 28h

Bit	Name	R/W	Default	Description
7	LPT_DPORT_EN	R/W	-	0: The 80 port data could not be output to LPT pins. 1: The 80 port data could be output to LPT pins in DPORT_EN is set to “1”.
6	CIR_LED_GP40_EN	R/W	0	GPIO40/CIR_LED# function select. The pin function is controlled by {CIR_LED_GP40_EN, FDC_GP_EN} 1x: The pin function is CIR_LED#. 01: The pin function is GPIO 40. 00: Reserved.
5	DPORT_EN	R/W	-	0: The 80 port function is disabled. 1: The 80 port function is enabled.
4	TEMP_OUT_EN	R/W	0	Set this bit to “1” will output the CPU temperature to the 7-segment LED.
3-0	Reserved	-	-	Reserved.

8.1.11 Multi Function Select 4 Register — Index 29h (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	FDC_GP_RST_SEL	R/W	0	This bit selects the reset signal for GPIO4 and GPIO5. 0: Reset by internal VSB5V power good. 1: Reset by LRESET#.
6	TSI_GP16_EN	R/W	0	PECI/TSI_DAT/IBX_DAT/GPIO16 function select. The pin function is controlled by {TSI_GP16_EN, GPIO16_EN} 1x: The pin function is TSI_DAT/IBX_DAT. 01: The pin function is GPIO16. 00: The pin function is PECI.
5	TSI_GP15_EN	R/W	0	SST/TSI_CLK/IBX_CLK/GPIO15 function select. The pin function is controlled by {TSI_GP15_EN, GPIO15_EN} 1x: The pin function is TSI_CLK/IBX_CLK. 01: The pin function is GPIO15. 00: The pin function is SST.
4	GPIO14_LV_SEL	R/W	0	CIRWB#/TSI_DAT/IBX_DAT/GPIO14 input level select. 0: TTL input level. 1: Low input level. 0.9V for high and 0.6V for low.
3	GPIO13_LV_SEL	R/W	0	CIRTX/TSI_CLK/IBX_CLK/GPIO13 input level select. 0: TTL input level. 1: Low input level. 0.9V for high and 0.6V for low.
2	GPIO27_EN	R/W	0	SUS_WARN#/GPIO27 function select. 0: The pin function is SUS_WARN#. 1: The pin function is GPIO27.
1	GPIO26_EN	R/W	0	SLP_SUS#/GPIO26 function select. 0: The pin function is SLP_SUS#. 1: The pin function is GPIO26.

0	GPIO25_EN	R/W	0	CIRRX#/GPIO25 function select. 0: The pin function is CIRRX#. 1: The pin function is GPIO25.

8.1.12 Multi Function Select 1 Register — Index 2Ah (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7-6	GPIO06_SEL	R/W	2'b11	SUSC#/GPIO06/BEEP/ALERT# function select. 00: The pin function is ALERT#. 01: The pin function is BEEP. 10: The pin function is GPIO06. 11: The pin function is SUSC#.
5	GPIO05_EN	R/W	1	GPIO05/LED_VCC function select. 0: The pin function is LED_VCC. 1: The pin function is GPIO05. This bit is powered by VBAT.
4	GPIO04_EN	R/W	1	GPIO04/LED_VSB function select. 0: The pin function is LED_VSB. 1: The pin function is GPIO04. This bit is powered by VBAT.
3	GPIO03_SEL	R/W	0	SLOTOCC#/GPIO03 function select. 0: The pin function is SLOTOCC#. 1: The pin function is GPIO03.
2	GPIO02_EN	R/W	0	DPWROK/GPIO02 function select. 0: The pin function is DPWROK. 1: The pin function is GPIO02.
1	GPIO01_EN	R/W	0	SUS_ACK#/GPIO01 function select. 0: The pin function is SUS_ACK#. 1: The pin function is GPIO01.
0	GPIO00_EN	R/W	0	ERP_CTRL2#/GPIO00 function select. 0: The pin function is ERP_CTRL2#. 1: The pin function is GPIO00.

8.1.13 Multi Function Select 2 Register — Index 2Bh (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7-6	GPIO13_SEL	R/W	00b	IRTX/GPIO13 function select. 00: Reserved. 01: The pin function is IRTX. 10: Reserved. 11: The pin function is GPIO13

5-4	GPIO12_SEL	R/W	11b	GPIO12/WDTRST# function select. 00: The pin function is WDTRST#. 01: reserved. 10: The pin function is GPIO12. 11: The pin function is CIRLED.
3-2	GPIO11_SEL	R/W	00b	FANCTRL3/GPIO11/IRTX1 function select. 00: The pin function is FANCTRL3. 01: The pin function is IRTX1. 10: Reserved. 11: The pin function is GPIO11.
1-0	GPIO10_SEL	R/W	00b	FANIN3/GPIO10/IRRX1 function select. 00: The pin function is FANIN3. 01: The pin function is IRRX1. 10: Reserved. 11: The pin function is GPIO10.

8.1.14 Multi Function Select 3 Register — Index 2Ch (Powered by VSB3V)

Bit	Name	R/W	Default	Description
7	GPIO1_2_RST_SEL	R/W	0	0: Reset by internal VSB5V power good. 1: Reset by LRESET#
6	UR2_GP_EN2	R/W	0	0: Pin2~4 and pin126~128 function as UART2 modem control. 1: Pin2~4 and pin126~128 function as GPIO3x.
5	UR2_GP_EN1	R/W	0	0: Pin5, 6 function as UART2 SOUT2/SIN2. 1: Pin5, 6 function as GPIO3x.
4	FDC_GP_EN	R/W	0	0: Reserved. 1: Pin 7 ~19 function as GPIOs.
3	GPIO16_SEL	R/W	0	PECI/TSI_DAT/IBX_SDA/GPIO16 function select. 0: The pin function is PECI/TSI_DAT/IBX_SDA decided by INTEL_MODEL register. 1: The pin function is GPIO16.
2	GPIO15_SEL	R/W	0	SST/TSI_CLK/IBX_CLK/GPIO15 function select. 0: The pin function is SST/TSI_CLK/IBX_CLK decided by INTEL_MODEL register. 1: The pin function is GPIO15.
1-0	GPIO14_SEL	R/W	00b	IRRX/GPIO14 function select. 00: Reserved. 01: The pin function is IRRX. 10: Reserved. 11: The pin function is GPIO14.

8.1.15 Wakeup Control Register — Index 2Dh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	SLOT_PWR_SEL	R/W	0	0: SLOTOCC# is pull-up to VSB3V. 1: SLOTOCC# is pull-up to VBAT.

6	VSBOK_HYS_DIS	R/W	0	0: RSMRST# will sink low when VSB3V is below 2.5V. 1: RSMRST# will sink low when VSB3V is below 2.8V. VSB3V power good level is 2.8V.
5	VREF_S3	R/W	0	1: VREF2 and 3 keep power on in S3 state 0: VREF2 and 3 are power down in S3 state
4	KEY_SEL_ADD	R/W	0	This bit is added to add more wakeup key function.
3	WAKEUP_EN	R/W	1	0: disable keyboard/mouse wake up. 1: enable keyboard/mouse wake up.
2-1	KEY_SEL	R/W	00	This registers select the keyboard wake up key. Accompanying with KEY_SEL_ADD, there are eight wakeup keys:
0	MO_SEL	R/W	0	This register selects the mouse wake up key. 0: Wake up by clicking. 1: Wake up by clicking and movement.

KEY_SEL_ADD	KEY_SEL	Wakeup Key
0	00	Ctrl + Esc
0	01	Ctrl + F1
0	10	Ctrl + Space
0	11	Any Key
1	00	Windows Wakeup
1	01	Windows Power
1	10	Ctrl + Alt + Space
1	11	Space

8.2 UART1 Registers (CR01)

UART 1 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR1_EN	R/W	1	0: disable UART 1. 1: enable UART 1.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of UART 1 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 1 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR1IRQ	R/W	4h	Select the IRQ channel for UART 1.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.

5	RS485_INV	R/W	0	0: Normal RS485 mode. 1: RTS# is inverted in RS485 mode.
4	RS485_EN	R/W	0	RS485 Mode Enable. 0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.
3-0	Reserved	-	-	Reserved.

8.3 UART 2 Registers (CR02)

UART 2 Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	UR2_EN	R/W	1	0: disable UART 2. 1: enable UART 2.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of UART 2 base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	F8h	The LSB of UART 2 base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELUR2IRQ	R/W	3h	Select the IRQ channel for UART 2.

RS485 Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7-6	Reserved	-	-	Reserved.
5	RS485_INV	R/W	0	0: Normal RS485 mode. 1: RTS# is inverted in RS485 mode.
4	RS485_EN	R/W	0	0: RS232 driver. 1: RS485 driver. Auto drive RTS# high when transmitting data, otherwise is kept low.
3	RXW4C_IR	R/W	0	0: No reception delay when SIR is changed form TX to RX. 1: Reception delays 4 characters time when SIR is changed form TX to RX.
2	TXW4C_IR	R/W	0	0: No transmission delay when SIR is changed form RX to TX. 1: Transmission delays 4 characters time when SIR is changed form RX to TX.
1-0	Reserved	-	-	Reserved.

SIR Mode Control Register — Index F1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.

4-3	IRMODE	R/W	00	00: disable IR function. 01: disable IR function. 10: IrDA function, active pulse is 1.6uS. 11: IrDA function, active pulse is 3/16 bit time.
2	HDUPLX	R/W	1	0: SIR is in full duplex mode for loopbak test. TXW4C_IR and RXW4C_IR are of no use. 1: SIR is in half duplex mode.
1	TXINV_IR	R/W	0	0: IRTX1 is in normal condition. 1: inverse the IRTX1.
0	RXINV_IR	R/W	0	0: IRRX1is in normal condition. 1: inverse the IRRX1.

8.4 Parallel Port Registers (CR03)

Parallel Port Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PRT_EN	R/W	1	0: disable Parallel Port. 1: enable Parallel Port.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	03h	The MSB of Parallel Port base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	78h	The LSB of Parallel Port base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
3-0	SELPRTIRQ	R/W	7h	Select the IRQ channel for Parallel Port.

DMA Channel Select Register — Index 74h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	ECP_DMA_MODE	R/W	0	0: non-burst mode DMA. 1: enable burst mode DMA.
3	Reserved	-	-	Reserved.
2-0	SELPRTDMA	R/W	011	Select the DMA channel for Parallel Port.

PRT Mode Select Register — Index F0h

Bit	Name	R/W	Default	Description
7	SPP_IRQ_MODE	R/W	0	Interrupt mode in non-ECP mode. 0: Level mode. 1: Pulse mode.
6-3	ECP_FIFO_THR	R/W	1000	ECP FIFO threshold.

2-0	PRT_MODE	R/W	010	000: Standard and Bi-direction (SPP) mode. 001: EPP 1.9 and SPP mode. 010: ECP mode (default). 011: ECP and EPP 1.9 mode. 100: Printer mode. 101: EPP 1.7 and SPP mode. 110: Reserved. 111: ECP and EPP1.7 mode.

8.5 Hardware Monitor Registers (CR04)

8.6.1 Hardware Monitor Configuration Registers

Hardware Monitor Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	HM_EN	R/W	1	0: disable Hardware Monitor. 1: enable Hardware Monitor.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	02h	The MSB of Hardware Monitor base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	95h	The LSB of Hardware Monitor base address.

IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELHMIRQ	R/W	0000	Select the IRQ channel for Hardware Monitor.

8.6 KBC Registers (CR05)

KBC Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	KBC_EN	R/W	1	0: disable KBC. 1: enable KBC.

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of KBC command port address. The address of data port is command port address + 4.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	60h	The LSB of KBC command port address. The address of data port is command port address + 4.

KB IRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELKIRQ	R/W	1h	Select the IRQ channel for keyboard interrupt.

Mouse IRQ Channel Select Register — Index 72h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELMIRQ	R/W	Ch	Select the IRQ channel for PS/2 mouse interrupt.

Auto Swap Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	AUTO_DET_EN	R/W	1b	0: disable auto detect keyboard/mouse swap. 1: enable auto detect keyboard/mouse swap.
6-5	Reserved	-	-	Reserved.
4	KB_MO_SWAP	R/W	0b	0: Keyboard/mouse does not swap. 1: Keyboard/mouse swaps. This bit is set/clear by hardware if AUTO_DET_EN is set to “1”. Users could also program this bit manually.
3	PSEUDO_8408_EN	R/W	0	Set “1” to enable auto response to KBC command. It will return to 0xFA, 0xAA for 0xFF command and 0xFA for other commands. This bit is used for GPIO scan code function without PS/2 keyboard.
2-0	Reserved	R/W	1h	Reserved

User Wakeup Code Register — Index FFh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7-0	USER_WAKEUP_CODE	R/W	29h	This is the user defined code for wakeup function.

8.7 GPIO Registers (CR06) (All registers of GPIO are powered by VSB3V)

GPIO0 Output Enable Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_OE	R/W	0	0: GPIO06 is in input mode. 1: GPIO06 is in output mode.
5	GPIO05_OE	R/W	0	0: GPIO05 is in input mode. 1: GPIO05 is in output mode.
4	GPIO04_OE	R/W	0	0: GPIO04 is in input mode. 1: GPIO04 is in output mode.
3	GPIO03_OE	R/W	0	0: GPIO03 is in input mode. 1: GPIO03 is in output mode.

2	GPIO02_OE	R/W	0	0: GPIO02 is in input mode. 1: GPIO02 is in output mode.
1	GPIO01_OE	R/W	0	0: GPIO01 is in input mode. 1: GPIO01 is in output mode.
0	GPIO00_OE	R/W	0	0: GPIO00 is in input mode. 1: GPIO00 is in output mode.

GPIO0 Output Data Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_VAL	R/W	1	0: GPIO06 outputs 0 when in output mode. 1: GPIO06 outputs1 when in output mode.
5	GPIO05_VAL	R/W	1	0: GPIO05 outputs 0 when in output mode. 1: GPIO05 outputs 1 when in output mode.
4	GPIO04_VAL	R/W	1	0: GPIO04 outputs 0 when in output mode. 1: GPIO04 outputs 1 when in output mode.
3	GPIO03_VAL	R/W	1	0: GPIO03 outputs 0 when in output mode. 1: GPIO03 outputs 1 when in output mode.
2	GPIO02_VAL	R/W	1	0: GPIO02 outputs 0 when in output mode. 1: GPIO02 outputs 1 when in output mode.
1	GPIO01_VAL	R/W	1	0: GPIO01 outputs 0 when in output mode. 1: GPIO01 outputs 1 when in output mode.
0	GPIO00_VAL	R/W	1	0: GPIO00 outputs 0 when in output mode. 1: GPIO00 outputs 1 when in output mode.

GPIO0 Pin Status Register — Index F2h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_IN	R	-	The pin status of SUSC#/GPIO06/Beep/Alert#.
5	GPIO05_IN	R	-	The pin status of GPIO05/LED_VCC.
4	GPIO04_IN	R	-	The pin status of GPIO04/LED_VSB.
3	GPIO03_IN	R	-	The pin status of SLOTCC#/GPIO03.
2	GPIO02_IN	R	-	The pin status of DPWROK/GPIO02.
1	GPIO01_IN	R	-	The pin status of SUS_ACK#/GPIO01.
0	GPIO00_IN	R	-	The pin status of ERP_CTRL2#/GPIO00.

GPIO0 Drive Enable Register — Index F3h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO06_DRV_EN	R/W	0	0: GPIO06 is open drain in output mode. 1: GPIO06 is push pull in output mode.
5	GPIO05_DRV_EN*	R/W	0	0: GPIO05 is open drain in output mode. 1: GPIO05 is push pull in output mode. This bit is powered by VBAT.

4	GPIO04_DRV_EN*	R/W	0	0: GPIO04 is open drain in output mode. 1: GPIO04 is push pull in output mode. This bit is powered by VBAT.
3	GPIO03_DRV_EN	R/W	0	0: GPIO03 is open drain in output mode. 1: Reserved.
2	GPIO02_DRV_EN	R/W	0	0: GPIO02 is open drain in output mode. 1: GPIO02 is push pull in output mode.
1	GPIO01_DRV_EN	R/W	0	0: GPIO01 is open drain in output mode. 1: GPIO01 is push pull in output mode.
0	GPIO00_DRV_EN	R/W	0	0: GPIO00 is open drain in output mode. 1: GPIO00 is push pull in output mode.

LED_VSB Control Register — Index FEh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	LED_VSB_DS3	R/W	0	Set this bit “1” to enable LED_VSB deep S3 mode. LED_VSB will output 0.25Hz clock with 25% duty in deep S3 state.
5-4	LED_VSB_S5_MODE	R/W	0	These bits control the LED_VSB output mode in S5 state. The LED_VSB output is controlled by {LED_VSB_S5_ADD, LED_VSB_S5_MODE} 000: Sink 0 001: Tri-state. 010: 0.5Hz clock 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty. 111: 0.25Hz clock with 25% duty.
3-2	LED_VSB_S3_MODE	R/W	0	These bits control the LED_VSB output mode in S3 state. The LED_VSB output is controlled by {LED_VSB_S3_ADD, LED_VSB_S3_MODE} 000: Sink 0 001: Tri-state. 010: 0.5Hz clock 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty. 111: 0.25Hz clock with 25% duty.

1-0	LED_VSB_S0_MODE	R/W	0	These bits control the LED_VSB output mode in S0 state. The LED_VSB output is controlled by {LED_VSB_S0_ADD, LED_VSB_S0_MODE} 000: Sink 0 001: Tri-state. 010: 0.5Hz clock 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty. 111: 0.25Hz clock with 25% duty.

LED_VCC Control Register — Index FFh (Powered by VBAT)

Bit	Name	R/W	Default	Description
7	LED_VCC_INV_DIS	R/W	0	0: LED_VCC output clock is inverted. 1: LED_VCC output clock is not inverted.
6	LED_VCC_DS3	R/W	0	Set this bit “1” to enable LED_VCC deep S3 mode. LED_VCC will output 0.25Hz clock with 25% duty in deep S3 state.
5-4	LED_VCC_S5_MODE	R/W	0	These bits control the LED_VCC output mode in S5 state. The LED_VCC output is controlled by {LED_VCC_S5_ADD, LED_VCC_S5_MODE} 000: Sink 0 001: Tri-state. 010: 0.5Hz clock 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty. 111: 0.25Hz clock with 25% duty.
3-2	LED_VCC_S3_MODE	R/W	0	These bits control the LED_VCC output mode in S3 state. The LED_VCC output is controlled by {LED_VCC_S3_ADD, LED_VCC_S3_MODE} 000: Sink 0 001: Tri-state. 010: 0.5Hz clock 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty. 111: 0.25Hz clock with 25% duty.

1-0	LED_VCC_S0_MODE	R/W	0	These bits control the LED_VCC output mode in S0 state. The LED_VCC output is controlled by {LED_VCC_S0_ADD, LED_VCC_S0_MODE} 000: Sink 0 001: Tri-state. 010: 0.5Hz clock 011: 1Hz clock. 100: 0.125Hz clock with 50% duty. 101: 0.25Hz clock with 50% duty. 110: 0.125Hz clock with 25% duty. 111: 0.25Hz clock with 25% duty.

GPIO1 Output Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_OE	R/W	0	0: GPIO16 is in input mode. 1: GPIO16 is in output mode.
5	GPIO15_OE	R/W	0	0: GPIO15 is in input mode. 1: GPIO15 is in output mode.
4	GPIO14_OE	R/W	0	0: GPIO14 is in input mode. 1: GPIO14 is in output mode.
3	GPIO13_OE	R/W	0	0: GPIO13 is in input mode. 1: GPIO13 is in output mode.
2	GPIO12_OE	R/W	0	0: GPIO12 is in input mode. 1: GPIO12 is in output mode.
1	GPIO11_OE	R/W	0	0: GPIO11 is in input mode. 1: GPIO11 is in output mode.
0	GPIO10_OE	R/W	0	0: GPIO10 is in input mode. 1: GPIO10 is in output mode.

GPIO1 Output Data Register — Index E1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_VAL	R/W	1	0: GPIO16 outputs 0 when in output mode. 1: GPIO16 outputs1 when in output mode.
5	GPIO15_VAL	R/W	1	0: GPIO15 outputs 0 when in output mode. 1: GPIO15 outputs 1 when in output mode.
4	GPIO14_VAL	R/W	1	0: GPIO14 outputs 0 when in output mode. 1: GPIO14 outputs 1 when in output mode.
3	GPIO13_VAL	R/W	1	0: GPIO13 outputs 0 when in output mode. 1: GPIO13 outputs 1 when in output mode.
2	GPIO12_VAL	R/W	1	0: GPIO12 outputs 0 when in output mode. 1: GPIO12 outputs 1 when in output mode.
1	GPIO11_VAL	R/W	1	0: GPIO11 outputs 0 when in output mode. 1: GPIO11 outputs 1 when in output mode.
0	GPIO10_VAL	R/W	1	0: GPIO10 outputs 0 when in output mode. 1: GPIO10 outputs 1 when in output mode.

GPIO1 Pin Status Register — Index E2h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_IN	R	-	The pin status of PECI/TSI_DAT/IBX_SDA/GPIO16
5	GPIO15_IN	R	-	The pin status of SST/TSI_CLK/IBX_CLK/GPIO15.
4	GPIO14_IN	R	-	The pin status of CIRWB#/TSI_DAT/IBX_SDA/GPIO14.
3	GPIO13_IN	R	-	The pin status of CIRTX/TSI_CLK/IBX_CLK/GPIO13.
2	GPIO12_IN	R	-	The pin status of CIR_LED#GPIO12/WDTRST#
1	GPIO11_IN	R	-	The pin status of FANCTL3/GPIO11/IRTX1.
0	GPIO10_IN	R	-	The pin status of FANIN3/GPIO10/IRRX1.

GPIO1 Drive Enable Register — Index E3h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved.
6	GPIO16_DRV_EN	R/W	0	0: GPIO16 is open drain in output mode. 1: GPIO16 is push pull in output mode.
5	GPIO15_DRV_EN	R/W	0	0: GPIO15 is open drain in output mode. 1: GPIO15 is push pull in output mode.
4	GPIO14_DRV_EN	R/W	0	0: GPIO14 is open drain in output mode. 1: GPIO14 is push pull in output mode.
3	GPIO13_DRV_EN	R/W	0	0: GPIO13 is open drain in output mode. 1: GPIO13 is push pull in output mode.
2	GPIO12_DRV_EN	R/W	0	0: GPIO12 is open drain in output mode. 1: GPIO12 is push pull in output mode.
1	GPIO11_DRV_EN	R/W	0	0: GPIO11 is open drain in output mode. 1: GPIO11 is push pull in output mode.
0	GPIO10_DRV_EN	R/W	0	0: GPIO10 is open drain in output mode. 1: GPIO10 is push pull in output mode.

GPIO2 Output Enable Register — Index D0h

Bit	Name	R/W	Default	Description
7	GPIO27_OE	R/W	0	0: GPIO27 is in input mode. 1: GPIO27 is in output mode.
6	GPIO26_OE	R/W	0	0: GPIO26 is in input mode. 1: GPIO25 is in output mode.
5	GPIO25_OE	R/W	0	0: GPIO25 is in input mode. 1: GPIO25 is in output mode.
4-0	Reserved	-	-	Reserved.

GPIO2 Output Data Register — Index D1h

Bit	Name	R/W	Default	Description
7	GPIO27_VAL	R/W	1	0: GPIO27 outputs 0 when in output mode. 1: GPIO27 outputs 1 when in output mode.
6	GPIO26_VAL	R/W	1	0: GPIO26 outputs 0 when in output mode. 1: GPIO26 outputs 1 when in output mode.

5	GPIO25_VAL	R/W	1	0: GPIO25 outputs 0 when in output mode. 1: GPIO25 outputs 1 when in output mode.
4-0	Reserved	-	-	Reserved.

GPIO2 Pin Status Register — Index D2h

Bit	Name	R/W	Default	Description
7	GPIO27_IN	R	-	The pin status of SUS_WARN#/GPIO27.
6	GPIO26_IN	R	-	The pin status of SLP_SUS#/GPIO26.
5	GPIO25_IN	R	-	The pin status of CIRRX#/GPIO25.
4-0	Reserved	-	-	Reserved.

GPIO2 Drive Enable Register — Index D3h

Bit	Name	R/W	Default	Description
7	GPIO27_DRV_EN	R/W	0	0: GPIO27 is open drain in output mode. 1: GPIO27 is push pull in output mode.
6	GPIO26_DRV_EN	R/W	0	0: GPIO26 is open drain in output mode. 1: GPIO26 is push pull in output mode.
5	GPIO25_DRV_EN	R/W	0	0: GPIO25 is open drain in output mode. 1: GPIO25 is push pull in output mode.
4-0	Reserved	-	-	Reserved.

GPIO3 Output Enable Register — Index C0h

Bit	Name	R/W	Default	Description
7	GPIO37_OE	R/W	0	0: GPIO37 is in input mode. 1: GPIO37 is in output mode.
6	GPIO36_OE	R/W	0	0: GPIO36 is in input mode. 1: GPIO35 is in output mode.
5	GPIO35_OE	R/W	0	0: GPIO35 is in input mode. 1: GPIO35 is in output mode.
4	GPIO34_OE	R/W	0	0: GPIO34 is in input mode. 1: GPIO34 is in output mode.
3	GPIO33_OE	R/W	0	0: GPIO33 is in input mode. 1: GPIO33 is in output mode.
2	GPIO32_OE	R/W	0	0: GPIO32 is in input mode. 1: GPIO32 is in output mode.
1	GPIO31_OE	R/W	0	0: GPIO31 is in input mode. 1: GPIO31 is in output mode.
0	GPIO30_OE	R/W	0	0: GPIO30 is in input mode. 1: GPIO30 is in output mode.

GPIO3 Output Data Register — Index C1h

Bit	Name	R/W	Default	Description
7	GPIO37_VAL	R/W	1	0: GPIO37 outputs 0 when in output mode. 1: GPIO37 outputs 1 when in output mode.

6	GPIO36_VAL	R/W	1	0: GPIO36 outputs 0 when in output mode. 1: GPIO36 outputs 1 when in output mode.
5	GPIO35_VAL	R/W	1	0: GPIO35 outputs 0 when in output mode. 1: GPIO35 outputs 1 when in output mode.
4	GPIO34_VAL	R/W	1	0: GPIO34 outputs 0 when in output mode. 1: GPIO34 outputs 1 when in output mode.
3	GPIO33_VAL	R/W	1	0: GPIO33 outputs 0 when in output mode. 1: GPIO33 outputs 1 when in output mode.
2	GPIO32_VAL	R/W	1	0: GPIO32 outputs 0 when in output mode. 1: GPIO32 outputs 1 when in output mode.
1	GPIO31_VAL	R/W	1	0: GPIO31 outputs 0 when in output mode. 1: GPIO31 outputs 1 when in output mode.
0	GPIO30_VAL	R/W	1	0: GPIO30 outputs 0 when in output mode. 1: GPIO30 outputs 1 when in output mode.

GPIO3 Pin Status Register — Index C2h

Bit	Name	R/W	Default	Description
7	GPIO37_IN	R	-	The pin status of SIN2/SEGE/GPIO37.
6	GPIO36_IN	R	-	The pin status of SOUT2/SEGB/GPIO36/ OVP_STRAP.
5	GPIO35_IN	R	-	The pin status of DSR2#/L#/GPIO35.
4	GPIO34_IN	R	-	The pin status of RTS2#/SEGC/GPIO34/PWM_DC.
3	GPIO33_IN	R	-	The pin status of DTR2#/SEGD/GPIO33.
2	GPIO32_IN	R	-	The pin status of CTS2#/SEGA/GPIO32.
1	GPIO31_IN	R	-	The pin status of RI2#/GPIO31.
0	GPIO30_IN	R	-	The pin status of DCD2#/GPIO30.

GPIO3 Drive Enable Register — Index C3h

Bit	Name	R/W	Default	Description
7	GPIO37_DRV_EN	R/W	0	0: GPIO37 is open drain in output mode. 1: GPIO37 is push pull in output mode.
6	GPIO36_DRV_EN	R/W	0	0: GPIO36 is open drain in output mode. 1: GPIO36 is push pull in output mode.
5	GPIO35_DRV_EN	R/W	0	0: GPIO35 is open drain in output mode. 1: GPIO35 is push pull in output mode.
4	GPIO34_DRV_EN	R/W	0	0: GPIO34 is open drain in output mode. 1: GPIO34 is push pull in output mode.
3	GPIO33_DRV_EN	R/W	0	0: GPIO33 is open drain in output mode. 1: GPIO33 is push pull in output mode.
2	GPIO32_DRV_EN	R/W	0	0: GPIO32 is open drain in output mode. 1: GPIO32 is push pull in output mode.
1	GPIO31_DRV_EN	R/W	0	0: GPIO31 is open drain in output mode. 1: GPIO31 is push pull in output mode.
0	GPIO30_DRV_EN	R/W	0	0: GPIO30 is open drain in output mode. 1: GPIO30 is push pull in output mode.

GPIO4 Output Enable Register — Index B0h

Bit	Name	R/W	Default	Description
7	GPIO47_OE	R/W	0	0: GPIO47 is in input mode. 1: GPIO47 is in output mode.
6	GPIO46_OE	R/W	0	0: GPIO46 is in input mode. 1: GPIO45 is in output mode.
5	GPIO45_OE	R/W	0	0: GPIO45 is in input mode. 1: GPIO45 is in output mode.
4	GPIO44_OE	R/W	0	0: GPIO44 is in input mode. 1: GPIO44 is in output mode.
3	GPIO43_OE	R/W	0	0: GPIO43 is in input mode. 1: GPIO43 is in output mode.
2	GPIO42_OE	R/W	0	0: GPIO42 is in input mode. 1: GPIO42 is in output mode.
1	GPIO41_OE	R/W	0	0: GPIO41 is in input mode. 1: GPIO41 is in output mode.
0	GPIO40_OE	R/W	0	0: GPIO40 is in input mode. 1: GPIO40 is in output mode.

GPIO4 Output Data Register — Index B1h

Bit	Name	R/W	Default	Description
7	GPIO47_VAL	R/W	1	0: GPIO47 outputs 0 when in output mode. 1: GPIO47 outputs Tri-state when in output mode.
6	GPIO46_VAL	R/W	1	0: GPIO46 outputs 0 when in output mode. 1: GPIO46 outputs Tri-state when in output mode.
5	GPIO45_VAL	R/W	1	0: GPIO45 outputs 0 when in output mode. 1: GPIO45 outputs Tri-state when in output mode.
4	GPIO44_VAL	R/W	1	0: GPIO44 outputs 0 when in output mode. 1: GPIO44 outputs Tri-state when in output mode.
3	GPIO43_VAL	R/W	1	0: GPIO43 outputs 0 when in output mode. 1: GPIO43 outputs Tri-state when in output mode.
2	GPIO42_VAL	R/W	1	0: GPIO42 outputs 0 when in output mode. 1: GPIO42 outputs Tri-state when in output mode.
1	GPIO41_VAL	R/W	1	0: GPIO41 outputs 0 when in output mode. 1: GPIO41 outputs Tri-state when in output mode.
0	GPIO40_VAL	R/W	1	0: GPIO40 outputs 0 when in output mode. 1: GPIO40 outputs Tri-state when in output mode.

GPIO4 Pin Status Register — Index B2h

Bit	Name	R/W	Default	Description
7	GPIO47_IN	R	-	The pin status of GPIO47.
6	GPIO46_IN	R	-	The pin status of GPIO46.
5	GPIO45_IN	R	-	The pin status of GPIO45.
4	GPIO44_IN	R	-	The pin status of GPIO44.

3	GPIO43_IN	R	-	The pin status of GPIO43.
2	GPIO42_IN	R	-	The pin status of GPIO42.
1	GPIO41_IN	R	-	The pin status of GPIO41.
0	GPIO40_IN	R	-	The pin status of GPIO40.

GPIO5 Output Enable Register — Index A0h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_OE	R/W	0	0: GPIO54 is in input mode. 1: GPIO54 is in output mode.
3	GPIO53_OE	R/W	0	0: GPIO53 is in input mode. 1: GPIO53 is in output mode.
2	GPIO52_OE	R/W	0	0: GPIO52 is in input mode. 1: GPIO52 is in output mode.
1	GPIO51_OE	R/W	0	0: GPIO51 is in input mode. 1: GPIO51 is in output mode.
0	GPIO50_OE	R/W	0	0: GPIO50 is in input mode. 1: GPIO50 is in output mode.

GPIO5 Output Data Register — Index A1h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_VAL	R/W	1	0: GPIO54 outputs 0 when in output mode. 1: GPIO54 outputs Tri-state when in output mode.
3	GPIO53_VAL	R/W	1	0: GPIO53 outputs 0 when in output mode. 1: GPIO53 outputs Tri-state when in output mode.
2	GPIO52_VAL	R/W	1	0: GPIO52 outputs 0 when in output mode. 1: GPIO52 outputs Tri-state when in output mode.
1	GPIO51_VAL	R/W	1	0: GPIO51 outputs 0 when in output mode. 1: GPIO51 outputs Tri-state when in output mode.
0	GPIO50_VAL	R/W	1	0: GPIO50 outputs 0 when in output mode. 1: GPIO50 outputs Tri-state when in output mode.

GPIO5 Pin Status Register — Index A2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved.
4	GPIO54_IN	R	-	The pin status of GPIO54.
3	GPIO53_IN	R	-	The pin status of GPIO53.
2	GPIO52_IN	R	-	The pin status of GPIO52.
1	GPIO51_IN	R	-	The pin status of GPIO51.
0	GPIO50_IN	R	-	The pin status of GPIO50.

GPIO5 PME Enable Register — Index A4h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	GPIO54_PME_EN	R/W	0	When GPIO54_EVENT_STS is 1 and GPIO54_PME_EN is set to 1, a GPIO PME event will be generated.
3	GPIO53_PME_EN	R/W	0	When GPIO53_EVENT_STS is 1 and GPIO53_PME_EN is set to 1, a GPIO PME event will be generated.
2	GPIO52_PME_EN	R/W	0	When GPIO52_EVENT_STS is 1 and GPIO52_PME_EN is set to 1, a GPIO PME event will be generated.
1	GPIO51_PME_EN	R/W	0	When GPIO51_EVENT_STS is 1 and GPIO51_PME_EN is set to 1, a GPIO PME event will be generated.
0	GPIO50_PME_EN	R/W	0	When GPIO50_EVENT_STS is 1 and GPIO50_PME_EN is set to 1, a GPIO PME event will be generated.

GPIO5 Input Detection Select Register — Index A5h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	GPIO54_DET_SEL	R/W	0	When GPIO54 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
3	GPIO53_DET_SEL	R/W	0	When GPIO53 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
2	GPIO52_DET_SEL	R/W	0	When GPIO52 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
1	GPIO51_DET_SEL	R/W	0	When GPIO51 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge
0	GPIO50_DET_SEL	R/W	0	When GPIO50 is in input mode, set this bit to select which input event should be detected. 0: rising edge 1: falling edge

GPIO5 Event Status Register — Index A6h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	GPIO54_ EVENT_STS	R/W	-	When GPIO54 is in input mode and a GPIO54 input is detected according to CRA5 [4], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
3	GPIO53_ EVENT_STS	R/W	-	When GPIO53 is in input mode and a GPIO53 input is detected according to CRA5 [3], this bit will be set to 1. Write a 1 to this bit will clear it to 0.

2	GPIO52_ EVENT_STS	R/W	-	When GPIO52 is in input mode and a GPIO52 input is detected according to CRB5 [2], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
1	GPIO51_ EVENT_STS	R/W	-	When GPIO51 is in input mode and a GPIO51 input is detected according to CRB5 [1], this bit will be set to 1. Write a 1 to this bit will clear it to 0.
0	GPIO50_ EVENT_STS	R/W	-	When GPIO50 is in input mode and a GPIO50 input is detected according to CRB5 [0], this bit will be set to 1. Write a 1 to this bit will clear it to 0.

GPIO52 KBC Emulation Make Code Register — Index ABh

Bit	Name	R/W	Default	Description
7-0	GP52_MAKE_CODE	R/W	0	This is the make code for GPIO52 KBC emulation. The break code will be GP52_MAKE_CODE + 0x80.

GPIO51 KBC Emulation Make Code Register — Index ACh

Bit	Name	R/W	Default	Description
7-0	GP51_MAKE_CODE	R/W	0	This is the make code for GPIO51 KBC emulation. The break code will be GP51_MAKE_CODE + 0x80.

GPIO50 KBC Emulation Make Code Register — Index ADh

Bit	Name	R/W	Default	Description
7-0	GP50_MAKE_CODE	R/W	0	This is the make code for GPIO50 KBC emulation. The break code will be GP50_MAKE_CODE + 0x80.

GPIO5 KBC Emulation Prefix Code Register — Index AEh

Bit	Name	R/W	Default	Description
7-0	GP_PRE_CODE	R/W	E0h	This is the prefix code for GPIO5 KBC emulation. When PRE_CODE_EN is set, prefix code followed by make/break code is sent when the event occurs.

GPIO5 KBC Emulation Control Register — Index AFh

Bit	Name	R/W	Default	Description
7	GP_KBC_EN	R/W	0	Set “1” to enable GPIO5 KBC emulation.
6	PRE_CODE_EN	R/W	0	0: Disable prefix code. Make/break code is sent when the event occurs. 1: Enable prefix code. Prefix code followed by make/break code is sent when the event occurs.
5	GP52_BRK_STE	R/WC	0	This bit is set when GPIO52 is released (rising edge) and auto cleared by host reading 0x60 port. It could be clear by writing “1”.
4	GP52_MAKE_STE	R/WC	0	This bit is set when GPIO52 is pressed (falling edge) and auto cleared by host reading 0x60 port. It could be clear by writing “1”. The status will continue to set when still pressing the GPIO52. The delay time is 0.5 ~ 1 sec and repeated time is 50ms.
5	GP51_BRK_STE	R/WC	0	This bit is set when GPIO51 is released (rising edge) and auto cleared by host reading 0x60 port. It could be clear by writing “1”.
5	GP51_MAKE_STE	R/WC	0	This bit is set when GPIO51 is pressed (falling edge) and auto cleared by host reading 0x60 port. It could be clear by writing “1”. The status will continue to set when still pressing the GPIO51. The delay time is 0.5 ~ 1 sec and repeated time is 50ms.
5	GP50_BRK_STE	R/WC	0	This bit is set when GPIO50 is released (rising edge) and auto cleared by host reading 0x60 port. It could be clear by writing “1”.

0	GP50_MAKE_STE	R/WC	0	This bit is set when GPIO50 is pressed (falling edge) and auto cleared by host reading 0x60 port. It could be clear by writing "1". The status will continue to set when still pressing the GPIO50 i. The delay time is 0.5 ~ 1 sec and repeated time is 50ms.

GPIO6 Output Enable Register — Index 90h

Bit	Name	R/W	Default	Description
7	GPIO67_OE	R/W	0	0: GPIO67 is in input mode. 1: GPIO67 is in output mode.
6	GPIO66_OE	R/W	0	0: GPIO66 is in input mode. 1: GPIO65 is in output mode.
5	GPIO65_OE	R/W	0	0: GPIO65 is in input mode. 1: GPIO65 is in output mode.
4	GPIO64_OE	R/W	0	0: GPIO64 is in input mode. 1: GPIO64 is in output mode.
3	GPIO63_OE	R/W	0	0: GPIO63 is in input mode. 1: GPIO63 is in output mode.
2	GPIO62_OE	R/W	0	0: GPIO62 is in input mode. 1: GPIO62 is in output mode.
1	GPIO61_OE	R/W	0	0: GPIO61 is in input mode. 1: GPIO61 is in output mode.
0	GPIO60_OE	R/W	0	0: GPIO60 is in input mode. 1: GPIO60 is in output mode.

GPIO6 Output Data Register — Index 91h

Bit	Name	R/W	Default	Description
7	GPIO67_VAL	R/W	1	0: GPIO67 outputs 0 when in output mode. 1: GPIO67 outputs 1 when in output mode.
6	GPIO66_VAL	R/W	1	0: GPIO66 outputs 0 when in output mode. 1: GPIO66 outputs 1 when in output mode.
5	GPIO65_VAL	R/W	1	0: GPIO65 outputs 0 when in output mode. 1: GPIO65 outputs 1 when in output mode.
4	GPIO64_VAL	R/W	1	0: GPIO64 outputs 0 when in output mode. 1: GPIO64 outputs 1 when in output mode.
3	GPIO63_VAL	R/W	1	0: GPIO63 outputs 0 when in output mode. 1: GPIO63 outputs 1 when in output mode.
2	GPIO62_VAL	R/W	1	0: GPIO62 outputs 0 when in output mode. 1: GPIO62 outputs 1 when in output mode.
1	GPIO61_VAL	R/W	1	0: GPIO61 outputs 0 when in output mode. 1: GPIO61 outputs 1 when in output mode.
0	GPIO60_VAL	R/W	1	0: GPIO60 outputs 0 when in output mode. 1: GPIO60 outputs 1 when in output mode.

GPIO6 Pin Status Register — Index 92h

Bit	Name	R/W	Default	Description
7	GPIO67_IN	R	-	The pin status of STB#/GPIO67.
6	GPIO66_IN	R	-	The pin status of AFD /GPIO66.
5	GPIO65_IN	R	-	The pin status of ERR#/ GPIO65.
4	GPIO64_IN	R	-	The pin status of INIT#/ GPIO64.
3	GPIO63_IN	R	-	The pin status of ACK#/GPIO63.
2	GPIO62_IN	R	-	The pin status of BUSY/GPIO62.
1	GPIO61_IN	R	-	The pin status of PE/GPIO61.
0	GPIO60_IN	R	-	The pin status of SLCT/GPIO60.

GPIO6 Drive Enable Register — Index 93h

Bit	Name	R/W	Default	Description
7	GPIO67_DRV_EN	R/W	0	0: GPIO67 is open drain in output mode. 1: GPIO67 is push pull in output mode.
6	GPIO66_DRV_EN	R/W	0	0: GPIO66 is open drain in output mode. 1: GPIO66 is push pull in output mode.
5	GPIO65_DRV_EN	R/W	0	0: GPIO65 is open drain in output mode. 1: GPIO65 is push pull in output mode.
4	GPIO64_DRV_EN	R/W	0	0: GPIO64 is open drain in output mode. 1: GPIO64 is push pull in output mode.
3	GPIO63_DRV_EN	R/W	0	0: GPIO63 is open drain in output mode. 1: GPIO63 is push pull in output mode.
2	GPIO62_DRV_EN	R/W	0	0: GPIO62 is open drain in output mode. 1: GPIO62 is push pull in output mode.
1	GPIO61_DRV_EN	R/W	0	0: GPIO61 is open drain in output mode. 1: GPIO61 is push pull in output mode.
0	GPIO60_DRV_EN	R/W	0	0: GPIO60 is open drain in output mode. 1: GPIO60 is push pull in output mode.

GPIO7 Output Enable Register — Index 80h

Bit	Name	R/W	Default	Description
7	GPIO77_OE	R/W	0	0: GPIO77 is in input mode. 1: GPIO77 is in output mode.
6	GPIO76_OE	R/W	0	0: GPIO76 is in input mode. 1: GPIO75 is in output mode.
5	GPIO75_OE	R/W	0	0: GPIO75 is in input mode. 1: GPIO75 is in output mode.
4	GPIO74_OE	R/W	0	0: GPIO74 is in input mode. 1: GPIO74 is in output mode.
3	GPIO73_OE	R/W	0	0: GPIO73 is in input mode. 1: GPIO73 is in output mode.
2	GPIO72_OE	R/W	0	0: GPIO72 is in input mode. 1: GPIO72 is in output mode.

1	GPIO71_OE	R/W	0	0: GPIO71 is in input mode. 1: GPIO71 is in output mode.
0	GPIO70_OE	R/W	0	0: GPIO70 is in input mode. 1: GPIO70 is in output mode.

GPIO7 Output Data Register — Index 81h

Bit	Name	R/W	Default	Description
7	GPIO77_VAL	R/W	1	0: GPIO77 outputs 0 when in output mode. 1: GPIO77 outputs 1 when in output mode.
6	GPIO76_VAL	R/W	1	0: GPIO76 outputs 0 when in output mode. 1: GPIO76 outputs 1 when in output mode.
5	GPIO75_VAL	R/W	1	0: GPIO75 outputs 0 when in output mode. 1: GPIO75 outputs 1 when in output mode.
4	GPIO74_VAL	R/W	1	0: GPIO74 outputs 0 when in output mode. 1: GPIO74 outputs 1 when in output mode.
3	GPIO73_VAL	R/W	1	0: GPIO73 outputs 0 when in output mode. 1: GPIO73 outputs 1 when in output mode.
2	GPIO72_VAL	R/W	1	0: GPIO72 outputs 0 when in output mode. 1: GPIO72 outputs 1 when in output mode.
1	GPIO71_VAL	R/W	1	0: GPIO71 outputs 0 when in output mode. 1: GPIO71 outputs 1 when in output mode.
0	GPIO70_VAL	R/W	1	0: GPIO70 outputs 0 when in output mode. 1: GPIO70 outputs 1 when in output mode.

GPIO7 Pin Status Register — Index 82h

Bit	Name	R/W	Default	Description
7	GPIO77_IN	R	-	The pin status of PD7/GPIO77.
6	GPIO76_IN	R	-	The pin status of PD6/GPIO76.
5	GPIO75_IN	R	-	The pin status of PD5/ GPIO75.
4	GPIO74_IN	R	-	The pin status of PD4/GPIO74.
3	GPIO73_IN	R	-	The pin status of PD3/GPIO73.
2	GPIO72_IN	R	-	The pin status of PD2/GPIO72.
1	GPIO71_IN	R	-	The pin status of PD1/GPIO71.
0	GPIO70_IN	R	-	The pin status of PD0/GPIO70.

GPIO7 Drive Enable Register — Index 83h

Bit	Name	R/W	Default	Description
7	GPIO77_DRV_EN	R/W	0	0: GPIO77 is open drain in output mode. 1: GPIO77 is push pull in output mode.
6	GPIO76_DRV_EN	R/W	0	0: GPIO76 is open drain in output mode. 1: GPIO76 is push pull in output mode.
5	GPIO75_DRV_EN	R/W	0	0: GPIO75 is open drain in output mode. 1: GPIO75 is push pull in output mode.
4	GPIO74_DRV_EN	R/W	0	0: GPIO74 is open drain in output mode. 1: GPIO74 is push pull in output mode.

3	GPIO73_DRV_EN	R/W	0	0: GPIO73 is open drain in output mode. 1: GPIO73 is push pull in output mode.
2	GPIO72_DRV_EN	R/W	0	0: GPIO72 is open drain in output mode. 1: GPIO72 is push pull in output mode.
1	GPIO71_DRV_EN	R/W	0	0: GPIO71 is open drain in output mode. 1: GPIO71 is push pull in output mode.
0	GPIO70_DRV_EN	R/W	0	0: GPIO70 is open drain in output mode. 1: GPIO70 is push pull in output mode.

8.8 Watch Dog Timer Registers (CR07)

Watchdog Timer Configuration Register — Index F0h (* cleared by SLOTOCC_N and watch dog timeout)

Bit	Name	R/W	Default	Description
7	WDOUT_EN	R/W	0	If this bit is set to 1 and watchdog timeout event occurs, WDTRST# output is enabled.
6-1	Reserved	-	0	Reserved
0	WD_RST_EN	R/W	0	0: Disable WDT. 1: Enable WDT to reset the VID register marked with *.

Watchdog Timer Configuration Register 1— Index F5h

Bit	Name	R/W	Default	Description
7	Reserved	R	0	Reserved
6	WDTMOUT_STS	R/W	0	If watchdog timeout event occurs, this bit will be set to 1. Write a 1 to this bit will clear it to 0.
5	WD_EN	R/W	0	If this bit is set to 1, the counting of watchdog time is enabled.
4	WD_PULSE	R/W	0	Select output mode (0: level, 1: pulse) of RSTOUT# by setting this bit.
3	WD_UNIT	R/W	0	Select time unit (0: 1sec, 1: 60 sec) of watchdog timer by setting this bit.
2	WD_HACTIVE	R/W	0	Select output polarity of RSTOUT# (1: high active, 0: low active) by setting this bit.
1:0	WD_PSWIDTH	R/W	0	Select output pulse width of RSTOUT# 0: 1 ms 1: 25 ms 2: 125 ms 3: 5 sec

Watchdog Timer Configuration Register 2 — Index F6h

Bit	Name	R/W	Default	Description
7:0	WD_TIME	R/W	0	Time of watchdog timer

WDT PME Register — Index FAh

Bit	Name	R/W	Default	Description
7	WDT_PME	R	0	0: No WDT PME occurred. 1: WDT PME occurred. The WDT PME is occurred one unit before WDT timeout.
6	WDT_PME_EN	R/W	0	0: Disable WDT PME. 1: Enable WDT PME.
5-1	Reserved	R	0	Reserved
0	CPU_CHANGE	R/W	0	This bit will be set at SLOTOCC# rise edge. Internal 1us de-bounce circuit is implemented. Write “1” to this bit will clear the status.

*Those register are reset by SLOTOCC# falling edge (CPU change) or Watchdog timer timeout (if enabled).

8.9 CIR Registers (CR08)

Configuration Registers

CIR Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	CIR_EN	R/W	0	0: disable CIR 1: enable CIR

Base Address High Register — Index 60h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_HI	R/W	00h	The MSB of CIR base address.

Base Address Low Register — Index 61h

Bit	Name	R/W	Default	Description
7-0	BASE_ADDR_LO	R/W	00h	The LSB of CIR base address.

CIRIRQ Channel Select Register — Index 70h

Bit	Name	R/W	Default	Description
7-4	Reserved	-	-	Reserved.
3-0	SELCIRIRQ	R/W	0h	Select the IRQ channel for CIR interrupt.

Device Register

CIR Status Register — Index 00h

Bit	Name	R/W	Default	Description
7	CIR_IRQ_EN	R/W	0	CIR IRQ function enable
6-4	Reserved	R	0	Reserved
3	TX_FINISH	R/W	0	CIR transmittion finish status. Write 1 clear.
2	TX_UNDERRUN	R/W	0	CIR transmitttion underrun status. Write 1 clear.
1	RX_TIMEOUT	R/W	0	CIR receiver timeout status. Write 1 clear.
0	RX_RECEIVE	R/W	0	CIR receiver receives data status. Write 1 clear.

CIR RX Data Register — Index 01h

Bit	Name	R/W	Default	Description
7-0	RX_DATA	R	-	CIR received data is read from here.

CIR TX Control Register — Index 02h

Bit	Name	R/W	Default	Description
7	TX_START	R/W	0	Set 1 to start CIR TX transmittion and will be auto cleared if transmittion is finished.
6	TX_END	R/W	0	Set 1 to indicate that all TX data has been written to CIR TX FIFO.
5-0	Reserved	-	-	Reserved

CIR TX Data Register — Index 03h

Bit	Name	R/W	Default	Description
7-0	TX_DATA	R/W	-	The transmittion data should be written to TX_DATA.

CIR Control Register — Index 04h

Bit	Name	R/W	Default	Description
7-0	CIR_CMD	R/W	0	Host writes command to CIR.

8.10 PME, ACPI and ERP Registers (CR0A)

PME Device Enable Register — Index 30h

Bit	Name	R/W	Default	Description
7-1	Reserved	-	-	Reserved
0	PME_EN	R/W	0	0: disable PME. 1: enable PME.

PME Event Enable 1 Register — Index F0h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	MO_PME_EN	R/W	0	Mouse PME event enable. 0: disable mouse PME event. 1: enable mouse PME event.
5	KB_PME_EN	R/W	0	Keyboard PME event enable. 0: disable keyboard PME event. 1: enable keyboard PME event.
4	HM_PME_EN	R/W	0	Hardware monitor PME event enable. 0: disable hardware monitor PME event. 1: enable hardware monitor PME event.
3	PRT_PME_EN	R/W	0	Parallel port PME event enable. 0: disable parallel port PME event. 1: enable parallel port PME event.
2	UR2_PME_EN	R/W	0	UART 2 PME event enable. 0: disable UART 2 PME event. 1: enable UART 2 PME event.

1	UR1_PME_EN	R/W	0	UART 1 PME event enable. 0: disable UART 1 PME event. 1: enable UART 1 PME event.
0	Reserved	R/W	0	Reserved.

PME Event Status 1 Register — Index F1h

Bit	Name	R/W	Default	Description
7	Reserved	-	-	Reserved
6	MO_PME_ST	R/W	-	Mouse PME event status. 0: Mouse has no PME event. 1: Mouse has a PME event to assert. Write 1 to clear to be ready for next PME event.
5	KB_PME_ST	R/W	-	Keyboard PME event status. 0: Keyboard has no PME event. 1: Keyboard has a PME event to assert. Write 1 to clear to be ready for next PME event.
4	HM_PME_ST	R/W	-	Hardware monitors PME event status. 0: Hardware monitor has no PME event. 1: Hardware monitor has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	PRT_PME_ST	R/W	-	Parallel port PME event status. 0: Parallel port has no PME event. 1: Parallel port has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	UR2_PME_ST	R/W	-	UART 2 PME event status. 0: UART 2 has no PME event. 1: UART 2 has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	UR1_PME_ST	R/W	-	UART 1 PME event status. 0: UART 1 has no PME event. 1: UART 1 has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	Reserved	R/W	-	Reserved

PME Event Enable 2 Register — Index F2h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	CIR_PME_EN	R/W	0	CIR PME event enable. 0: disable CIR PME event. 1: enable CIR PME event.
3	Reserved	-	-	Reserved
2	RI2_PME_EN	R/W	0	RI2# PME event enable. 0: disable RI2# PME event. 1: enable RI2# PME event.

1	RI1_PME_EN	R/W	0	RI1# PME event enable. 0: disable RI2# PME event. 1: enable RI2# PME event.
0	GP_PME_EN	R/W	0	GPIO PME event enable. 0: disable GPIO PME event. 1: enable GPIO PME event.

PME Event Status 2 Register — Index F3h

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	CIR_PME_ST	R/W	-	CIR PME event status. 0: CIR has no PME event. 1: CIR has a PME event to assert. Write 1 to clear to be ready for next PME event.
3	ERP_PME_ST	R/W	-	ERP PME event status. 0: ERP has no PME event. 1: ERP has a PME event to assert. Write 1 to clear to be ready for next PME event.
2	RI2_PME_ST	R/W	-	RI2# PME event status. 0: RI2# has no PME event. 1: RI2# has a PME event to assert. Write 1 to clear to be ready for next PME event.
1	RI1_PME_ST	R/W	-	RI1# PME event status. 0: RI1# has no PME event. 1: RI1# has a PME event to assert. Write 1 to clear to be ready for next PME event.
0	GP_PME_ST	R/W	-	GPIO PME event status (operate only under S0 stage). 0: GPIO has no PME event. 1: GPIO has a PME event to assert. Write 1 to clear to be ready for next PME event.

ACPI Control Register 1 — Index F4h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Reserved
6	EN_CIRWAKEUP	R/W	0	Set one to enable CIR wakeup event asserted via PSOUT#.

5	DUAL_GATE_S5_ON	R/W	1	0: DUAL_GATE_N tri-state in S5 state. 1: DUAL_GATE_N output low in S5 state.
4	EN_KBWAKEUP	R/W	0	Set one to enable keyboard wakeup event asserted via PWSOUT#.
3	EN_MOWAKEUP	R/W	0	Set one to enable mouse wakeup event asserted via PWSOUT#.
2-1	PWRCTRL	R/W	11	The ACPI Control the PSON_N to always on or always off or keep last state 00 : keep last state 10 : Always on 01 : Always on without PSOUT# 11: Always off
0	VSB_PWR_LOSS	R/W	0	When VSB 3V comes, it will set to 1, and write 1 to clear it

ACPI Control Register 2 — Index F5h

Bit	Name	R/W	Default	Description
7	Reserved	R/W	0	Dummy for future use.
6-5	PWROK_DELAY	R/W	0	The additional PWROK delay. 00: no delay 01: 100ms. 10: 200ms 11: 400ms.
4-3	VDD_DELAY	R/W	00	The PWROK delay timing from VDD3VOK by followed setting 00 : 100ms 01 : 200ms 10 : 300ms 11 : 400ms
2	VINDB_EN	R/W	1	Enable the PCIRSTIN_N and ATXPWGD de-bounce.
1	PCIRST_DB_EN	R/W	0	Enable the LRESET_N de-bounce.
0	Reserved	R/W	0	Dummy register.

ACPI Control Register 3 — Index F6h

Bit	Name	R/W	Default	Description
7	S3_SEL	R/W	0	Select the KBC S3 state. 0: Enter S3 state when internal VDD3VOK signal de-asserted. 1: Enter S3 state when S3# is low or the TS3 register is set to 1.
6	Reserved	-	-	Reserved.
5	WDT_RST_EN	R/W	0	0: Disable WDT time out reset signal 1: Enable WDT time out reset signal output form PWROK.
4	PSON_DEL_EN	R/W	0	0: PSON# is the inverted of S3# signal. 1: PSON# will sink low only if the time after the last turn-off elapse at least 4 seconds.
3	VREF_S3_RST_EN	R/W	0	0: The VREF output value programmed by user will keep in S3/S5 state. 1: The VREF output value will be reset to default (64h) when enter S3/S5 state.
2	PCIRST3_GATE	R/W	1	Write “0” to this bit will force PCIRST3# to sink low.
1	PCIRST2_GATE	R/W	1	Write “0” to this bit will force PCIRST2# to sink low.
0	PCIRST1_GATE	R/W	1	Write “0” to this bit will force PCIRST1# to sink low.

ACPI Control Register 4 — Index F7h

Bit	Name	R/W	Default	Description
7	USBEN_DS5_ST	R/W	0	USBEN deep output value in deep s5 state. (powered by VBAT)
6	USBEN_S5_ST	R/W	0	USBEN deep output value in s5 state. (powered by VBAT)
5	USBEN_DS3_ST	R/W	0	USBEN deep output value in deep s3 state.
4	USBEN_S3_ST	R/W	1	USBEN deep output value in s3 state.
3-2	Reserved	R/W	-	Reserved
1-0	VCC_GATE_DELAY	R/W	00	VCCGATE# will be low when S3# is high, VCC3V is power on and VCC5V is power on. This register define the delay time from the condition is ready: 00: 10ms 01: 50ms 10: 100ms 11: 200ms

LED Additional Mode Select — Index FAh (powered by VBAT)

Bit	Name	R/W	Default	Description
7	Reserved	R/W	-	Reserved
6	LED_VSB_S5_ADD	R/W	0	Refer to LED_VSB_S5_MODE.
5	LED_VSB_S3_ADD	R/W	0	Refer to LED_VSB_S3_MODE.
4	LED_VSB_S0_ADD	R/W	0	Refer to LED_VSB_S0_MODE.
3	Reserved	R/W	-	Reserved
2	LED_VCC_S5_ADD	R/W	0	Refer to LED_VCC_S5_MODE.
1	LED_VCC_S3_ADD	R/W	0	Refer to LED_VCC_S3_MODE.
0	LED_VCC_S0_ADD	R/W	0	Refer to LED_VCC_S0_MODE.

Intel DSW Delay Select Register— Index FCh

Bit	Name	R/W	Default	Description
7-5	Reserved	R/W	-	Reserved
4	DUAL_GATE_DSW_EN	R/W	0	When this bit is set “1”. DUALGATE will be inverted of SUS_WARN#.
3-0	DSW_DELAY	R/W	7h	This is the delay time for SUS_ACK# and SUS_WARN#. Time unit is 0.5s.

RI De-bounce Select Register — Index FEh

Bit	Name	R/W	Default	Description
7-5	Reserved	-	-	Reserved
4	IR_VDD_S3	R/W	0	Set “1” to emulate S3 state for CIR.
3-2	Reserved	-	-	Reserved

1-0	RI_DB_SEL	R/W	0	Select RI de-bounce time. 00: reserved. 01: 200us. 10: 2ms. 11: 20ms.

ERP Enable Register — Index E0h

Bit	Name	R/W	Default	Description
7	ERP_EN	R/W	1	0 : disable ERP function 1: enable ERP function
6	S3_BACK	R/W	0	When this bit is set. It indicates the system is back from S3 state.
5	Reserved	-	-	Reserved
4	EVENT1_EN	R/W	0	USBEN/EVENT_IN1# function select. 0: The pin function is USBEN. 1: The pin function is EVENT_IN1#.
3	EVENT1_PME_EN	R/W	0	EVENT1 PME# event enable. 0: disable EVENT1 PME# event. 1: enable EVENT1 PME# event, when RING1 falling edge detect
2	EVENT1_PSOUT_EN	R/W	0	EVENT1 PSOUT# event enable. 0: disable EVENT1 PSOU#T event. 1: enable EVENT1 PSOUT# event, when RING2 falling edge detect
1	EVENT0_PME_EN	R/W	0	EVENT0 PM#E event enable. 0: disable EVENT0 PME# event. 1: enable EVENT0 PME# event, when RING1 falling edge detect
0	EVENT0_PSOUT_EN	R/W	0	EVENT0 PSOUT# event enable. 0: disable EVENT0 PSOUT# event. 1: enable EVENT0 PSOUT# event, when RING1 falling edge detect

ERP control register — Index E1h

Bit	Name	R/W	Default	Description
7-6	Boot_Mode	R/W	11	Write these two bits to select Boot Mode for Always Off/ Always On/ Keep Last State. 00:Default Always Off 11:Support Always On and Keep Last State 10:Reserved 01:Reserved
5	S3_ CTRL_1_DIS	R/W	0	If clear to “0” CTRL_1 will output Low when S3 state. Else If set to “1” CTRL_1 will output High when S3 state.
4	S3 _CTRL_0_DIS	R/W	0	If clear to “0” CTRL_0 will output Low when S3 state. Else If set to “1” CTRL_0 will output High when S3 state.
3	S5 _CTRL_1_DIS	R/W	1	If clear to “0” CTRL_1 will output Low when S5 state. Else If set to “1” CTRL_1 will output High when S5 state.
2	S5 _CTRL_0_DIS	R/W	1	If clear to “0” CTRL_0 will output Low when S5 state. Else If set to “1” CTRL_0 will output High when S5 state.

1	AC_ CTRL_1_DIS	R/W	0	If clear to “0” CTRL_1 will output Low when after AC lost. Else If set to “1” CTRL_1 will output High when after AC lost.
0	AC_ CTRL_0_DIS	R/W	0	If clear to “0” CTRL_0 will output Low when after AC lost. Else If set to “1” CTRL_0 will output High when after AC lost.

ERP control register — Index E2h

Bit	Name	R/W	Default	Description
7	AC_LOST	R/WC	-	“1” indicates an AC lost occurs. Write “1” to clear.
6	Reserved	-	-	Reserved.
5	VSB_CTRL_EN[1]	R/W	1’b0	0: disable ERP_CTRL1# assert RSMRST# low 1: enable ERP_CTRL 1# assert RSMRST# low
4	VSB_CTRL_EN[0]	R/W	1’b0	0: disable ERP_CTRL0# assert RSMRST# low 1: enable ERP_CTRL0# assert RSMRST# low
3-1	Reserved	-	-	Reserved
0	RSMRST_DET_3V_N	R/W	0	Device detects VSB5V power ok (4.4V) and VSB3V_IN become high, and after 60ms de-bounce time RSMRST will become high. But when user set this bit to 1. RSMRST will not check VSB3V_IN pin status.

ERP PSIN deb-register — Index E3h

Bit	Name	R/W	Default	Description
7-0	PS_DEB_TIME	R/W	0x13	PS_IN# pin input de-bounce time: the unit of this register is 1ms, default is 20ms.

ERP RSMRST deb-register — Index E4h

Bit	Name	R/W	Default	Description
7-0	RSMRST_DEB_TIME	R/W	0x09	RSMRST# internal de-bounce time: the unit of this register is 1ms, default is 10ms.

ERP PSOUT deb-register — Index E5h

Bit	Name	R/W	Default	Description
7-0	PS_OUT_PULSE_W	R/W	0xC7	PS_OUT_OUT output Pulse width: the unit of this register is 1ms , default is 200ms low pulse

ERP PSON deb-register — Index E6h

Bit	Name	R/W	Default	Description
7-0	PS_ON_DEB_TIME	R/W	0x09	PSON_IN pin input de-bounce time: the unit of this register is 1ms, default is 10ms.

ERP S5 deb-register — Index E7h

Bit	Name	R/W	Default	Description
7-0	S5_DEB_TIME	R/W	0x63	S5# pin input de-bounce time The unit of this register is 64ms, default is 6.4s.

ERP Wakeup Event Enable Register — Index E8h

Bit	Name	R/W	Default	Description
7	RI2_WAKEUP_EN	R/W	0	Enable RI2# PME# event to wakeup.
6	CIR_WAKEUP_EN	R/W	0	Enable CIR PME# event to wakeup.
5	RI1_WAKEUP_EN	R/W	0	Enable RI1# PME# event to wakeup.
4	EVENT_WAKEUP_EN	R/W	1	Enable EVENT_IN# event to wakeup.
3	Reserved	R/W	0	Reserved
2	TMOUT_WAKEUP_EN	R/W	0	Enable ErP Watchdog Timer timeout event to wakeup. See index EDh and EEh.
1	MO_WAKEUP_EN	R/W	0	Enable Mouse PME# event to wakeup.
0	KB_WAKEUP_EN	R/W	0	Enable Keyboard PME# event to wakeup.

ERP Deep S3 Delay Register — Index E9h

Bit	Name	R/W	Default	Description
7-0	S3_DEL_TIME	R/W	0xFF	S3 to deep S3 delay time. The unit of this register is 64ms, default is 16.32s.

ERP control register 2— Index ECh

Bit	Name	R/W	Default	Description
7-6	ERP_MODE	R/W	00	ERP mode select. 00: Fintek G3`. 01: Fintek G3` + Intel DSW. 10: Reserved. 11: Intel DSW.
5	DPWROK_CTRL_EN	R/W	0	Set “1” to enble DPWROK reset by ERP_CTRL1#.
4	VSB_CTRL_EN[2]	R/W	1’b0	0: disable ERP_CTRL2# assert RSMRST# low 1: enable ERP_CTRL 2# assert RSMRST# low
3	Revered	-	-	Reserved.
2	S3 _CTRL_2_DIS	R/W	0	If clear to “0” CTRL_2 will output Low in deep S3 state. Else If set to “1” CTRL_2 will output High in deep S3 state.
1	S5 _CTRL_2_DIS	R/W	1	If clear to “0” CTRL_2 will output Low in deep S5 state. Else If set to “1” CTRL_2 will output High in deep S5 state.
0	AC_ CTRL_2_DIS	R/W	0	If clear to “0” CTRL_2 will output Low when after AC lost. Else If set to “1” CTRL_2 will output High when after AC lost.

ERP Watchdog Control Register — Index EDh

Bit	Name	R/W	Default	Description
7-5	Revered	-	-	Reserved.
4	WD_TMOUT	R/WC	0	ERP watchdog timer timeout status. Write 1 to clear.
3-2	Revered	-	-	Reserved.

1	WD_UNIT	R/W	0	0: unit of WD_TIME is 1 sec. 1: unit of WD_TIME is 1 minute.
0	WD_EN	R/W	0	Enable ERP watchdog timer.

ERP Watchdog Time Register — Index EEh

Bit	Name	R/W	Default	Description
7-0	WD_TIME	R/W	0	ERP watchdog timer count time register. Start to count down when WD_EN is set. When reaching 0, WD_EN will auto clear and WD_TMOUT is set. A wakeup event will assert if enabled

8.11 VREF Control Registers (CR0B)

VREF3 Output Value — Index F0h

Bit	Name	R/W	Default	Description
7-0	VREF3_H	R/W	8'h64	The bit8-1 of VREF3 output value.

VREF2 Output Value — Index F1h

Bit	Name	R/W	Default	Description
7-0	VREF2_H	R/W	8'h64	The bit8-1 of VREF2 output value.

VREF1 Output Value — Index F2h

Bit	Name	R/W	Default	Description
7-0	VREF1_H	R/W	8'h64	The bit8-1 of VREF1 output value.

WDT Reset Enable — Index FFh

Bit	Name	R/W	Default	Description
7-1	Reserved.	-	-	Reserved.
0	WD_RST_EN	R/W	0	0: disable the WDT reset function. 1: VREF1~3 will be reset to default if WDT timeout occurs.

9 Electrical Characteristics

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to 70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

All ACPI timing accuracy is ±20%.

DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.3V ± 10%, VSS = 0V) (Note)

Parameter	Conditions	MIN	TYP	MAX	Unit
Temperature Error, Remote Diode	60 °C < T_D < 100 °C, VCC = 3.0V to 3.6V -40 °C <T_D < 60°C 100 °C <T_D < 127°C		± 1 ± 1	± 3 ± 3	°C
Supply Voltage range		3.0	3.3	3.6	V
Average operating supply current			10		mA
Standby supply current			5		uA
VBAT Current			1		uA
Resolution			1		°C
Power on reset threshold			2.2	2.4	V
Diode source current	High Level		95		uA
	Low Level		10		uA

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
$I/O_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{12t}-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OOD_{18t}-TTL level bi-directional pin, Output pin with 18mA source-sink capability, and can programming to open-drain function.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V

Output Low Current	IOL		-18		mA	VOL = 0.4 V
Output High Current	IOH		+18		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OOD_{12,5v}$-TTL level bi-directional pin, Output pin with 12mA source-sink capability, and can programming to open-drain function, 5v tolerance.						
Input Low Threshold Voltage	Vt-			0.8	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VDD = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
I/OD_{14t}-TTL level bi-directional pin, Open-drain output with14 mA sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		-14		mA	VOL = 0.4 V
I/O_{16t}- TTL level bi-directional pin, Output pin with 16mA source-sink capability.						
Input Low Threshold Voltage	Vt-			0.6	V	VDD = 3.3 V
Input High Threshold Voltage	Vt+	0.9			V	VDD = 3.3 V
Output High Current	IOH		+16		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = 1.2V
Input Low Leakage	ILIL	-1			μA	VIN = 0V
IN_{st} - TTL level input pin with schmitt trigger						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{t,5v}$ - TTL level input pin with 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,5v}$ - TTL level input pin with schmitt trigger, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$IN_{st,lv}$ - TTL level input pin with schmitt trigger, low level.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
OD_{12}-Open-drain output with12 mA sink capability.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{12,5v}$-Open-drain output with12 mA sink capability, 5V tolerance.						
Output Low Current	IOL		-12		mA	VOL = 0.4V
$OD_{16,u10,5v}$-Open-drain output with 16 mA sink capability, pull-up 10k ohms, 5V tolerance.						
Output Low Current	IOL		-16		mA	VOL = 0.4V
$O_{8,u47,5v}$- Output pin with 8 mA source-sink capability, pull-up 47k ohms, 5V tolerance.						
Output High Current	IOH	+6	+8		mA	VOH = 2.4V
O_{12}- Output pin with 12 mA source-sink capability.						
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
O_{16}- Output pin with 16 mA source-sink capability.						

Output High Current	IOH		+16		mA	VOH = 2.4V
O_{18}- Output pin with 18 mA source-sink capability.						
Output High Current	IOH		+18		mA	VOH = 2.4V
O_{24}- Output pin with 24 mA source-sink capability.						
Output High Current	IOH		+24		mA	VOH = 2.4V
O_{14}- Output pin with 14 mA source-sink capability.						
Output High Current	IOH		+14		mA	VOH = 2.4V
O_{30}- Output pin with 30 mA source-sink capability.						
Output High Current	IOH	+26	+30		mA	VOH = 2.4V
$I/O_{s1, D8,st, Iv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive and 1mA sink capability.						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+8		mA	VOH = 1.0V
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/O_{D8,st, Iv}$ - Low level bi-directional pin (VIH → 0.9V, VIL → 0.6V.) with schmitt trigger. Output with 8mA drive						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Output High Current	IOH		+8		mA	VOH = 1.0V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/OD_{12st,Iv}$ - Low level bi-directional pin with schmitt trigger. Open-drain output with 12mA sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		-12		mA	VOH = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/OOD_{12st,Iv}$ - Low level bi-directional pin with schmitt trigger, can select to OD or OUT by register, with 12 mA source-sink capability.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		-12		mA	VOH = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0 V
$I/OD_{12st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with12 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V
$I/OD_{16st,5v}$-TTL level bi-directional pin with schmitt trigger, Open-drain output with 16 mA sink capability, 5V tolerance.						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Current	IOL		+16		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	μA	VIN = VDD
Input Low Leakage	ILIL	-1			μA	VIN = 0V

10 Ordering Information

Part Number	Package Type	Production Flow
F71889AD	128-LQFP Green Package	Commercial, 0°C to +70°C

11 Top Marking Specification

The version identification is shown as the bold red three characters. Please refer to below table for detail:

1st Line: Fintek Logo

● : Pin 1 Identifier

2nd Line: Device Name where the last alphabet always means package code → **F71889AD**

3rd Line: Assembly Plant Code (x) + Assembled Year Code (x) + Week Code (xx) + Fintek Internal Code (xx) + **IC Version (x)** where A means version, B means version B, …

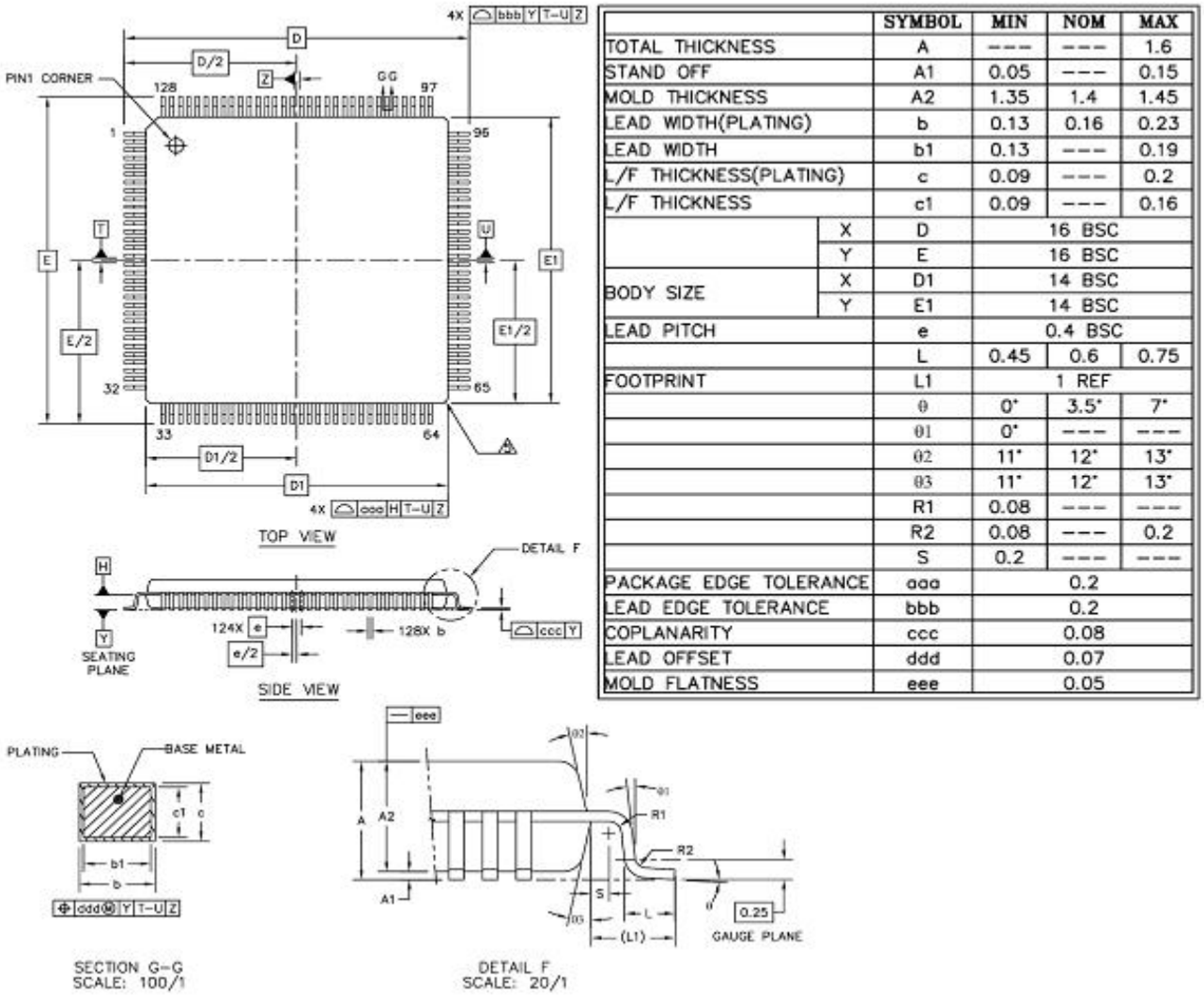
4th Line: Wafer Fab Code (XXXX…XX)

12 Package Dimensions

128 LQFP (14*14)

All Dimensions Shown in mm

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.16	0.23
LEAD WIDTH		b1	0.13	---	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



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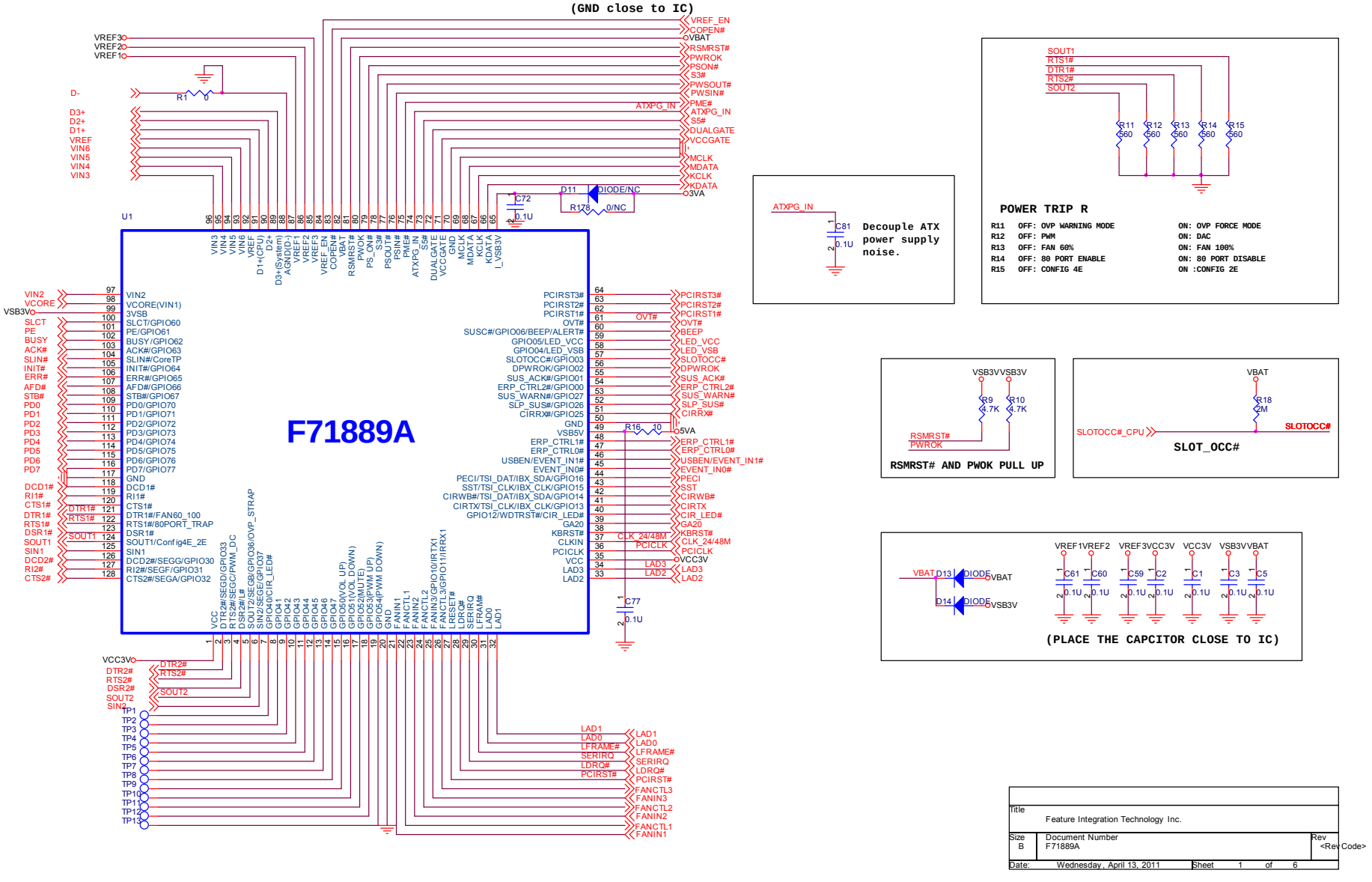
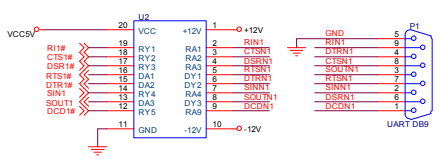
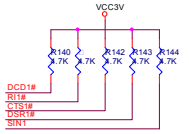
13 Application Circuit

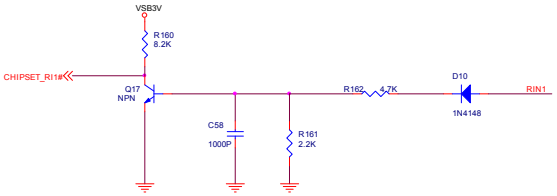




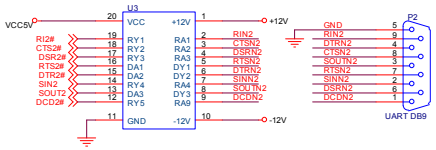


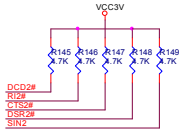
UART 1 PORT INTERFACE

If you do not use the UART port 1, please pull-up these pin to VCC3V.



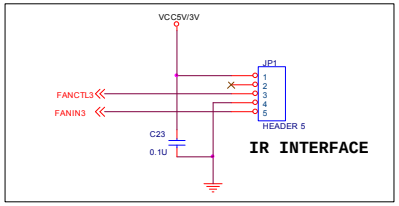
Wake up on ring for serial port circuit.



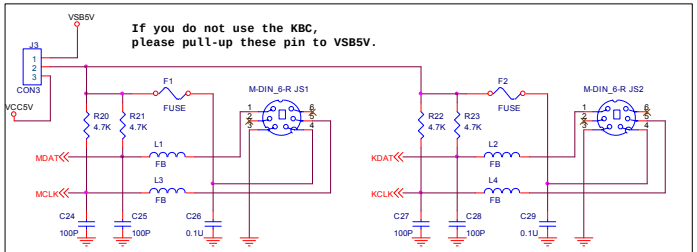


UART 2 PORT INTERFACE

If you do not use the UART port 2, please pull-up these pin to VCC3V.



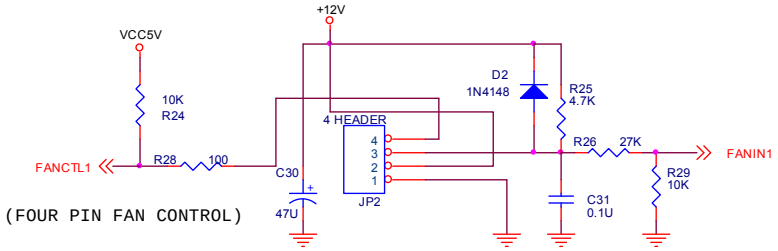
IR INTERFACE



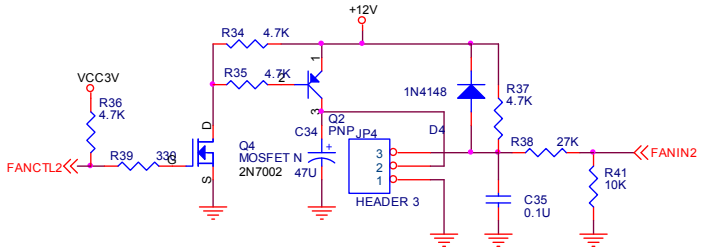
If you do not use the KBC, please pull-up these pin to VSB5V.

PS2 MOUSE INTERFACE **PS2 KEYBOARD INTERFACE**

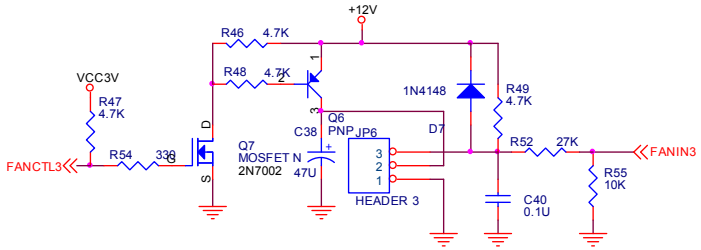
Title	Feature Intergration Technology Inc	
Size: Custom	Document Number: UART_PS2_IR	Rev: 0.1
Date: Friday, April 16, 2010	Sheet 2 of 6	



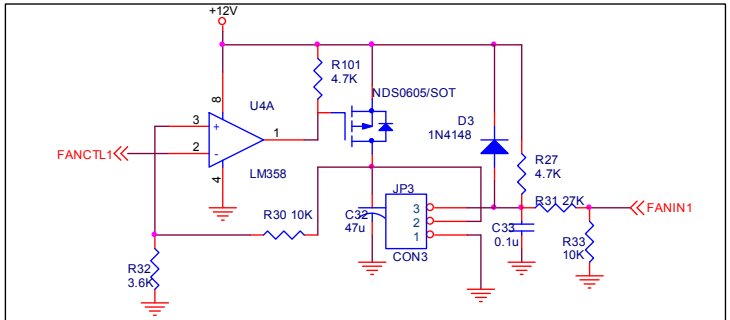
PWM FAN1 SPEED CONTROL



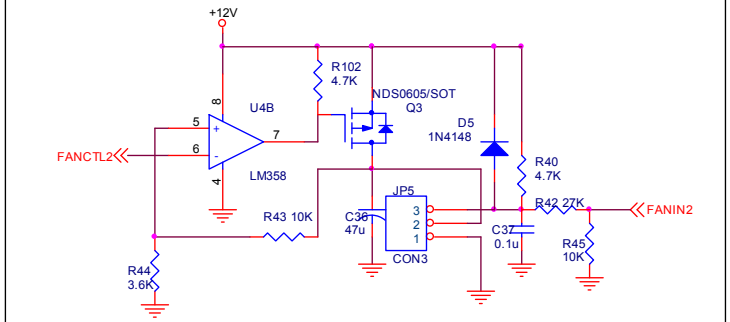
PWM FAN2 SPEED CONTROL



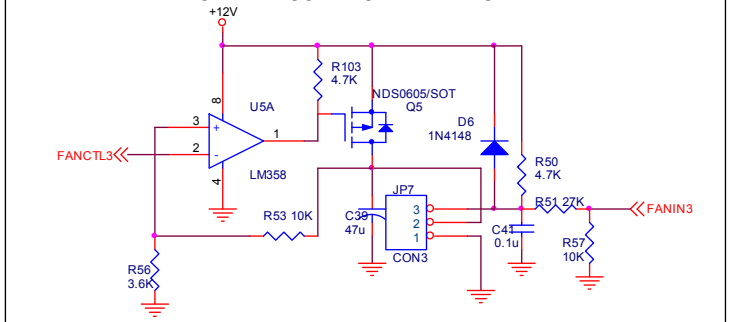
PWM FAN3 SPEED CONTROL



DC FAN CONTROL WITH OP 1



DC FAN CONTROL WITH OP 2



DC FAN CONTROL WITH OP 3

FAN CONTROL FOR PWM OR DC

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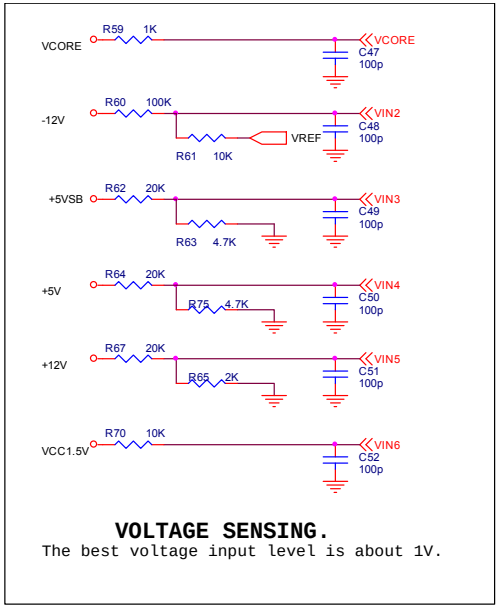
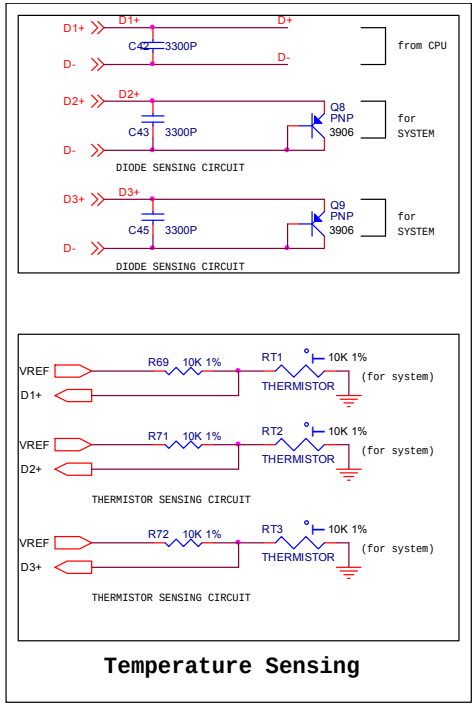
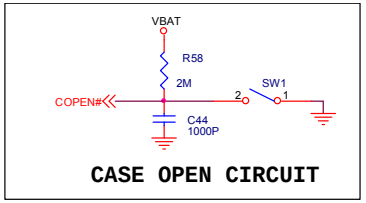


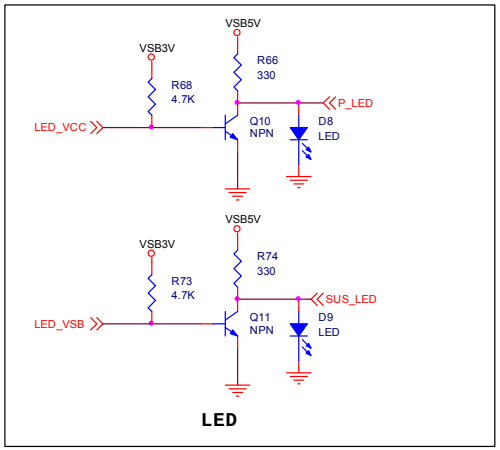
VOLTAGE SENSING.
The best voltage input level is about 1V.



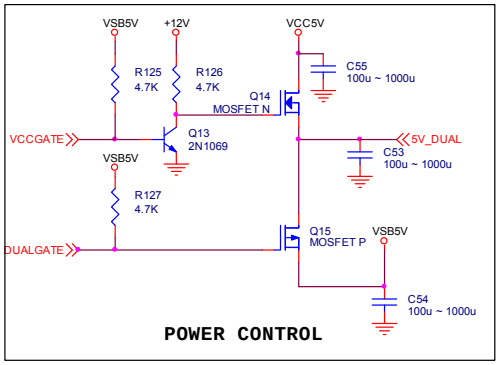
Temperature Sensing



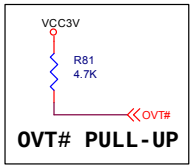
CASE OPEN CIRCUIT



LED



POWER CONTROL



OVT# PULL-UP

Title	Feature Integration Technology Inc.	
Size B	Document Number Hardware Monitor	Rev <RevCode>
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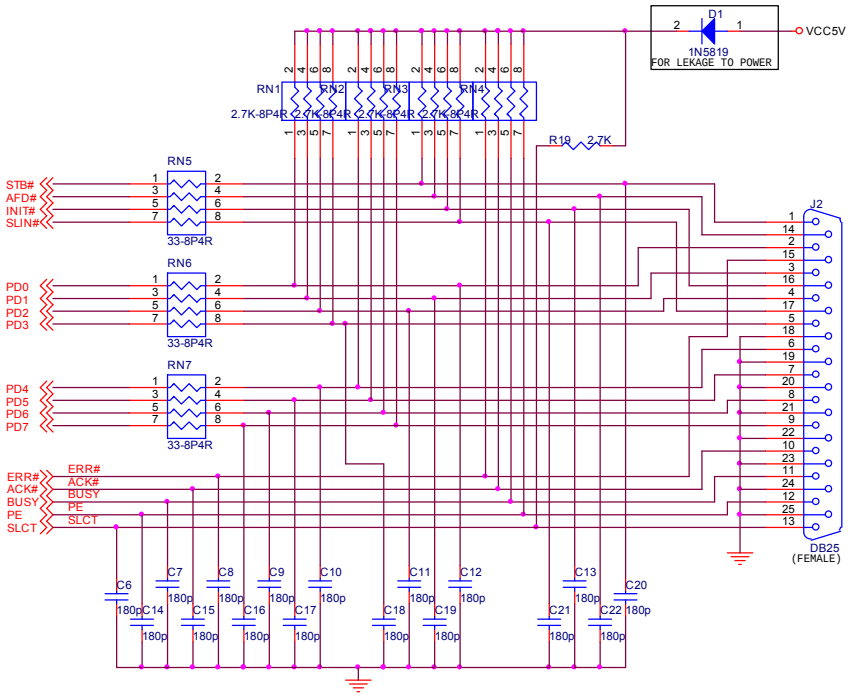
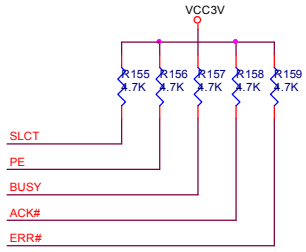
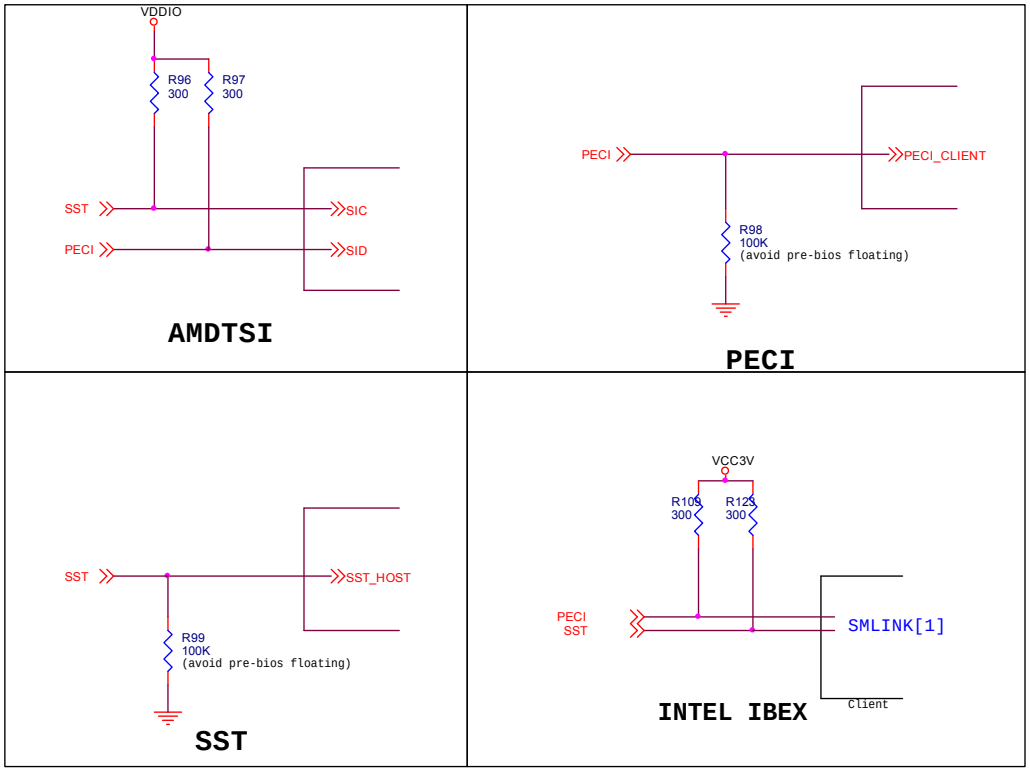


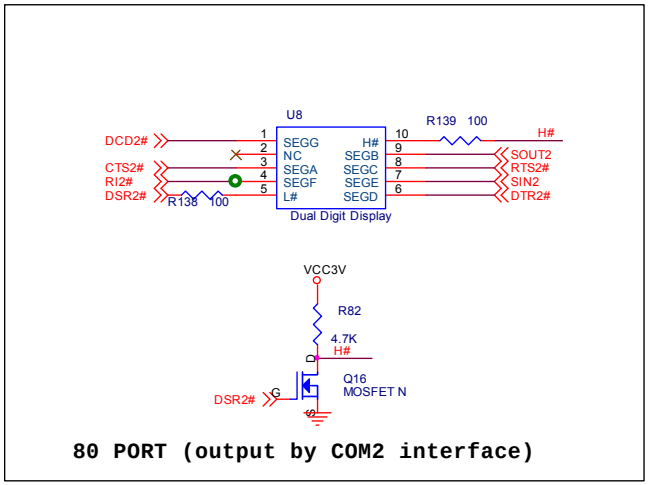
PARALLEL PORT INTERFACE



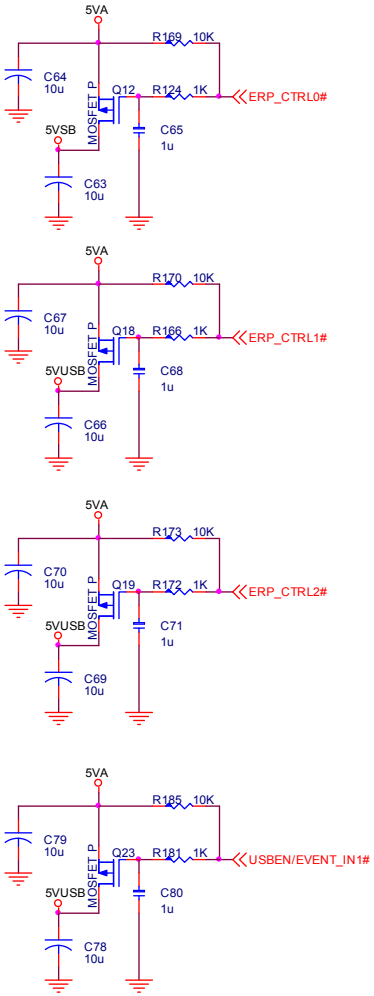
If you do not use the prarllel port , please pull-up these pin to VCC3V.

Title	Feature Integration Technology Inc.	
Size B	Document Number PRINTER PORT	Rev <RevCode>
Date: Friday, April 16, 2010	Sheet 5 of 6	

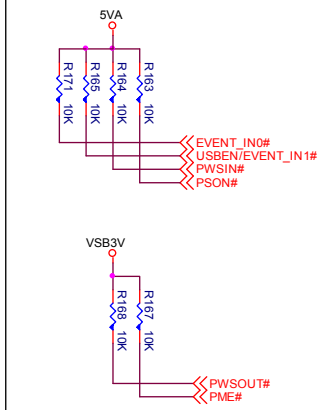




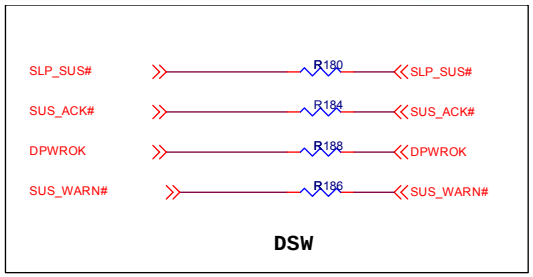
Title	Feature Integration Technology Inc.	
Size B	Document Number AMDTSI/SST/PECI/80PORT	Rev <Rev Code>
Date: Friday, April 16, 2010	Sheet 6 of 6	



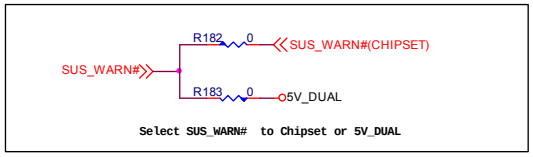
ERP Control VSB



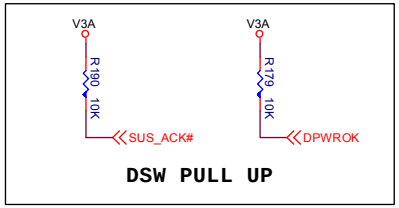
ERP ACPI PULL UP



DSW



Select SUS_WARN# to Chipset or 5V_DUAL



DSW PULL UP

Title: Feature Integration Technology Inc.		
Size: B	Document Number: ERP_CONTROL	Rev: <Rev Code>
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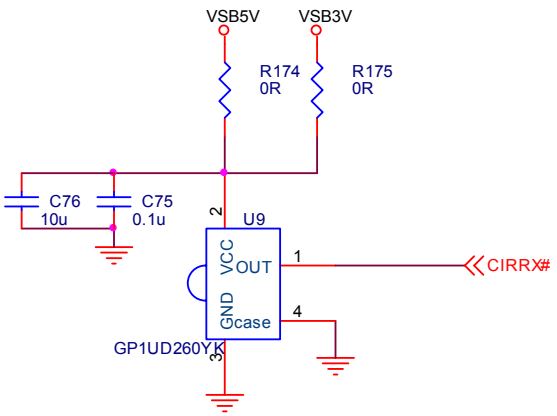
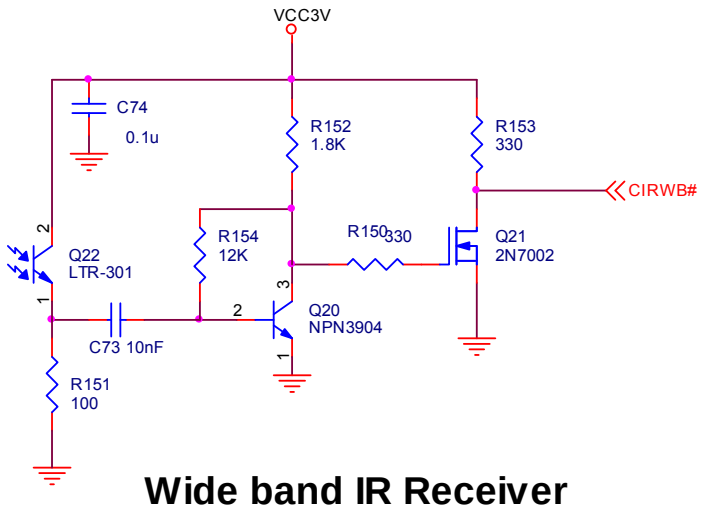
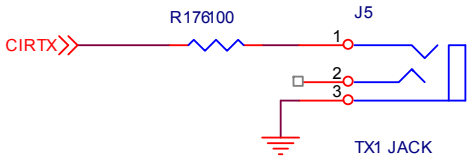


Long Rang IR Receiver

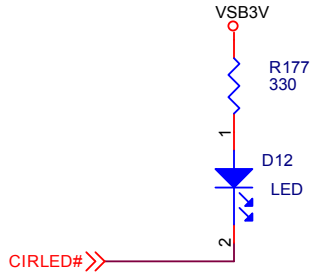
choose power and capacitance by IR receiver



Wide band IR Receiver



TX PORT



IR LED

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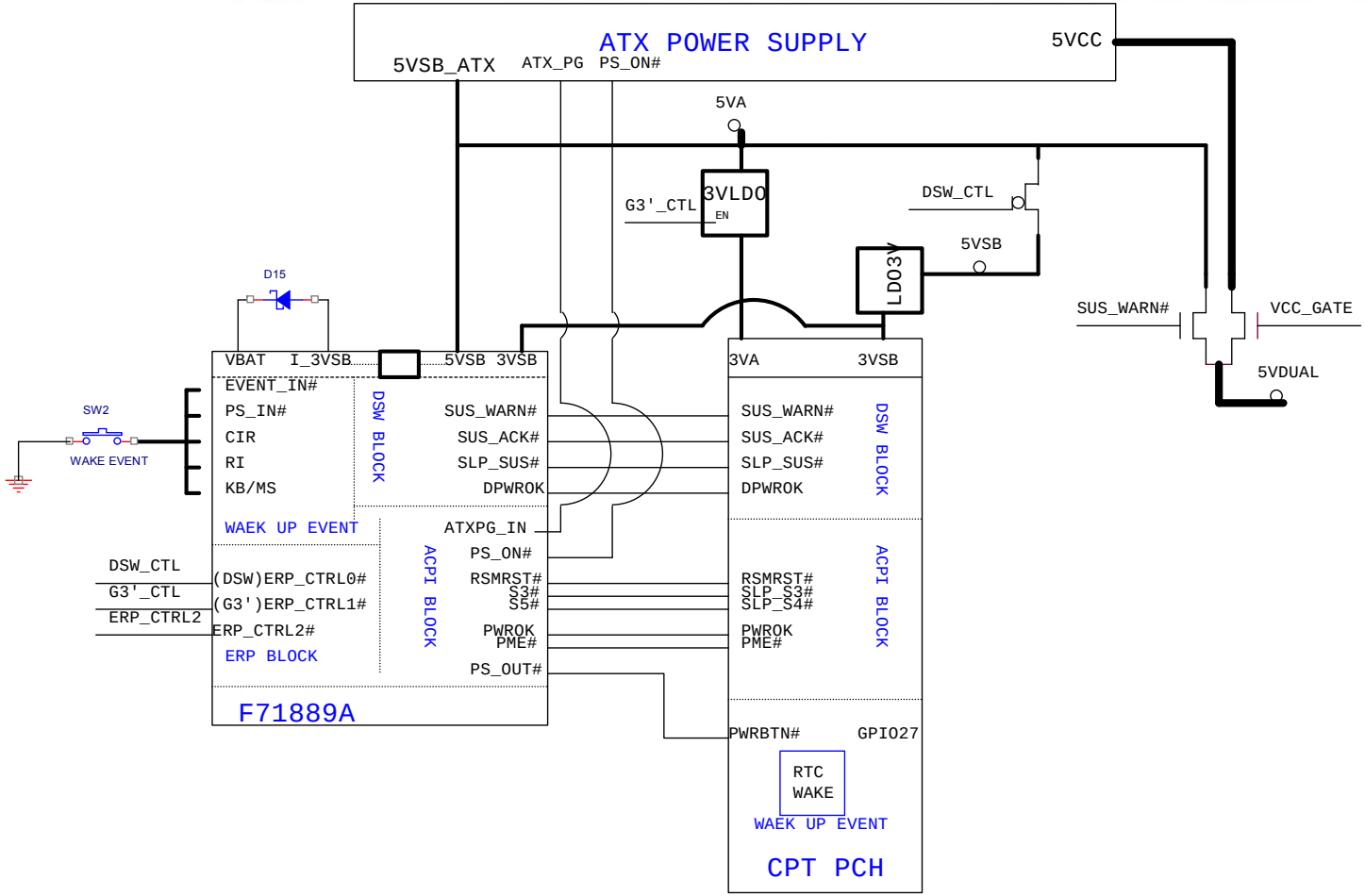
Size: A	Document Number: CIR	Rev: <Rev Code>
Date: Friday, April 16, 2010	Sheet 1 of 1	



Title	Feature Integration Technology Inc.	
Size B	Document Number ACPI BLOCK	Rev <Rev Code>
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