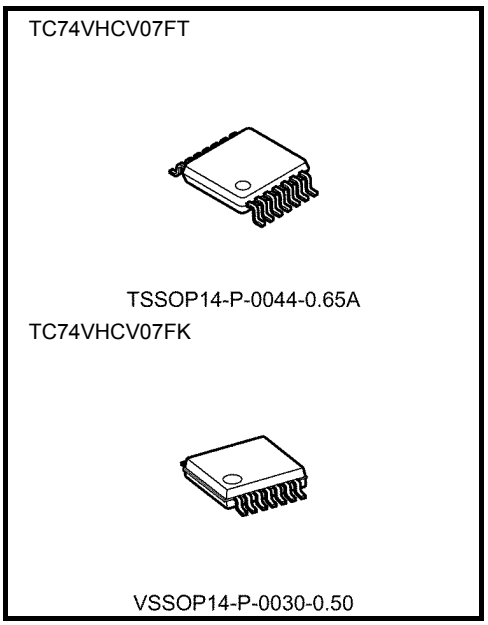
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHCV07FT,TC74VHCV07FK

Hex Schmitt Buffer (open drain)

The TC74VHCV07 is an advanced high speed CMOS BUFFER fabricated with silicon gate CMOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
Output have high performance MOS N-channel transistor. (OPEN-DRAIN outputs)
Input pin have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHCV07 is capable of squaring up transitions of slowly changing input signals such as line receivers.
Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

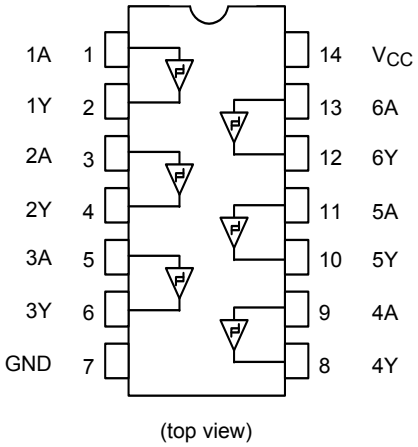


Weight
TSSOP14-P-0044-0.65A : 0.06 g (typ)
VSSOP14-P-0030-0.50 : 0.02 g (typ)

Features

- High speed: t_{pZ} = 3.8 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 2 μA (max) at Ta = 25°C
- Wide operating voltage range: $V_{CC\ (opr)}$ = 1.8 V to 5.5 V
- Ouput current: I_{OL} = 16 mA (min) (V_{CC} = 4.5 V)
- Available in TSSOP and VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 07 type

Pin Assignment

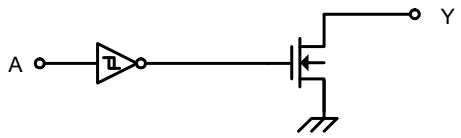


(top view)

Truth Table

A	Y
L	L
H	Z

System Diagram (per gate)



Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating		Unit
Supply voltage range	V_{CC}	−0.5 to 7.0		V
DC input voltage	V_{IN}	−0.5 to 7.0		V
DC output voltage	V_{OUT}	−0.5 to 7.0	(Note 2)	V
Input diode current	I_{IK}	−50		mA
Output diode current	I_{OK}	−50	(Note 3)	mA
DC output current	I_{OUT}	50		mA
Power dissipation	P_D	180		mW
DC V_{CC}/ground current	I_{CC}/I_{GND}	±100		mA
Storage temperature	T_{stg}	−65 to 150		°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state. I_{OUT} absolute maximum rating must be observed (Output in low state)

Note 3: $V_{OUT} < GND$

Operating Ranges (Note1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
output voltage	V_{OUT}	0 to 5.5	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 2 0 (V_{CC} = 3.3 ± 0.3 V) 0 to 1 (V_{CC} = 5 ± 0.5 V)	ms/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
Positive threshold voltage	V_P	—		1.8	—	—	1.65	—	1.65	V
				2.3	—	—	1.85	—	1.85	
				3.0	—	—	2.20	—	2.20	
				4.5	—	—	3.15	—	3.15	
				5.5	—	—	3.85	—	3.85	
Negative threshold voltage	V_N	—		1.8	0.15	—	—	0.15	—	
				2.3	0.45	—	—	0.45	—	
				3.0	0.90	—	—	0.90	—	
				4.5	1.35	—	—	1.35	—	
				5.5	1.65	—	—	1.65	—	
Hysteresis voltage	V_H	—		1.8	0.15	—	1.05	0.15	1.05	V
				2.3	0.20	—	1.10	0.20	1.10	
				3.0	0.30	—	1.20	0.30	1.20	
				4.5	0.40	—	1.40	0.40	1.40	
				5.5	0.50	—	1.60	0.50	1.60	
Low-level output voltage	V_{OL}	V_{IN} = V_{IL}	I_{OL} = 50 μA	1.8	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 8 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 16 mA	4.5	—	—	0.44	—	0.55	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH}, V_{OUT} = 0 to 5.5V		1.8 to 5.5	—	—	±0.25	—	±2.5	μA
Power-off leakage current	I_{OFF}	V_{IN}/V_{OUT} = 5.5 V		0	—	—	0.5	—	5.0	μA
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	2.0	—	20.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time	t_{pZL}	R_L = 1 kΩ	2.5 ± 0.2	15	—	6.7	10.4	1.0	13.0	ns
				50	—	9.4	15.2	1.0	18.0	
			3.3 ± 0.3	15	—	5.2	7.1	1.0	8.5	
				50	—	7.1	10.6	1.0	12.0	
			5.0 ± 0.5	15	—	3.8	5.5	1.0	6.5	
				50	—	5.3	7.5	1.0	8.5	
Propagation delay time	t_{pLZ}	R_L = 1 kΩ	2.5± 0.2	50	—	12.2	15.2	1.0	18.0	ns
			3.3 ± 0.3	50	—	9.5	10.6	1.0	12.0	
			5.0 ± 0.5	50	—	7.0	7.5	1.0	8.5	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Output capacitance	C_{OUT}	—			—	5	—	—	—	pF
Power dissipation capacitance	C_{PD}	(Note)			—	4	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

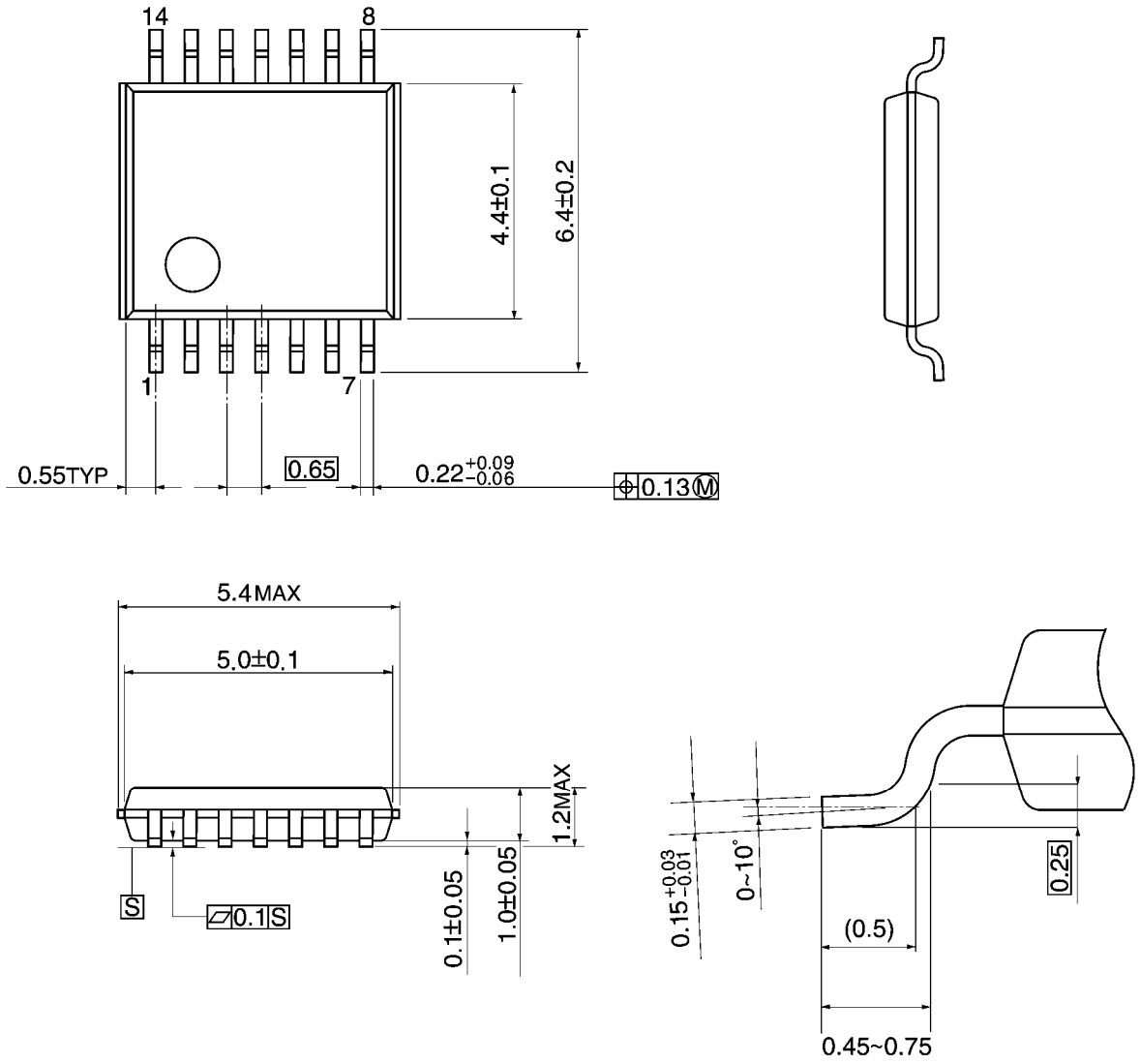
$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per gate)}$$

Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	3.3	0.3	—	V
			5.0	0.6	—	
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	3.3	−0.1	—	V
			5.0	−0.2	—	
Minimum high level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

Package Dimensions

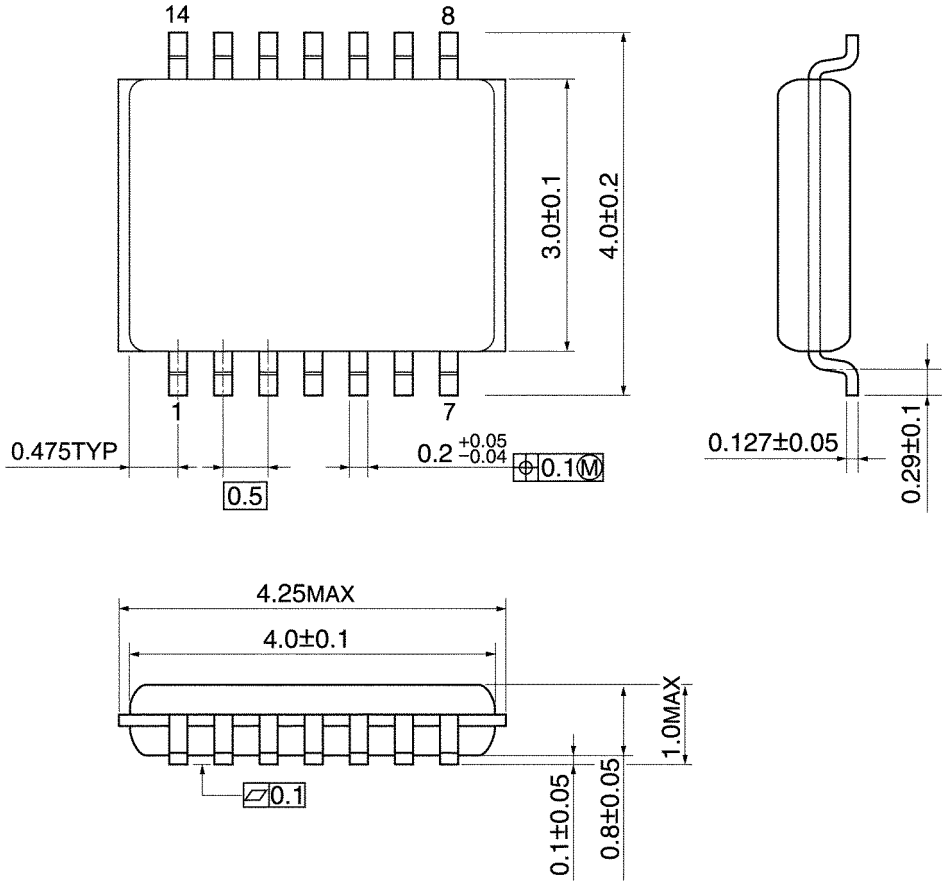
TSSOP14-P-0044-0.65A Unit: mm



Weight: 0.06 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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