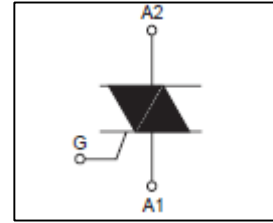


*Bi-Directional Triode Thyristor*

**Features**

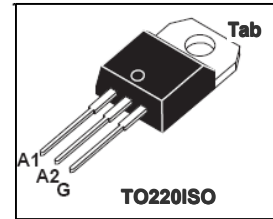
- Repetitive Peak off-State Voltage: 600V
- R.M.S On-State Current( $I_{T(RMS)}$ )=16A
- Low on-state voltage:  $V_{TM}=1.55V(\text{Max.})@ I_T=22.5A$
- High Commutation  $dV/dt$ .



**General Description**

General purpose swithhing and phase control applications. These devices are intended to be interfaced directly to micro-controllers, logic integrated circuits and other low power gate trigger circuits such as fan speed and temperature modulation control, lighting control and static switching relay.

The -W series are specially recommended for use on inductive loads, thanks to their high commutation performances. By using an internal ceramic pad, the WTPA series provides voltage insulated tab (rated at 2500V RMS). complying with UL standards (file ref.:E347423)



**Absolute Maximum Ratings** (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Value	Units
V <sub>DRM</sub> /V <sub>PRM</sub>	Peak Repetitive Forward Blocking Voltage(gate open) (Note 1)	600	V
I <sub>T(RMS)</sub>	Forward Current RMS (All Conduction Angles, T <sub>J</sub> =58°C)	16	A
I <sub>TSM</sub>	Peak Forward Surge Current, (full Cycle, Sine Wave, 50/60 Hz)	160/168	A
I <sup>2</sup> t	Circuit Fusing Considerations (tp= 10 ms)	144	A <sup>2</sup> s
P <sub>GM</sub>	Peak Gate Power — Forward, (T <sub>J</sub> = 58°C,Pulse with≤1.0us)	5	W
P <sub>G(AV)</sub>	Average Gate Power — Forward, (Over any 20ms period)	1	W
di/dt	Critical rate of rise of on-state current I <sub>TM</sub> = 20A; I <sub>G</sub> = 200mA; di <sub>G</sub> /dt = 200mA/μs	T <sub>J</sub> =125°C 50	A/μs
I <sub>FGM</sub>	Peak Gate Current — Forward, T <sub>J</sub> = 125°C (20 μs, 120 PPS)	4	A
V <sub>RGM</sub>	Peak Gate Voltage — Reverse, T <sub>J</sub> = 125°C (20 μs, 120 PPS)	10	V
T <sub>J</sub>	Junction Temperature	-40~125	°C
T <sub>stg</sub>	Storage Temperature	-40~150	°C

**Note1:** Although not recommended, off-state voltages up to 800V may be applied without damage, but the TRIAC may swiTJh to the on-state. The rate of rise of current should not exceed 15A/us.

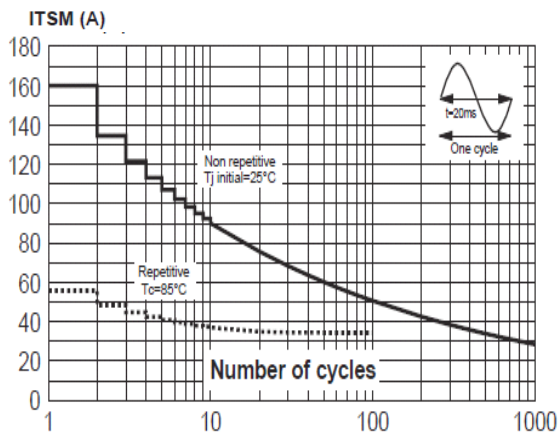
**Thermal Characteristics**

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R <sub>QJC</sub>	Thermal Resistance, Junction-to-Case	-	-	1.6	°C/W
R <sub>QJA</sub>	Thermal Resistance, Junction-to-Ambient	-	-	60	°C/W

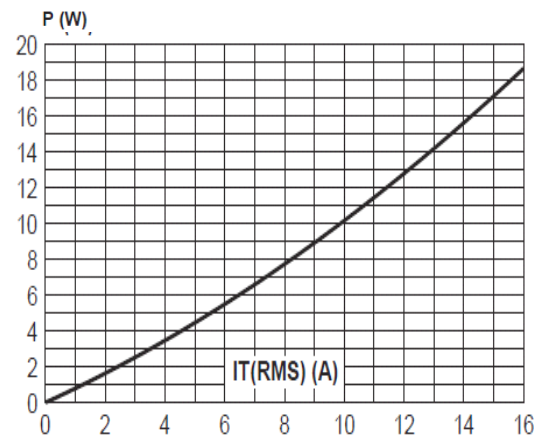
**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Characteristics	Min	Typ	Max	Unit	
$I_{DRM}/I_{RRM}$	Peak Forward or Reverse Blocking Current ( $V_{DRM}=V_{RRM}$ .)	$T_J=25^\circ\text{C}$	-	-	5	$\mu\text{A}$
		$T_J=125^\circ\text{C}$	-	-	1	mA
$V_{TM}$	Forward "On" Voltage (Note2) ( $I_{TM} = 22.5\text{A}$ $t_p=380\mu\text{s}$ )	-	-	1.55	V	
$I_{GT}$	Gate Trigger Current (Continuous dc) ( $V_D = 12\text{ Vdc}$ , $R_L = 33\ \Omega$ )	T2+G+	-	-	35	mA
		T2+G-	-	-	35	
		T2-G-	-	-	35	
$V_{GT}$	Gate Trigger Voltage (Continuous dc) ( $V_D = 12\text{ Vdc}$ , $R_L = 33\ \Omega$ )	T2+G+	-	-	1.2	V
		T2+G-	-	-	1.2	
		T2-G-	-	-	1.2	
$V_{GD}$	Gate threshold voltage( $V_D= V_{DRM}, R_L = 3.3\ \text{K}\Omega, T_J=125^\circ\text{C},$ )	0.2	-	-	V	
dV/dt	Critical rate of rise of commutation Voltage ( $V_D=0.67V_{DRM}$ )	40	-	-	V/ $\mu\text{s}$	
$I_H$	Holding Current ( $I_T= 100\ \text{mA}$ )	-	-	15	mA	
$I_L$	Latching current ( $V_D = 12\text{ Vdc}, I_{GT}=0.1\text{A}$ )	T2+G+	-	-	25	mA
		T2+G-	-	-	30	
		T2-G-	-	-	25	
$R_d$	Dynamic resistance	-	-	25	m $\Omega$	

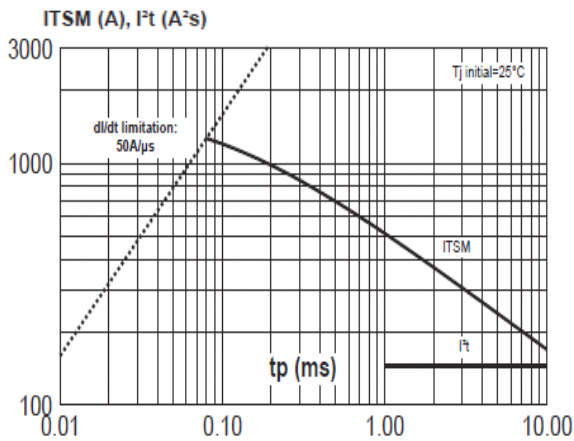
Note 2. Forward current applied for 1 ms maximum duration, duty cycle



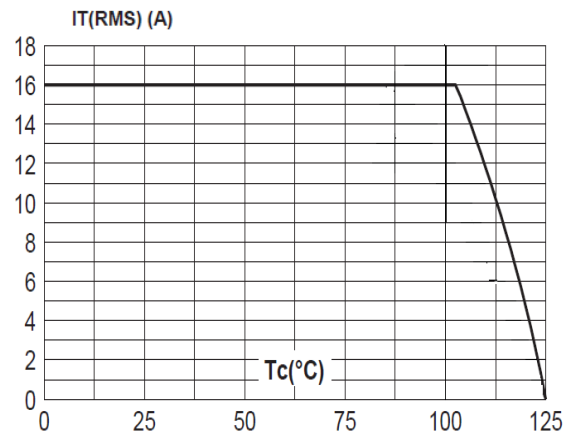
**Fig.1** Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50$  Hz.



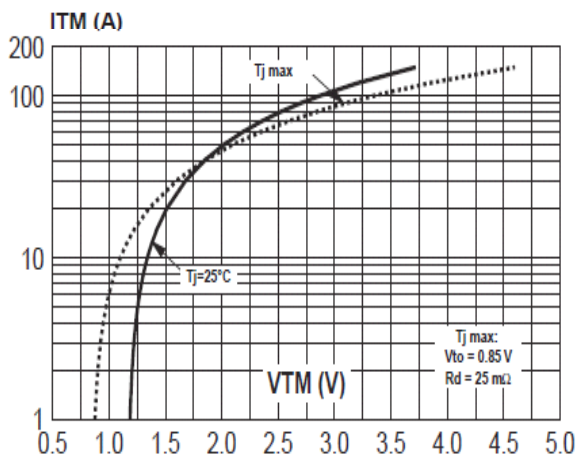
**Fig.2** Maximum on-state dissipation,  $P_{tot}$ , versus rms on-state current,  $I_{T(RMS)}$ , where  $\alpha =$  conduction angle.



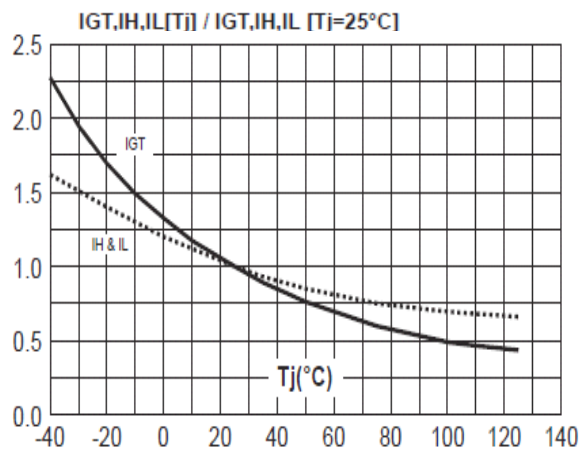
**Fig.3** Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10$ ms, and corresponding value of  $I^2t$ .



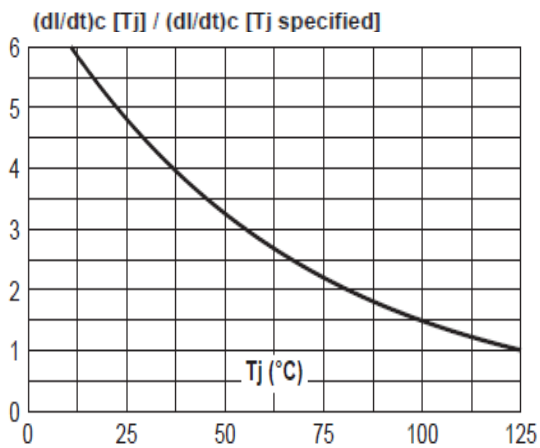
**Fig.4** Maximum permissible rms current  $I_{T(RMS)}$ , versus lead temperature  $T_{lead}$ .



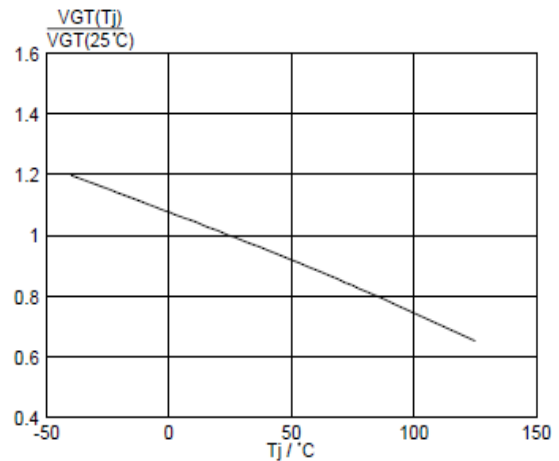
**Fig.5** Typical and maximum on-state characteristic.



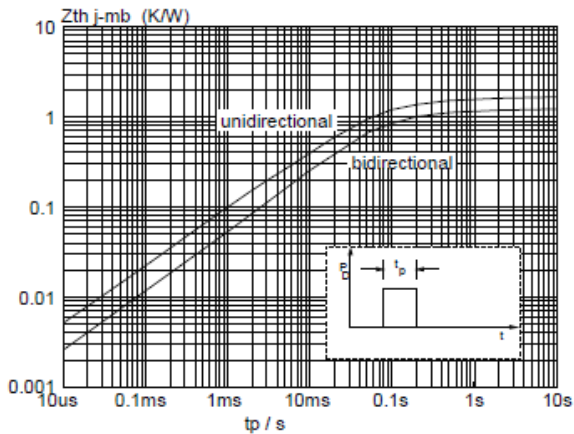
**Fig.6** Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).



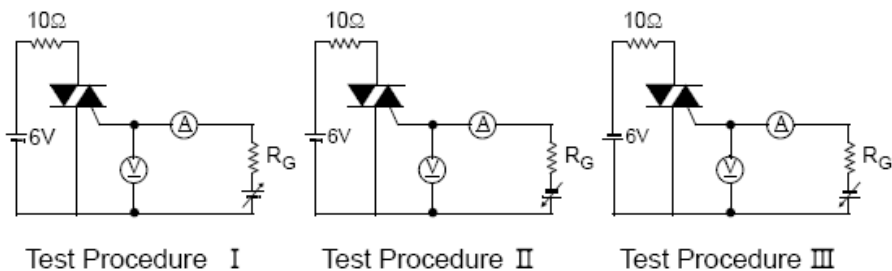
**Fig.7** Relative variation of critical rate of decrease of main current versus junction temperature.



**Fig.8** Normalised gate trigger voltage  $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$ , versus junction temperature T<sub>j</sub>.



**Fig.9** Transient thermal impedance Z<sub>th j-mb</sub>, versus pulse width t<sub>p</sub>.



**Fig.10** Gate Trigger Characteristics Test Circuit

**TO-220ISO Package Dimension**

