

## 2-line IPAD™, EMI filter and ESD protection for microphone

### Features

- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consumption: 1.0 mm x 1.45 mm
- Very thin package: 0.6 mm max
- High efficiency in ESD suppression
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging
- Lead-free and halogen-free package

### Complies with following standards

- IEC 61000-4-2 level 4, input and output pins
- IEC 61000-4-2 level 4 requirements
  - 8 kV (contact discharge)

or

- 15 kV (air discharge)

### Application

- Mobile phones

### Description

The EMIF02-MIC03M6 is a 2-line highly integrated device designed to suppress EMI/RFI noise in all systems exposed to electromagnetic interference.

This filter includes ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up to 8 kV on all pins.

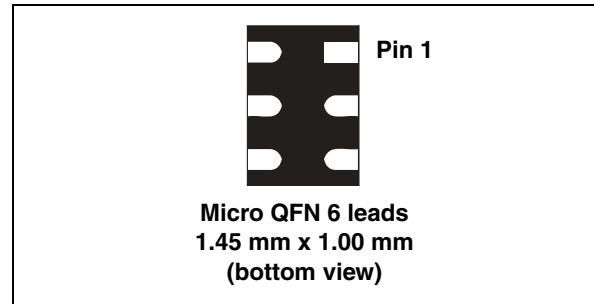


Figure 1. Pin configuration (top view)

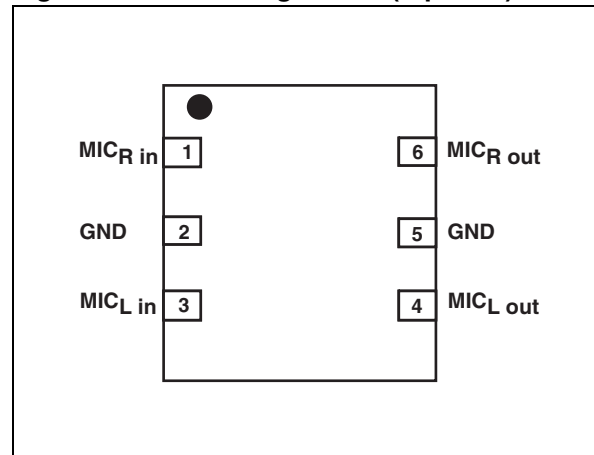
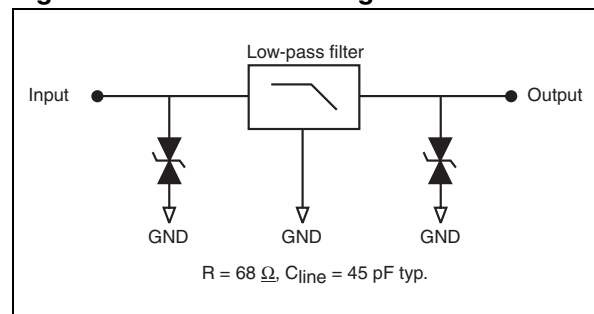


Figure 2. Basic cell configuration



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# 1 Characteristics

**Table 1. Absolute ratings<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>PP</sub>	ESD discharge IEC61000-4-2 contact discharge	8	kV
	ESD discharge IEC61000-4-2 air discharge <sup>(2)</sup>	15	
T <sub>j</sub>	Junction temperature	125	°C
T <sub>op</sub>	Operating temperature range	-40 to + 85	°C
T <sub>stg</sub>	Storage temperature range	-55 to +150	°C

- limiting values at T<sub>amb</sub> = 25 °C unless otherwise specified
- According to IEC61000-4-2 test conditions with ungrounded table top equipment set-up, PCB board on insulated plane (dimensions 25 x 25 mm<sup>2</sup>), 2 serial resistors of 470 kΩ to GND reference plane

**Table 2. Electrical characteristics (T<sub>amb</sub> = 25 °C)**

Symbol	Parameter								
V <sub>BR</sub>	Breakdown voltage								
I <sub>RM</sub>	Leakage current @ V <sub>RM</sub>								
V <sub>RM</sub>	Stand-off voltage								
V <sub>CL</sub>	Clamping voltage								
R <sub>d</sub>	Dynamic resistance								
I <sub>PP</sub>	Peak pulse current								
R <sub>I/O</sub>	Series resistance between Input & Output								
C <sub>line</sub>	Input capacitance per line								
Symbol	Test conditions					Min.	Typ.	Max.	Unit
V <sub>BR</sub>	I <sub>R</sub> = 1 mA					6	8		V
I <sub>RM</sub>	V <sub>RM</sub> = 3 V per line			500	nA				
R <sub>I/O</sub>	Tolerance ± 20%		68		Ω				
C <sub>line</sub> <sup>(1)</sup>	V <sub>R</sub> = 0 V, F = 1 MHz, V <sub>OSC</sub> = 30 mV		45		pF				

- Tolerance ± 20%

Figure 3. S21 attenuation measurement

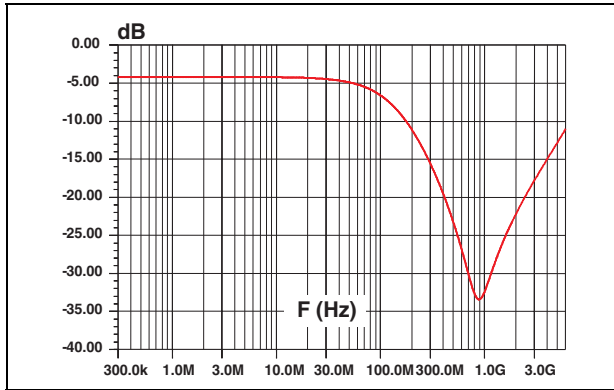


Figure 4. Analog cross talk measurements (MIC R / MIC L)

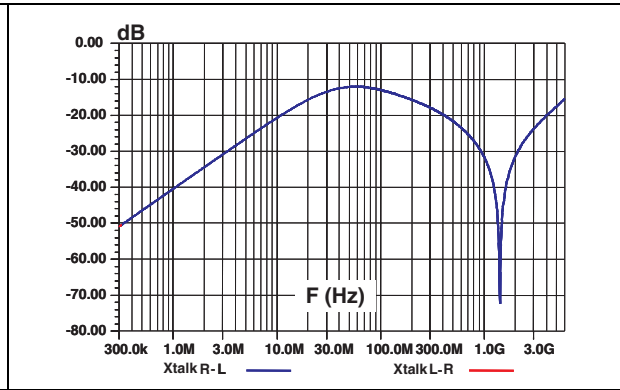


Figure 5. ESD response to IEC 61000-4-2 (+8 kV contact discharge) on MIC lines

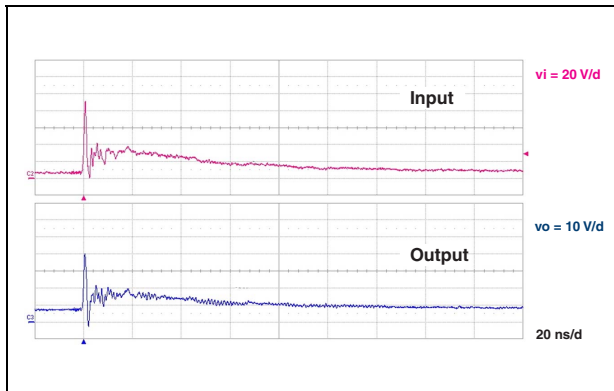
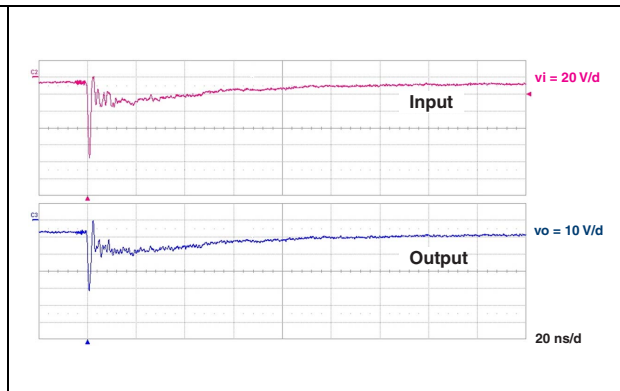
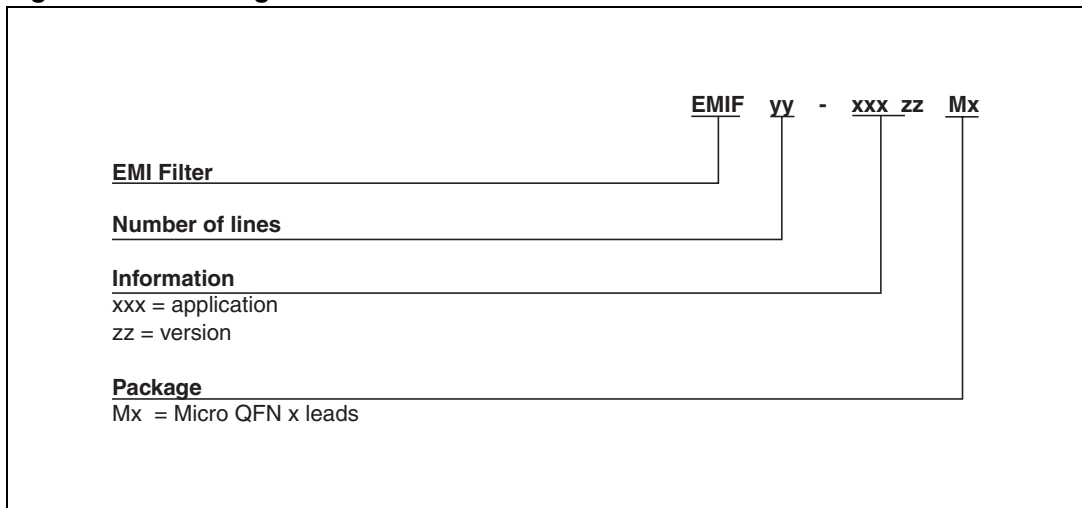


Figure 6. ESD response to IEC 61000-4-2 (-8 kV contact discharge) on MIC lines



## 2 Ordering information scheme

Figure 7. Ordering information scheme



### 3 Package information

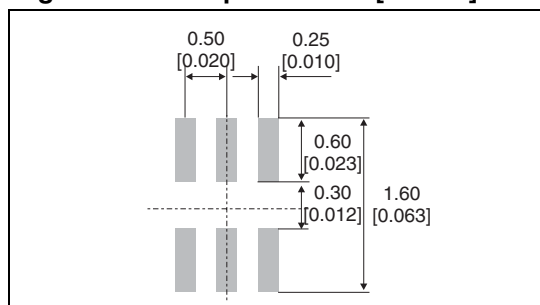
- Epoxy meets UL94, V0
- Lead-free packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Table 3. Micro QFN 1.45 x 1.00 6L dimensions**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D		1.45			0.057	
E		1.00			0.039	
e		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

**Figure 8. Footprint in mm [inches]**



**Figure 9. Marking**

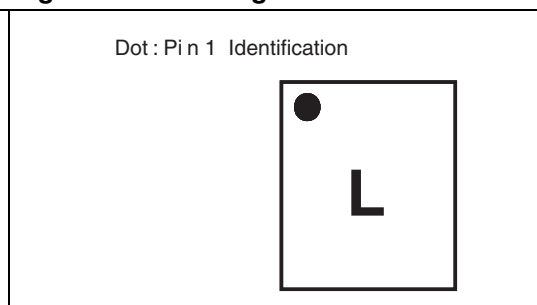
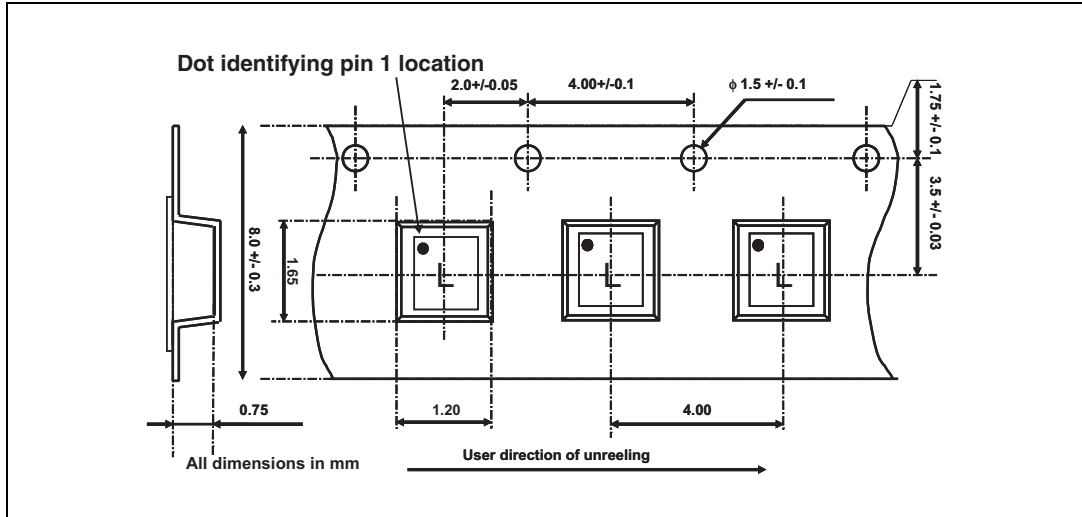


Figure 10. Tape and reel specification



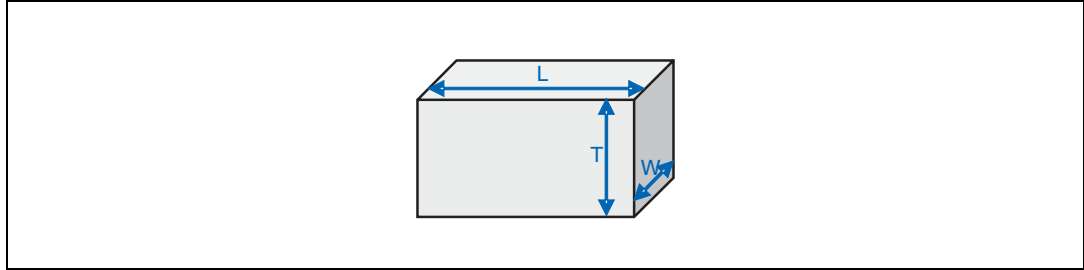
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

## 4 Recommendation on PCB assembly

### 4.1 Stencil opening design

1. General recommendation on stencil opening design
  - a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

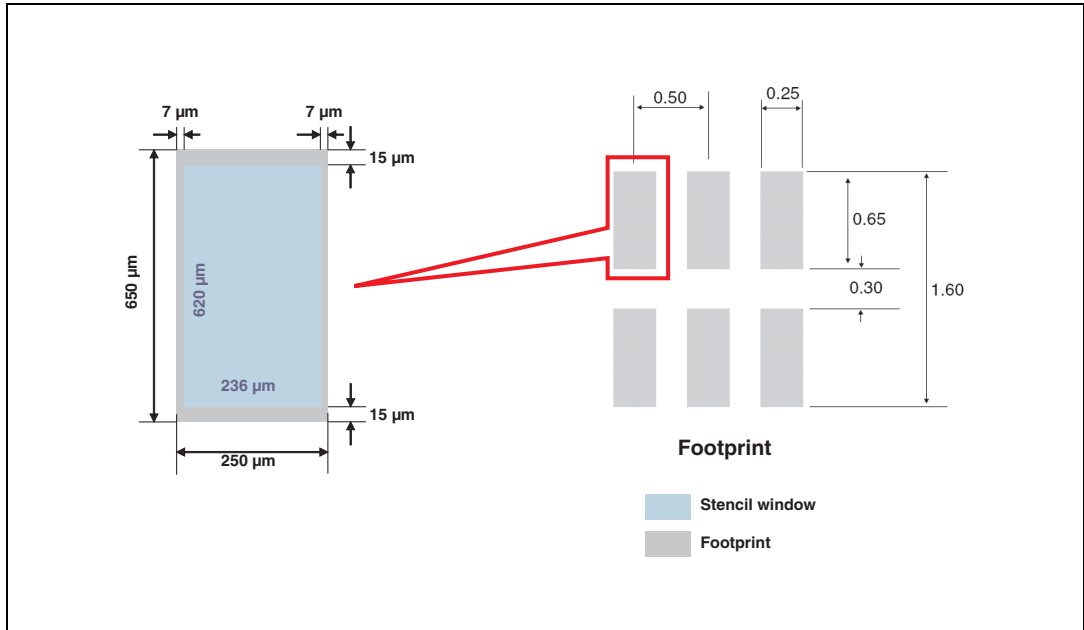
**Figure 11. Stencil opening dimensions**



- b) General design rule
  - Stencil thickness (T) = 75 ~ 125  $\mu\text{m}$
  - Aspect Ratio =  $\frac{W}{T} \geq 1.5$
  - Aspect Area =  $\frac{L \times W}{2T(L + W)} \geq 0.66$

2. Reference design
  - a) Stencil opening thickness: 100  $\mu\text{m}$
  - b) Stencil opening for leads: Opening to footprint ratio is 90%.

**Figure 12. Recommended stencil window position**



## 4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45  $\mu\text{m}$ .

## 4.3 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

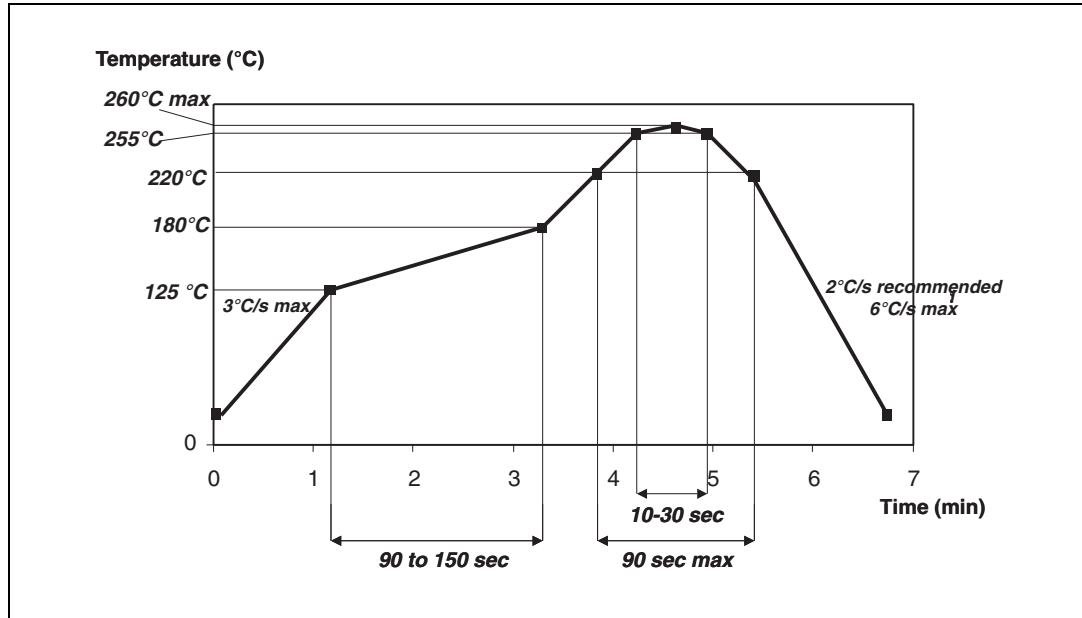
## 4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.



## 4.5 Reflow profile

Figure 13. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

## 5 Ordering information

**Table 4. Ordering information**

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-MIC03M6	L <sup>(1)</sup>	Micro QFN	2.2 mg	3000	Tape and reel (7")

1. The marking can be rotated by 90° to differentiate assembly location

## 6 Revision history

**Table 5. Document revision history**

Date	Revision	Changes
13-Feb-2008	1	Initial release
27-May-2011	2	Updated ECOPACK statement. Updated <i>n: IEC 61000-4-2 level 4 requirements on page 1</i> . Added note <i>2. on page 2</i> . Updated title <i>Figure 5.</i> and <i>Figure 6. on page 3</i> .

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