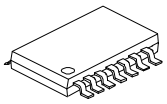
U74LVC34A

CMOS IC

HEX BUFFER



TSSOP-14

■ DESCRIPTION

The **U74LVC34A** is a hex buffer device providing, it provides the function Y = A.
This device has power-down protective circuit to prevent the device from destruction.

■ FEATURES

* Operation Voltage Range: 1.65~5.5V
* Low Power Dissipation
* 24mA Output Drive(V_{CC}=3.3V)
* High Noise Immunity
* Power Down Protection

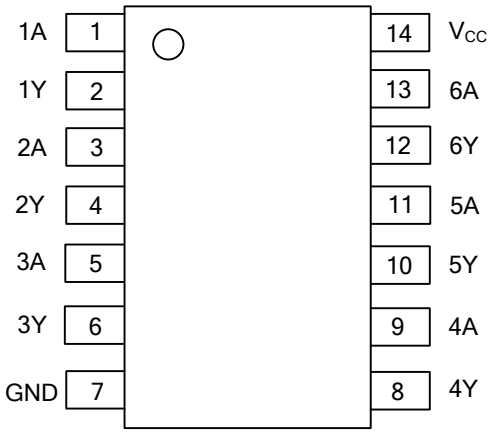
■ ORDERING INFORMATION

Ordering Number		Package	Packing
U74LVC34AL-P14-R	U74LVC34AG-P14-R	TSSOP-14	Tape Reel

U74LVC34AL-P14-R
- (1) Packing Type
- (2) Package Type
- (3) Lead Free

(1) R: Tape Reel
(2) P14: TSSOP-14
(3) G: Halogen Free, L: Lead Free

■ PIN CONFIGURATION

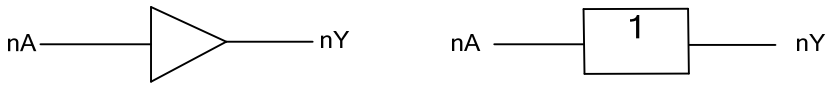


■ FUNCTION TABLE (Each Gate)

INPUT(A)	OUTPUT(Y)
L	L
H	H

Note: H=High level, L=Low Level

■ LOGIC SYMBOL (Each Gate)



IEC Logic Symbol

■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~6.5	V
Input Voltage	V_{IN}	-0.5~6.5	V
Output Voltage(active mode)	V_{OUT}	-0.5~V_{CC}+0.5	V
Output Voltage(power-down mode)	V_{OUT}	-0.5~6.5	V
Input Clamp Current(V_{IN}<0)	I_{IK}	-50	mA
Output Clamp Current(V_O<0)	I_{OK}	-50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Storage Temperature	T_{STG}	-65 ~ +150	℃

Note 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		85	℃
Input Transition Rise or Fall Rate	t_R / t_F	V_{CC} =1.8V±0.15V,2.5V±0.2V			20	ns/V
		V_{CC} =3.3V±0.3V			10	ns/V
		V_{CC} =5V±0.5V			5	ns/V

■ STATIC CHARACTERISTICS (T_A=-40~85℃)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Positive-going Input Threshold Voltage	V_{T+}	V_{CC} = 1.65~1.95V		0.65* V_{CC}			V
		V_{CC} = 2.3~2.7 V		1.7			
		V_{CC} = 2.7~3.6 V		2			
		V_{CC} = 4.5~5.5 V		0.7* V_{CC}			
Negative-going Input Threshold Voltage	V_{T-}	V_{CC} = 1.65~1.95 V				0.35* V_{CC}	V
		V_{CC} = 2.3~2.7 V				0.7	
		V_{CC} = 2.7~3.6 V				0.8	
		V_{CC} = 4.5~5.5 V				0.3* V_{CC}	
High-Level Output Voltage	V_{OH}	V_{CC} = 1.65~5.5 V	I_{OH}=-100μA	V_{CC}-0.1			V
		V_{CC} = 1.65 V	I_{OH}=-4mA	1.2			
		V_{CC} = 2.3 V	I_{OH}=-8mA	1.9			
		V_{CC} = 3 V	I_{OH}=-16mA	2.4			
		V_{CC} = 3 V	I_{OH}=-24mA	2.3			
		V_{CC} = 4.5 V	I_{OH}=-32mA	3.8			
Low-Level Output Voltage	V_{OL}	V_{CC} = 1.65~5.5 V	I_{OL}=100μA			0.1	V
		V_{CC} = 1.65 V	I_{OL}=4mA			0.45	
		V_{CC} = 2.3 V	I_{OL}=8mA			0.3	
		V_{CC} = 3 V	I_{OL}=16mA			0.4	
		V_{CC} = 3 V	I_{OL}=24mA			0.55	
		V_{CC} = 4.5 V	I_{OL}=32mA			0.55	
Input Leakage Current	$I_{I(LEAK)}$	V_{IN}=5.5V or GND, V_{CC} = 3.6V				±1	μA
Power OFF leakage current	I_{OFF}	V_{IN} or V_O =5.5V, V_{CC} = 0 V				±10	μA
Quiescent Supply Current	I_Q	V_{IN}=5.5 or GND, I_{OUT}=0 V_{CC} = 1.65 ~ 5.5 V				10	μA
Additional Quiescent Supply Current	Δ I_Q	One input at V_{CC}- 0.6V, other inputs at V_{CC} or GND V_{CC} = 3 ~ 5.5 V				500	μA
Input Capacitance	C_I	V_{IN}=V_{CC} or GND, V_{CC} = 3.3 V			3.5		pF

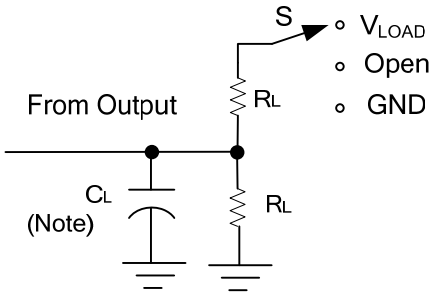
■ DYNAMIC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Propagation delay from input (nA or nB) to output(nY)	t_{PLH} / t_{PHL}	V_{CC}=1.8±0.15V	C_L=15pF, RL=1MΩ		2		9.9	ns
		V_{CC}=2.5±0.2V			1.5		6	
		V_{CC}=3.3±0.3V			1		3.5	
		V_{CC}=5±0.5V			1		2.9	
		V_{CC}=1.8±0.15V	C_L=30pF	RL=1kΩ	3.2		8.6	
		V_{CC}=2.5±0.2V		RL=500Ω	1.5		4.4	
		V_{CC}=3.3±0.3V	C_L=50pF, RL=500Ω		1.5		4.1	
		V_{CC}=5±0.5V			1		3.2	

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	V_{CC}=1.8V	f=10MHz		16		pF
		V_{CC}=2.5V			16		
		V_{CC}=3.3V			16		
		V_{CC}=5V			18		

■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

Note: C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	t_R, t_F	V_M	V_{LOAD}	C_L	R_L	$V_\triangle$
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	15pF	1MΩ	0.15V
					30 pF	1KΩ	
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2* V_{CC}	15pF	1MΩ	0.15V
					30 pF	500Ω	
3.3V±0.3V	3 V	≤2.5ns	1.5V	6V	15pF	1MΩ	0.3V
					50 pF	500Ω	
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2* V_{CC}	15pF	1MΩ	0.3V
					50 pF	500Ω