ePV6200

VFD Controller

Version 1.2

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Version History

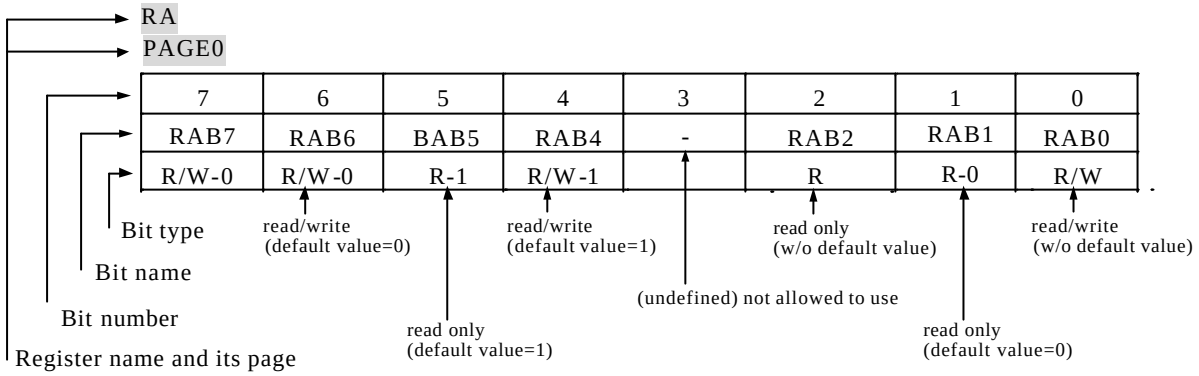
Specification Revision History		
Version	Content	Release Date
ePV6200		
1.0	Initial version	2004/3/30
1.1	revise error describe	2004/04/06

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. There are some undefined bits in the registers. The values in these bits are unpredicted. These bits are not allowed to use. We use the symbol "-" in the spec to recognize them.

2. You will see some names for the register bits definitions. Some name will be appeared very frequently in the whole spec. The following describes the meaning for the register's definitions such as bit type, bit name, bit number and so on.



I. General Description

The ePV6200 is an 8-bit RISC type VFD controller with low power, high speed CMOS technology. This integrated single chip has an on_chip watchdog timer (WDT), one time programming ROM (OTP), data RAM, programmable real time clock/counter, internal interrupt, power down mode, built-in four-wire SPI, IR detector and high voltage output for VFD application.

II. Feature

CPU

- Operating voltage : 2.2V~5.5V at main CLK less then 3.582MHz.
  Main CLK(Hz):3.582M ~ 17.91M
- 4k x 13 on chip Program ROM.
- 256 x 8 on chip data RAM
- 16 level stack for subroutine nesting
- 8-bit real time clock/counter (TCC)
- 8-bit counters : COUNTER1,COUNTER3,COUNTER4,COUNTER5
- 16-bit counters : COUNTER2
- On-chip watchdog timer (WDT)
- 99.9% single instruction cycle commands
- Four modes (Main clock can be programmed from 447.829k to 17.91MHz generated by internal PLL)

Mode	CPU status	Main clock	32.768kHz clock status
Sleep mode	Turn off	Turn off	Turn off
Idle mode	Turn off	Turn off	Turn on
Green mode	Turn on	Turn off	Turn on
Normal mode	Turn on	Turn on	Turn on

- 8 level Normal mode frequency : 447.829K , 895.658K , 1.791M , 3.582M , 7.165M , 10.747M , 14.331M , 17.91MHz..
- Input port interrupt function
- 12 interrupt source , 5 external (IR , INT1~INT4), 8 internal(SPI,TCC,COUNTER1~5)
- Dual clocks operation (Internal PLL main clock , External 32.768KHz)

SPI

- Serial interface for Clock, Data Input, Data Output, Strobe pins.

GPIO

- GPIO 9 Port(8 bit) : general purpose input/output; LED output
- GPIO C port(8 bit) : general purpose input/output for switch and key scanning(12x4 matrixs)

VFD

- Many display modes. (9-segment & 19-digit to 20-segment & 8-digit)
- Many display modes, can be programmed
- No external resistor necessary for driver outputs.(P-ch open-drain + pull-down resistor output)

POR

- 2.0V Power-on voltage detector reset

PACKAGE

- 52-pin die or 52-pin QFP

III. Application

DVD-R/W, DVD Recorder, DVD combo VFD Controller

V. Functional Block Diagram

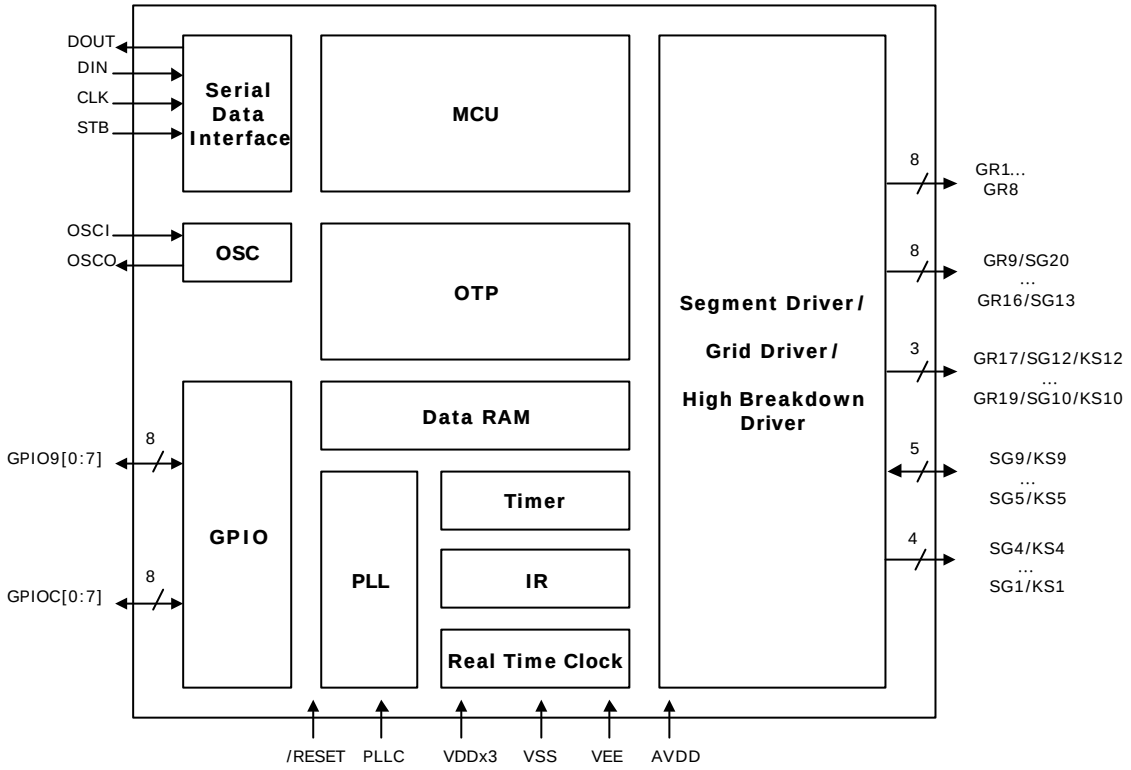


Fig.2a Block diagram

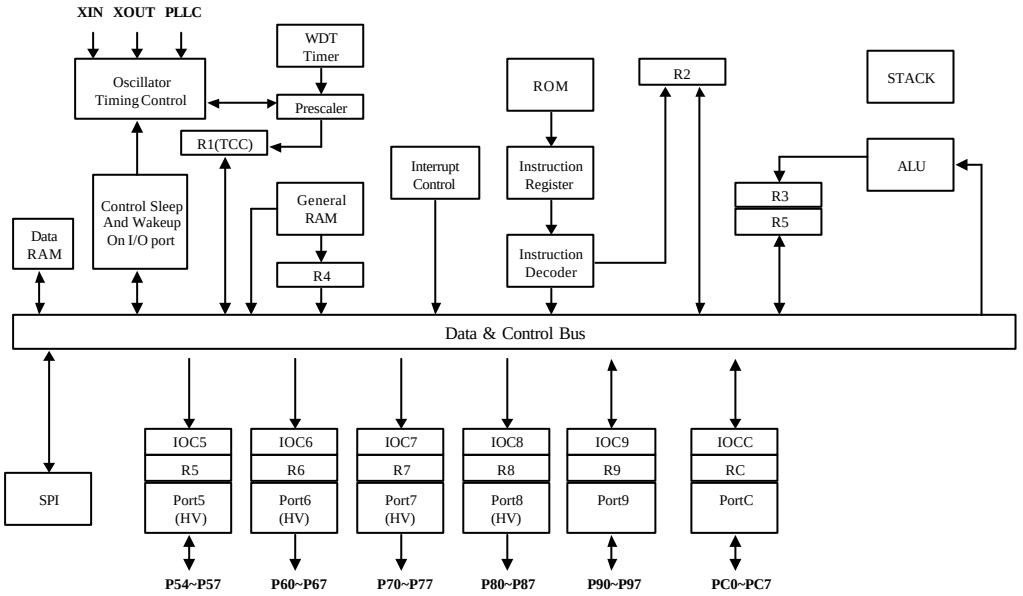


Fig.2b Block diagram

Port	HV	Port	HV	Port	HV
-		P60	SG5/KS5	P70	GR16/SG13
-		P61	SG6/KS6	P71	GR15 SG14
-		P62	SG7/KS7	P72	GR14/SG15
-		P63	SG8/KS8	P73	GR13/SG16
P54	SG1/KS1	P64	SG9/KS9	P74	GR12/SG17
P55	SG2/KS2	P65	GR19/SG10/KS10	P75	GR11/SG18
P56	SG3/KS3	P66	GR18/SG11/KS11	P76	GR10/SG19
P57	SG4/KS4	P67	GR17/SG12/KS12	P77	GR9/SG20

Port	HV	Port	GPIO	Port	GPIO
P80	GR8	P90	GPIO90/LED0/IR	PC0	GPIOC0/Key1
P81	GR7	P91	GPIO91/LED1/INT1	PC1	GPIOC1/Key2
P82	GR6	P92	GPIO92/LED2/INT2	PC2	GPIOC2/Key3
P83	GR5	P93	GPIO93/LED3/INT3	PC3	GPIOC3/Key4
P84	GR4	P94	GPIO94/LED4/INT4	PC4	GPIOC4/STB
P85	GR3	P95	GPIO95/LED5	PC5	GPIOC5/CLK
P86	GR2	P96	GPIO96/LED6	PC6	GPIOC6/DOUT
P87	GR1	P97	GPIO97/LED7	PC7	GPIOC7/ DIN

Table.2c Ports Mapping for HV and GPIO

VII. Functional Descriptions

VII.1 Operational Registers

Register configuration

	R PAGE registers		
Addr	R PAGE0	R PAGE1	R PAGE2
00	Indirect addressing		
01	TCC		
02	PC		
03	Page, Status		
04	RAM bank, RSR		
05	Port5 Output data	Program ROM page	
06	Port6 Output data		SPI data buffer
07	Port7 Output data		Counter1 data
08	Port8 Output data	Data RAM address	Counter2 LB data
09	Port9 I/O data	Data RAM data buffer	Counter2 HB data
0A	PLL, Main clock,WDTE		Counter3 data
0B		Port9 pull high	Counter4 data
0C	PortC I/O data	PortC pull high	Counter5 data
0D	Interrupt flag		
0E	Interrupt flag, Wake-up control		
0F	Interrupt flag		
10	16 bytes		
:	Common registers		
1F			
20	Bank0~Bank3		
:	Common registers		
3F	(32x8 for each bank)		

	IOC PAGE registers	
Addr	IOC PAGE0	IOC PAGE1
00		
01		
02		
03		
04		
05		Port5 switch
06		
07		
08		Clock source(CN2,CN1) Prescaler(CN2,CN1)
09	Port9 I/O control	Clock source(CN4,CN3) Prescaler(CN4,CN3)
0A		Clock source(CN5) Prescaler(CN5)
0B		
0C	PortC I/O control	PortC switch
0D	Interrupt mask	
0E	Interrupt mask	
0F	Interrupt mask	

VII.2 Operational Register Detail Description

R0 (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as indirect addressing pointer. Any instruction using R0 as register actually accesses data pointed by the RAM Select Register (R4).

Example:

```
Mov    A, @0x20        ;store a address at R4 for indirect addressing
Mov    0x04, A
Mov    A, @0xAA        ;write data 0xAA to R20 at bank0 through R0
Mov    0x00, A
```

R1 (TCC)

TCC data buffer. Increased by 16.384KHz or by the instruction cycle clock (controlled by CONT register).

Written and read by the program as any other register.

R2 (Program Counter)

The structure is depicted in Fig.3.

Generates 4k × 13 external ROM addresses to the relative programming instruction codes.

"JMP" instruction allows the direct loading of the low 10 program counter bits.

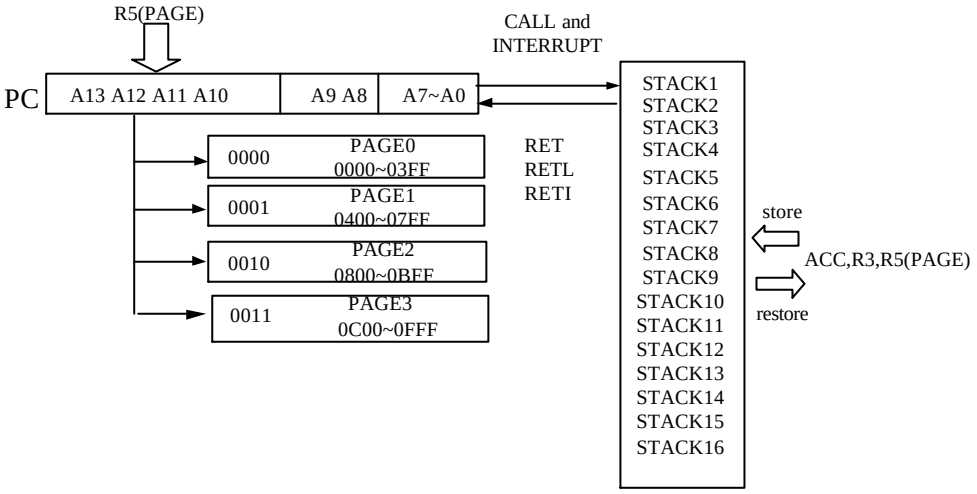
"CALL" instruction loads the low 10 bits of the PC, PC+1, and then push into the stack.

"RET" ("RETL k", "RETI") instruction loads the program counter with the contents at the top of stack.

"MOV R2, A" allows the loading of an address from the A register to the PC, and the ninth and tenth bits are cleared to "0".

"ADD R2,A" allows a relative address be added to the current PC, and contents of the ninth and tenth bits are cleared to "0".

Fig.3 Program counter organization



"TBL" allows a relative address added to the current PC, and contents of the ninth and tenth bits don't change.

The most significant bit (A10~A13) will be loaded with the contents of bit PS0~PS3 in the status register (R5 PAGE 1) upon the execution of a "JMP", "CALL", "ADD R2, A", or "MOV R2, A" instruction.

If an interrupt is triggered, PROGRAM ROM will jump to address 0x08 at page0. The CPU will store ACC, R3 status and R5 PAGE automatically, and they will be restored after instruction RETI.

R3 (Status, Page selection)

(Status flag, Page selection bits)

7	6	5	4	3	2	1	0
RPAGE1	**RPAGE0**	IOCPAGE	T	P	Z	DC	C
R/W-0	R/W-0	R/W-0	R	R	R/W	R/W	R/W

Bit 0(C) : Carry flag

Bit 1(DC) : Auxiliary carry flag

Bit 2(Z) : Zero flag

Bit 3(P) : Power down bit

Set to 1 during power on or by a "WDTC" command and reset to 0 by a "SLEP" command.

Bit 4(T) : Time-out bit

Set to 1 by the "SLEP" and "WDTC" command, or during power up and reset to 0 by WDT timeout.

EVENT	T	P	REMARK
WDT wake up from sleep mode	0	0	
WDT time out (not sleep mode)	0	1	
/RESET wake up from sleep	1	0	
Power up	1	1	
Low pulse on /RESET	x	X	x : don't care

Bit 5(IOCPAGE) : change IOC5 ~ IOCE to another page

0/1 ➔ IOC page0 / IOC page1

Bit 6, Bit 7 (RPAGE0 ~ RPAGE1) : change R5 ~ RC to another page

Please refer to VII.1 Operational registers for detail register configuration.

(RPAGE1,RPAGE0)	**R page # selected**
(0,0)	**R page 0**
(0,1)	**R page 1**
(1,x)	**R page 2**

R4 (RAM selection for common registers R20 ~ R3F))

(RAM selection register)

7	6	5	4	3	2	1	0
RB1	RB0	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
R/W-0	R/W-0	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 5 (RSR0 ~ RSR5) : Indirect addressing for common registers R20 ~ R3F

RSR bits are used to select up to 32 registers (R20 to R3F) in the indirect addressing mode.

Bit 6 ~ Bit 7 (RB0 ~ RB1) : Bank selection bits for common registers R20 ~ R3F

These selection bits are used to determine which bank is activated among the 4 banks for 32 register (R20 to R3F)..

Please refer to VII.1 Operational registers for details.

R5 (PORT5 Output data, Program page selection)

PAGE0 (PORT5 Output data register for HV)

7	6	5	4	3	2	1	0
P57	P56	P55	P54	-	-	-	-
W-0	W-0	W-0	W-0	-	-	-	-

PAGE1 (Program ROM page register)

7	6	5	4	3	2	1	0
AD9	AD8	-	-	PS3	PS2	PS1	PS0
R	R	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 3 (PS0 ~ PS3) : Program page selection bits

PS3	PS2	PS1	PS0	Program memory page (Address)
0	0	0	0	Page 0
0	0	0	1	Page 1
0	0	1	0	Page 2
0	0	1	1	Page 3

User can use PAGE instruction to change page to maintain program page by user. And the program page is maintained by EMC's complier. It will change user's program by inserting instructions within program.

R6 (PORT6 Output data)

PAGE0 (PORT6 Output data register for HV)

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

PAGE2 (SPI data buffer)

7	6	5	4	3	2	1	0
SPIB7	SPIB6	SPIB5	SPIB4	SPIB3	SPIB2	SPIB1	SPIB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (SPIB0 ~ SPIB7) : SPI data buffer

If you write data to this register, the data will write to SPIW register. If you read this data, it will read the data from SPIR register. Please refer to figure5

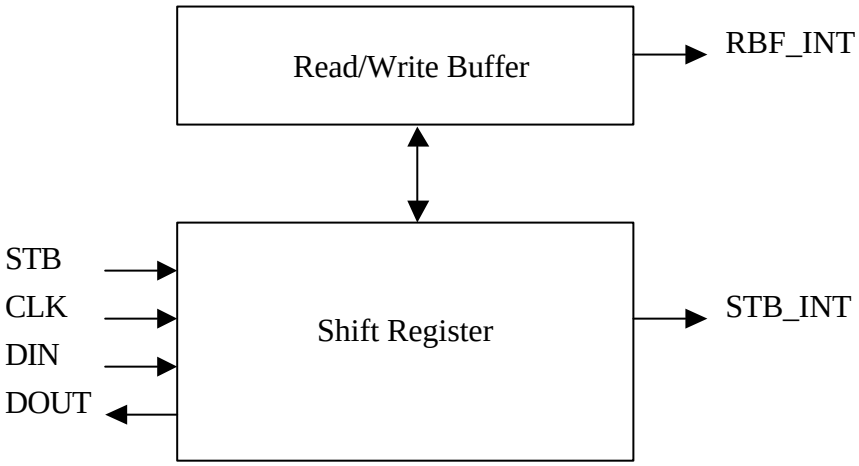
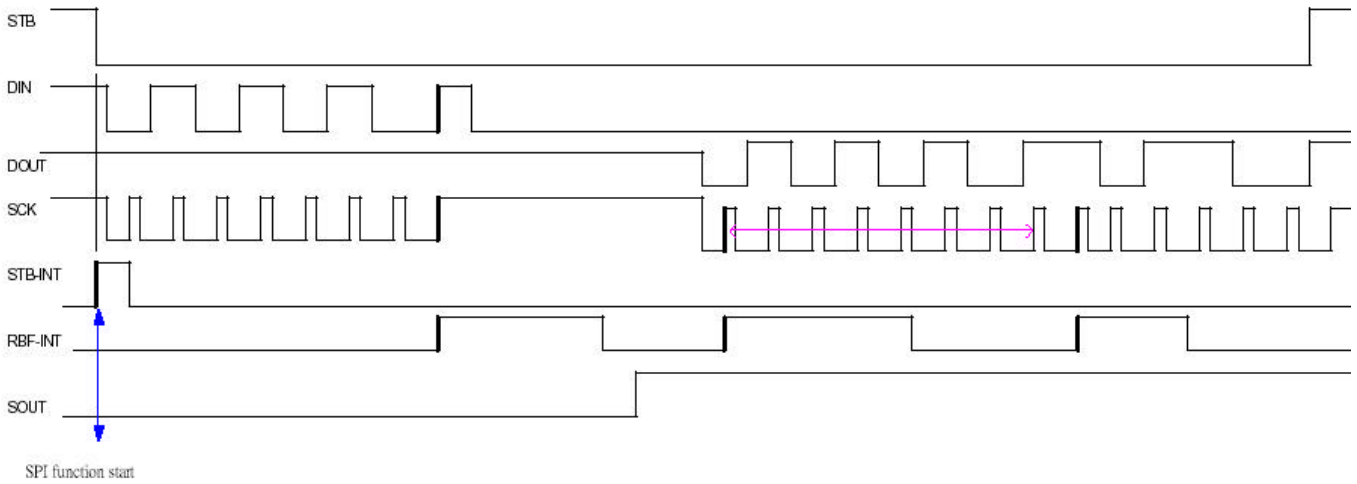


Fig.5



R7 (PORT7 Output data , Counter1 data

PAGE 0 (PORT7 Output data register for HV)

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70

PAGE 2 (Counter 1 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN17	CN16	CN15	CN14	CN13	CN12	CN11	CN10
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN10 ~ CN17) : Counter1's buffer that user can read and write.
Counter1 is a 8-bit up-counter with 8-bit prescaler that user can use R7 PAGE2 to preset and read the counter.(write ➔ preset) After a interruption , it will reload the preset value.

R8 (PORT8 Output data, Data RAM address) , Counter2_LB data

PAGE 0 (PORT8 Output data register for HV)

7	6	5	4	3	2	1	0
P87	P86	P85	P84	P83	P82	P81	P80
W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0

PAGE 1 (Data RAM address register)

7	6	5	4	3	2	1	0
RAM_A7	RAM_A6	RAM_A5	RAM_A4	RAM_A3	RAM_A2	RAM_A1	RAM_A0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (RAM_A0 ~ RAM_A7) : data RAM address

PAGE 2 (Counter2 Low byte data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN27	CN26	CN25	CN24	CN23	CN22	CN21	CN20
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CN20 ~ CN27) : Counter2_LB's buffer that user can read and write.
Counter2 is a 16-bit up-counter with 8-bit prescaler that user can use R8 PAGE2 to preset and read the counter.(write ➔ preset) After a interruption, it will reload the preset value.

R9 (PORT9 I/O data, Data RAM data buffer) ,Counter2_HB data

PAGE0 (PORT9 I/O data register)

7	6	5	4	3	2	1	0
P97	P96	P95	P94	P93	P92	P91	P90
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (P90 ~ P97) : 8-bit PORT9(0~7) I/O data register
User can use IOC register to define input or output each bit, and to define the pull high condition.
Bit 0:

1. P90: be defined as Input/Output
2. LED0: be defined as Output
3. IR Input: be defined as Input and IR is enable (when IOCF Bit7 is set to 1)

Bit 1~Bit4:

1. P91~P94: be defined as Input/Output
2. LED1~LED4: be defined as Output
3. INT1~INT4: be defined as Input

Bit 5~Bit7:

1. P95~P97: be defined as Input/Output
2. LED5~LED7: be defined as Output

PAGE 1 (Data RAM data register)

7	6	5	4	3	2	1	0
RAM_D7	RAM_D6	RAM_D5	RAM_D4	RAM_D3	RAM_D2	RAM_D1	RAM_D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (RAM_D0 ~ RAM_D7) : Data RAM' s data

PAGE 2 (Counter2 High byte data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

CN215	CN214	CN213	CN212	CN211	CN210	CN29	CN28
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 0 ~ Bit 7 (CN28 ~ CN215) : Counter2_HB's buffer that user can read and write.

Counter2 is a 16-bit up-counter with 8-bit prescaler that user can use R9 PAGE2 to preset and read the counter.(write ➔ preset) After a interruption, it will reload the preset value.

RA (PLL, Main clock selection, Watchdog timer),Counter3 data

PAGE0 (PLL enable bit, Main clock selection bits, Watchdog timer enable bit)

7	6	5	4	3	2	1	0
IDLE	PLLEN	CLK2	CLK1	CLK0	-	-	WDTEN
R/W-0	R/W-0	R/W-0	R/W-1	R/W-1			R/W-0

Bit 0(WDTEN) : Watch dog control bit

User can use WDTC instruction to clear watch dog counter. The counter 's clock source is 32768/2 Hz. If the prescaler assigns to TCC. Watch dog will time out by (1/32768)*2 * 256 = 15.616mS. If the prescaler assigns to WDT, the time of time out will be more times depending on the ratio of prescaler.

0/1 ➔ disable/enable

Bit 1~Bit 2 : Unused

Bit 3 ~ Bit 5 (CLK0 ~ CLK2) : MAIN clock selection bits

User can choose different frequency of main clock by CLK1 and CLK2. All the clock selection is list below.

PLLEN	CLK2	CLK1	CLK0	Sub clock	MAIN clock	CPU clock
1	0	0	0	32.768kHz	447.829kHz	447.829kHz (Normal mode)
1	0	0	1	32.768kHz	895.658kHz	895.658kHz (Normal mode)
1	0	1	0	32.768kHz	1.791MHz	1.791MHz (Normal mode)
1	0	1	1	32.768kHz	3.582MHz	3.582MHz (Normal mode)
1	1	0	0	32.768kHz	7.165MHz	7.165MHz (Normal mode)
1	1	0	1	32.768kHz	10.747MHz	10.747MHz (Normal mode)
1	1	1	0	32.768kHz	14.331MHz	14.331MHz (Normal mode)
1	1	1	1	32.768kHz	17.91MHz	17.91MHz (Normal mode)
0	Don' t care	Don' t care	Don' t care	32.768kHz	don' t care	32.768kHz (Green mode)

Bit 6(PLLEN) : PLL's power control bit which is CPU mode control register

0/1 ➔ disable PLL/enable PLL

If enable PLL, CPU will operate at normal mode (high frequency). Otherwise, it will run at green mode (low frequency, 32768 Hz).

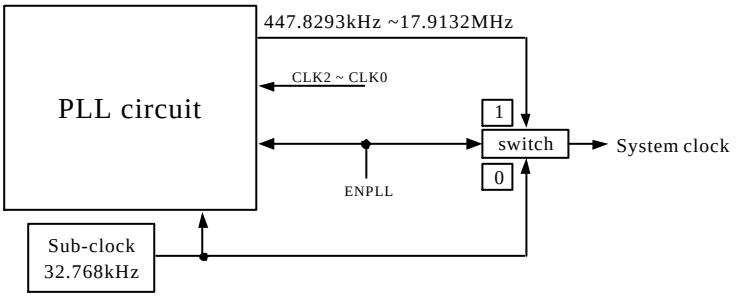


Fig.6 The relation between 32.768kHz and PLL

Bit 7(IDLE) : Sleep mode or IDLE mode control after using "SLEP" instruction.

0/1 ➔ SLEEP mode/IDLE mode.

This bit will decide SLEP instruction which mode to go.

The status after wake-up and the wake-up sources list as the table below.

Wakeup signal	SLEEP mode	IDLE mode
	RA(7,6)=(0,0) + SLEP	RA(7,6)=(1,0) + SLEP
TCC time out IOCF bit0=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
COUNTER1 time out IOCF bit1=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
COUNTER2 time out IOCF bit2=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
COUNTER3 time out IOCD bit0=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
COUNTER4 time out IOCD bit1=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
COUNTER5 time out IOCD bit2=1	No function	(1) Wake-up (2) Jump to SLEP next instruction
PORT90(IR function) IOCF bit3=1	Reset and jump to address 0	(1) Wake-up (2) Jump to SLEP next instruction
WDT time out	Reset and jump to address 0	(1) Wake-up (2) Next instruction
PORTC(0~3)(Key1~Key4) RE PAGE0 bit3 or bit4 or bit5 or bit6 = 1	Reset and Jump to address 0	(1) Wake-up (2) Jump to SLEP next instruction
PORT9(1~4) IOCF bit4 or bit5 or bit6 =1 or bit7=1	Reset and Jump to address 0	(1) Wake-up (2) Jump to SLEP next instruction

<Note> PORT90 's wakeup function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).

PORT91 's wakeup function is controlled by IOCF bit 4. It' s falling edge trigger.

PORT92~PORT94 's wakeup function is controlled by IOCF. They are falling edge trigger.

PORTC0~PORTC3' s wakeup function are controlled by RE PAGE0 bit 0 ~ bit 3. They are falling edge trigger.

PAGE 2 (Counter3 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN37	CN36	CN35	CN34	CN33	CN32	CN31	CN30
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN30 ~ CN37) : Counter3's buffer that user can read and write.

Counter3 is a 8-bit up-counter with 8-bit prescaler that user can use RA PAGE2 to preset and read the counter.(write ➔ preset) After a interruption , it will reload the preset value.

RB (PORT9 switches)

PAGE1 (PORT9, pull high)

7	6	5	4	3	2	1	0
PH97	PH96	PH95	PH94	PH93	PH92	PH91	PH90
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7(PH90 ~ PH97): PORT9 bit0~bit7 pull high control register

0 ➔ disable pull high function.

1 ➔ enable pull high function

PAGE2 (Counter4 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN47	CN46	CN45	CN44	CN43	CN42	CN41	CN40

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN40 ~ CN47) : Counter4's buffer that user can read and write.

Counter 4 is a 8-bit up-counter with 8-bit prescaler that user can use RB PAGE2 to preset and read the counter.(write ➔ preset) After a interruption , it will reload the preset value.

RC (PORTC I/O data , Counter5 data)

PAGE 0 I/O data buffer/serial signal

7	6	5	4	3	2	1	0
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

bit0~bit3:

1. PC0~PC3: be defined as Input/Output
2. KEY1~KEY4: be defined as Keyscan Input

bit4: 1. PC4 be defined as Input/Output 2. STB: Serial strobe signal

bit5: 1. PC5 be defined as Input/Output 2. CLK:Serial clock signal

bit6: 1. PC6 be defined as Input/Output 2. SDO : Serial data out

bit7: 1. PC7 be defined as Input/Output 2. SDI : Serial data in

PAGE1 (PORTC, pull high)

7	6	5	4	3	2	1	0
PHC7	PHC6	PHC5	PHC4	PHC3	PHC2	PHC1	PHC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (PHC0 ~ PHC7) : PORTC bit0~bit7 pull high control register

0 ➔ disable pull high function.

1 ➔ enable pull high function

PAGE2 (Counter5 data register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CN57	CN56	CN55	CN54	CN53	CN52	CN51	CN50
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 7 (CN50 ~ CN57) : Counter5's buffer that user can read and write.

Counter5 is a 8-bit up-counter with 8-bit prescaler that user can use RC PAGE2 to preset and read the counter.(write ➔ preset) After a interruption , it will reload the preset value.

RD (Interrupt Flag,)

PAGE 0 (Interrupt flagss register)

7	6	5	4	3	2	1	0
-	-	-	-	-	CNT5	CNT4	CNT3
-	-	-	-	-	R/W-0	R/W-0	R/W-0

"1" means interrupt request, "0" means non-interrupt

Bit 0(CNT3) : counter3 timer overflow interrupt flag

Set when counter3 timer overflows.

Bit 1(CNT4) : counter4 timer overflow interrupt flag

Set when counter4 timer overflows.

Bit 2(CNT5) : counter5 timer overflow interrupt flag

Set when counter5 timer overflows.

RE (Interrupt flags, Wake-up)

PAGE0 (Interrupt flags, Wake-up control bits)

7	6	5	4	3	2	1	0
-	RBF	-	STB	/WUPC3	/WUPC2	/WUPC1	/WUPC0
-	R/W-0	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 (/WUPC0) : PORTC0 wake-up control, 0/1 ➔ disable/enable PC0 pin wake-up function

Bit 1 (/WUPC1) : PORTC1 wake-up control, 0/1 ➔ disable/enable PC1 pin wake-up function
Bit 2 (/WUPC2) : PORTC2 wake-up control, 0/1 ➔ disable/enable PC2 pin wake-up function
Bit 3 (/WUPC3) : PORTC3 wake-up control, 0/1 ➔ disable/enable PC3 pin wake-up function
Bit 4(STB) : SPI data transfer starting interrupt. While the STB signal goes low, it will issue this interrupt.
Bit 5(-):-
Bit 6 (RBF) : SPI data transfer complete interrupt
If SPI's RBF signal has a rising edge signal (RBF set to "1" when transfer data completely), CPU will set this bit.
Bit 7(-) : -

RF (Interrupt flags)

PAGE0(Interrupt status register)

7	6	5	4	3	2	1	0
INT4	INT3	INT2	INT1	IR	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

"1" means interrupt request, "0" means non-interrupt

Bit 0(TCIF) : TCC timer overflow interrupt flag
Set when TCC timer overflows.

Bit 1(CNT1) : counter1 timer overflow interrupt flag
Set when counter1 timer overflows.

Bit 2(CNT2) : counter2 timer overflow interrupt flag
Set when counter2 timer overflows.

Bit 3(IR) : external INT pin interrupt flag
If PORT90 has a falling edge/ rising edge (controlled by CONT register) trigger signal, CPU will set this bit.

Bit 4(INT1) : external INT1 pin interrupt flag
If PORT91 has a falling edge trigger signal, CPU will set this bit.

Bit 5(INT2) : external INT2 pin interrupt flag
If PORT92 has a falling edge trigger signal, CPU will set this bit.

Bit 6 : (INT3) : external INT3 pin interrupt flag
If PORT93 has a falling edge trigger signal, CPU will set this bit.

Bit 7(INT4) : external IR interrupt flag
If PORT94 has a falling edge trigger signal, CPU will set this bit.

Trigger edge as the table

Signal	Trigger
TCC	Time out
COUNTER1	Time out
COUNTER2	Time out
COUNTER3	Time out
COUNTER4	Time out
COUNTER5	Time out
IR	Falling Rising edge
INT1	Falling edge
INT2	Falling edge
INT3	Falling edge
INT4	Falling edge

R10~R3F (General Purpose Register)

R10~R1F , R20~R3F (Banks 0 ~ 3) : all are general purpose registers.

VII.3 Special Purpose Registers

A (Accumulator)

Internal data transfer, or instruction operand holding

It's not an addressable register.

CONT (Control Register)

7	6	5	4	3	2	1	0
P90EG	INT	TS	RETBK	PAB	PSR2	PSR1	PSR0

Bit 0 ~ Bit 2 (PSR0 ~ PSR2) : TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC rate	WDT rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Bit 3(PAB) : Prescaler assignment bit

0/1 ➔ TCC/WDT

Bit 4(RETBK) : Return value backup control for interrupt routine

0/1 ➔ disable/enable

When this bit is set to 1, the CPU will store ACC,R3 status and R5 PAGE 1 automatically after an interrupt is triggered. And it will be restored after instruction RETI. When this bit is set to 0, the user need to store ACC, R3 and R5 PAGE 1 in user program.

Bit 5(TS) : TCC signal source

0 ➔ internal instruction cycle clock

1 ➔ 16.384kHz

Bit 6 (INT) : INT enable flag

0 ➔ interrupt masked by DISI or hardware interrupt

1 ➔ interrupt enabled by ENI/RETI instructions

Bit 7(P90EG) : interrupt edge type of P90

0 ➔ P90 's interruption source is a rising edge signal.

1 ➔ P90 's interruption source is a falling edge signal.

CONT register is readable (CONTR) and writable (CONTW).

TCC and WDT :

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or WDT only at the same time.

An 8 bit counter is available for TCC or WDT determined by the status of the bit 3 (PAB) of the CONT register.

See the prescaler ratio in CONT register.

Fig.17 depicts the circuit diagram of TCC/WDT.

Both TCC and prescaler will be cleared by instructions which write to TCC each time.

The prescaler will be cleared by the WDTC and SLEP instructions, when assigned to WDT mode.

The prescaler will not be cleared by SLEP instructions, when assigned to TCC mode.

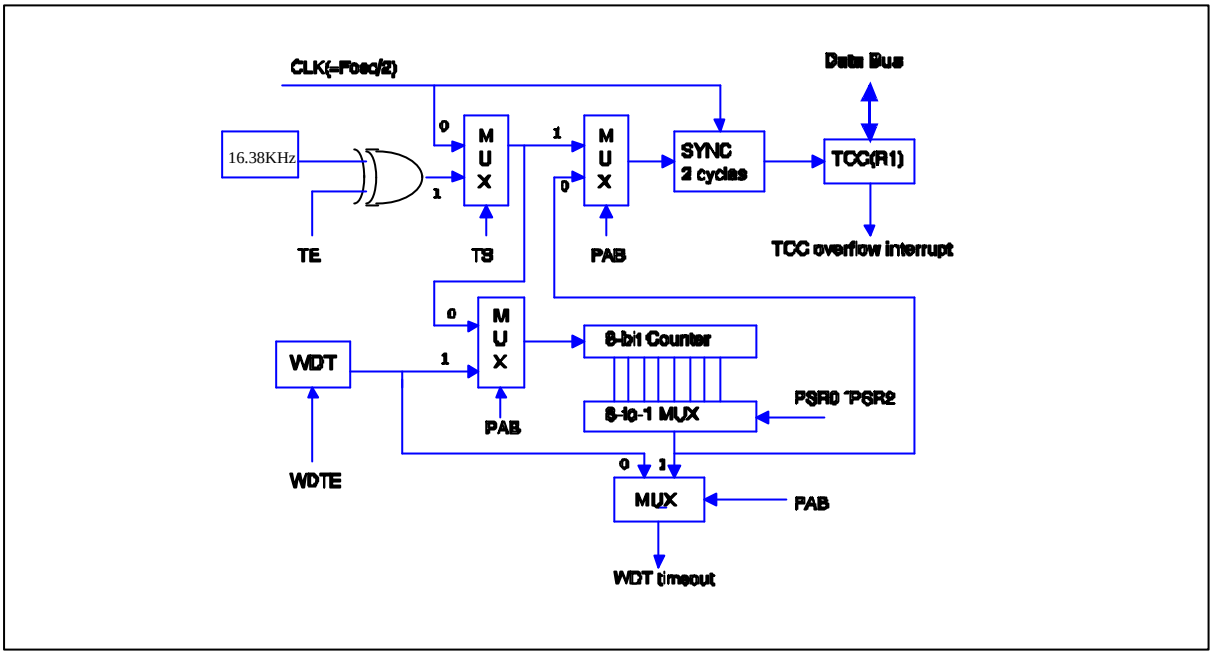


Fig.7 Block diagram of TCC WDT

IOC 5 (PORT5 switches)

Page 1

7	6	5	4	3	2	1	0
P57S	P56S	P55S	P54S				
R/W-0	R/W-0	R/W-0	R/W-0				

Bit 4~ Bit 7(P54S~P57S) : port5 I/O direction control register

0 ➔ put the relative I/O pin as output HV

1 ➔ put the relative I/O pin into high impedance

IOC8

PAGE1 (Clock source and prescaler for COUNTER1 and COUNTER2)

7	6	5	4	3	2	1	0
CNT2S	C2_PSC2	C2_PSC1	C2_PSC0	CNT1S	C1_PSC2	C1_PSC1	C1_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C1_PSC0 ~ C1_PSC2) : COUNTER1 prescaler ratio

C1_PSC2	C1_PSC1	C1_PSC0	COUNTER1
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT1S) : COUNTER1 clock source

0/1 ➔ 16.384kHz/system clock

Bit 4 ~ Bit 6 (C2_PSC0 ~ C2_PSC2) : COUNTER2 prescaler ratio

C2_PSC2	C2_PSC1	C2_PSC0	COUNTER2
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128

1	1	1	1:256

Bit 7(CNT2S) : COUNTER2 clock source

0/1 ➔ 16.384kHz/system clock

IOC9 (PORT9 I/O control , Clock source and prescaler for COUNTER3 and COUNTER4)

PAGE0 (PORT9 I/O control register)

7	6	5	4	3	2	1	0
IOC97	IOC96	IOC95	IOC94	IOC93	IOC92	IOC91	IOC90
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOC90 ~ IOC97) : PORT9(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (Clock source and prescaler for COUNTER3 and COUNTER4)

7	6	5	4	3	2	1	0
CNT4S	C4_PSC2	C4_PSC1	C4_PSC0	CNT3S	C3_PSC2	C3_PSC1	C3_PSC0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C3_PSC0 ~ C3_PSC2) : COUNTER3 prescaler ratio

C3_PSC2	C3_PSC1	C3_PSC0	COUNTER3
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT3S) : COUNTER3 clock source

0/1 ➔ 16.384kHz/system clock

Bit 4 ~ Bit 6 (C4_PSC0 ~ C4_PSC2) : COUNTER4 prescaler ratio

C4_PSC2	C4_PSC1	C4_PSC0	COUNTER4
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 7(CNT4S) : COUNTER4 clock source

0/1 ➔ 16.384kHz/system clock

IOCA

PAGE1 (Clock source and prescaler for COUNTER5)

7	6	5	4	3	2	1	0
-	-	-	-	CNT5S	C5_PSC2	C5_PSC1	C5_PSC0
-	-	-	-	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ Bit 2 (C5_PSC0 ~ C5_PSC2) : COUNTER5 prescaler ratio

C5_PSC2	C5_PSC1	C5_PSC0	COUNTER5
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32

1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3(CNT5S) : COUNTER5 clock source

0/1 ➔ 16.384kHz/system clock

IOCC (PORTC I/O control)

PAGE0 (PORTC I/O control register)

7	6	5	4	3	2	1	0
IOCC7	IOCC6	IOCC5	IOCC4	IOCC3	IOCC2	IOCC1	IOCC0
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

Bit 0 ~ Bit 7 (IOCC0 ~ IOCC7) : PORTC(0~7) I/O direction control register

0 ➔ put the relative I/O pin as output

1 ➔ put the relative I/O pin into high impedance

PAGE1 (PORTC switches)

7	6	5	4	3	2	1	0
PC7S	PC6S	PC5S	PC4S	-	-	-	-
R/W-1	R/W-1	R/W-1	R/W-1	-	-	-	-

Bit 4(PC4S) : Select STB or I/O PORTC4 pin

0 ➔ PC4 (I/O PORTC4) pin is selected

1 ➔ STB pin is selected

Bit 5(PC5S) : Select CLK or I/O PORTC5 pin

0 ➔ PC5 (I/O PORTC5) pin is selected

1 ➔ CLK pin is selected

Bit 6(PC6S) : Select DOUT or I/O PORTC6 pin

0 ➔ PC6 (I/O PORTC6) pin is selected

1 ➔ DOUT pin is selected (N-channel,Open-Drain)

Bit 7(PC7S) : Select DIN or I/O PORTC7 pin

0 ➔ PC7 (I/O PORTC7) pin is selected

1 ➔ DIN pin is selected

IOCD (Interrupt Mask, Prescaler of CN3 ~ CN5)

PAGE0 (Interrupt mask)

7	6	5	4	3	2	1	0
-	-	-	-	-	CNT5	CNT4	CNT3
-	-	-	-	-	R/W-0	R/W-0	R/W-0

Bit 0 ~ 3 : interrupt enable bit

0 ➔ disable interrupt

1 ➔ enable interrupt

IOCE (Interrupt mask)

PAGE0 (Interrupt mask)

7	6	5	4	3	2	1	0
-	RBF	-	STB	-	-	-	-
-	R/W-0	-	R/W-0	-	-	-	-

Bit 4(STB): STB goes LOW interrupt mask.

0/1 ➔ disable/enable interrupt

Bit 5 (-): -

0/1 ➔ disable/enable interrupt

Bit 6 (RBF) : SPI' s RBF interrupt mask

0/1 ➔ disable/enable interrupt

IOCF (Interrupt mask)

PAGE0(Interrupt mask register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

INT4	INT3	INT2	INT1	IR	CNT2	CNT1	TCIF
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Bit 0 ~ 7: interrupt enable bit

0 ➔ disable interrupt

1 ➔ enable interrupt

<Note> IOCF is the interrupt mask register. User can read and clear

The status after interrupt and the interrupt sources list as the table below.

Interrupt signal	IDLE mode	GREEN mode	NORMAL mode
	RA(7,6)=(1,0) + SLEP	RA(7,6)=(x,0) no SLEP	RA(7,6)=(x,1) no SLEP
TCC time out IOCF bit0=1 And "ENI"	(1) Wake-up (2) Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER1 time out IOCF bit1=1 And "ENI"	(1) Wake-up (2)Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER2 time out IOCF bit2=2 And "ENI"	(1) Wake-up (2) Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER3 time out IOCD bit0=1 And "ENI"	(1) Wake-up (2)Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER4 time out IOCD bit1=1 And "ENI"	(1) Wake-up (2)Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
COUNTER5 time out IOCD bit2=1 And "ENI"	(1) Wake-up (2)Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
INT1~4 IOCF bit4=1 or IOCF bit5=1 IOCF bit6 = 1 or IOCF bit7= 1 And “ENI	(1) Wake-up (2)Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
IR IOCF bit3= 1 And “ENI	(1) Wake-up (2)Interrupt (jump to address 8 at page0) (3) after RETI instruction, jump to SLEP Next instruction	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)
RBF	No function	Interrupt	Interrupt

IOCE bit6 = 1 And "ENI		(jump to address 8 at page0)	(jump to address 8 at page0)
STB IOCE bit4 = 1 And "ENI	No function	Interrupt (jump to address 8 at page0)	Interrupt (jump to address 8 at page0)

<Note> PORT90 's interrupt function is controlled by IOCF bit 3. It's falling edge or rising edge trigger (controlled by CONT register bit7).
PORT9(1~4) 's interrupt functions are controlled by IOCF bit (4,5,6,7). They are falling edge trigger.
STB interrupt source function is controlled by IOCE PAGE0 bit 4. It is falling edge trigger after the STB goes low.

VII.4 I/O Port

The I/O registers are bi-directional tri-state I/O ports. The I/O ports can be defined as "input" or "output" pins by the I/O control registers under program control. The I/O data registers and I/O control registers are both readable and writable. The I/O interface circuit is shown in Fig.8

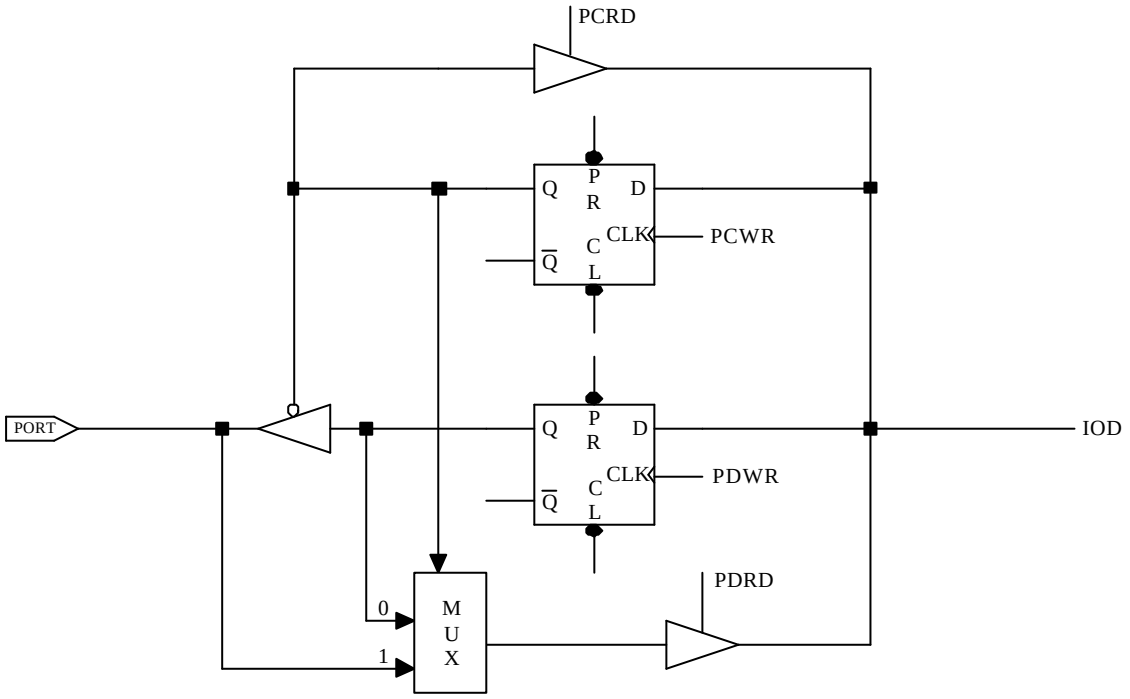


Fig.8 The circuit of I/O port and I/O control register

VII.5 RESET

The RESET can be caused by

(1) Power on reset

(2) WDT timeout. (if enabled and in GREEN or NORMAL mode)

(3) /RESET pin pull low

Once the RESET occurs, the following functions are performed.

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0".
- When power on, the upper 3 bits of R3 and the upper 2 bits of R4 are cleared.
- The Watchdog timer and prescaler counter are cleared.
- The Watchdog timer is disabled.
- The CONT register is set to all "1"
- The other register (bit 7 ~ bit 0) default values are as follows.

Operation registers :

Address	R register PAGE0	R register PAGE1	R register PAGE2	R register PAGE3	IOC register PAGE0	IOC register PAGE1
0x4	00xxxxxx					
0x5	0000xxxx	xxxx0000	00000000			
0x6	00000000		xxxxxxxx			
0x7	00000000	00000000	xxxxxxxx			
0x8	00000000	00000000	xxxxxxxx			00000000
0x9	00000000	xxxxxxxx	xxxxxxxx		11111111	00000000
0xA	00011xx0	xxxxxxxx	xxxxxxxx			00000000
0xB	00000000	00000000	xxxxxxxx		x1111111	x0000000
0xC	1011xxxx	00000000	xxxxxxxx		1111xxxx	1111xxxx
0xD	xxxxx000				xxxxx000	
0xE	X0000000				x000xxxx	
0xF	00000000				00000000	

VII.6 Wake-up

The controller has two types of sleep mode for power saving :

(1) SLEEP mode, RA(7) = 0 + "SLEP" instruction

The controller will turn off all the CPU and crystal. Other circuit with power control like key tone control or PLL control (which has enable register), user has to turn it off by software.

(2) IDLE mode, RA(7) = 1 + "SLEP" instruction.

The controller will turn off the CPU , but the crystal is continue oscillation

Wake-up from SLEEP mode

(1) WDT time out

(2) External interrupt

(3) /RESET pull low

All these cases will reset controller , and run the program at address zero. The status just like the power on reset. Be sure to enable circuit at case (1) or (2).

Wake-up from IDLE mode

(1)WDT time out

(2) external interrupt

(3) internal interrupt like counters

All these cases, user has to enable circuit before entering IDLE mode. After wake-up, all the register will keep values just like into "SLEP" instruction before.

At case (2) or (3), controller will wake up and jump to address 0x08 for interruption sub-routine. After finishing sub-routine ("RETI" instruction), program will jump to the next instruction from "SLEP" instruction.

VII.7 Interrupt

RD,RE,RF is the interrupt status register which records the interrupt request in flag bit. IOCF is the interrupt mask register. Global interrupt is enabled by ENI instruction and is disabled by DISI instruction. When one of the interrupts (when enabled) generated, will cause the next instruction to be fetched from address 008H. Once in the interrupt service routine, the source of the interrupt can be determined by polling the flag bits in the RF register.

The interrupt flag bit must be cleared in software before leaving the interrupt service routine and enabling interrupts to avoid recursive interrupts.

VII.8 Instruction Set

Instruction set has the following features:

(1) Every bit of any register can be set, cleared, or tested directly.

(2) The I/O register can be regarded as general register. That is, the same instruction can operates on I/O register.

The symbol "R" represents a register designator which specifies which one of the 64 registers (including operational registers and general purpose registers) is to be utilized by the instruction. Bits 6 and 7 in R4 determine the selected register bank. "b" represents a bit field designator which selects the number of the bit, located in the register "R", affected by the operation. "k" represents an 8 or 10-bit constant or literal value.

INSTRUCTION BINARY	HEX	MNEMONIC	OPERATION	STATUS AFFECTED	Instruction cycle
0 0000 0000 0000	0000	NOP	No Operation	None	1
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C	1
0 0000 0000 0010	0002	CONTW	A → CONT	None	1
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T,P	1
0 0000 0000 0100	0004	WDTC	0 → WDT	T,P	1
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None	1
0 0000 0001 0000	0010	ENI	Enable Interrupt	None	1
0 0000 0001 0001	0011	DISI	Disable Interrupt	None	1
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None	2
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC Enable Interrupt	None	2
0 0000 0001 0100	0014	CONTR	CONT → A	None	1
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None	1
0 0000 0010 0000	0020	TBL	R2+A → R2 bits 9,10 do not clear	Z,C,DC	2
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None	1
0 0000 1000 0000	0080	CLRA	0 → A	Z	1
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z	1
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C,DC	1
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C,DC	1
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z	1
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z	1
0 0010 00rr rrrr	02rr	OR A,R	A ∨ R → A	Z	1
0 0010 01rr rrrr	02rr	OR R,A	A ∨ R → R	Z	1
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z	1
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z	1
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z	1

0	0011	01rr	rrrr	03rr	XOR R,A	A ⊕ R → R	Z	1
0	0011	10rr	rrrr	03rr	ADD A,R	A + R → A	Z,C,DC	1
0	0011	11rr	rrrr	03rr	ADD R,A	A + R → R	Z,C,DC	1
0	0100	00rr	rrrr	04rr	MOV A,R	R → A	Z	1
0	0100	01rr	rrrr	04rr	MOV R,R	R → R	Z	1
0	0100	10rr	rrrr	04rr	COMA R	/R → A	Z	1
0	0100	11rr	rrrr	04rr	COM R	/R → R	Z	1
0	0101	00rr	rrrr	05rr	INCA R	R+1 → A	Z	1
0	0101	01rr	rrrr	05rr	INC R	R+1 → R	Z	1
0	0101	10rr	rrrr	05rr	DJZA R	R-1 → A, skip if zero	None	2 if skip
0	0101	11rr	rrrr	05rr	DJZ R	R-1 → R, skip if zero	None	2 if skip
0	0110	00rr	rrrr	06rr	RRCA R	R(n) → A(n-1) R(0) → C, C → A(7)	C	1
0	0110	01rr	rrrr	06rr	RRC R	R(n) → R(n-1) R(0) → C, C → R(7)	C	1
0	0110	10rr	rrrr	06rr	RLCA R	R(n) → A(n+1) R(7) → C, C → A(0)	C	1
0	0110	11rr	rrrr	06rr	RLC R	R(n) → R(n+1) R(7) → C, C → R(0)	C	1
0	0111	00rr	rrrr	07rr	SWAPA R	R(0-3) → A(4-7) R(4-7) → A(0-3)	None	1
0	0111	01rr	rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None	1
0	0111	10rr	rrrr	07rr	JZA R	R+1 → A, skip if zero	None	2 if skip
0	0111	11rr	rrrr	07rr	JZ R	R+1 → R, skip if zero	None	2 if skip
0	100b	bbrr	rrrr	0xxx	BC R,b	0 → R(b)	None	1
0	101b	bbrr	rrrr	0xxx	BS R,b	1 → R(b)	None	1
0	110b	bbrr	rrrr	0xxx	JBC R,b	if R(b)=0, skip	None	2 if skip
0	111b	bbrr	rrrr	0xxx	JBS R,b	if R(b)=1, skip	None	2 if skip
1	00kk	kkkk	kkkk	1kkk	CALL k	PC+1 → [SP] (Page, k) → PC	None	2
1	01kk	kkkk	kkkk	1kkk	JMP k	(Page, k) → PC	None	2
1	1000	kkkk	kkkk	18kk	MOV A,k	k → A	None	1
1	1001	kkkk	kkkk	19kk	OR A,k	A ∨ k → A	Z	1
1	1010	kkkk	kkkk	1Akk	AND A,k	A & k → A	Z	1
1	1011	kkkk	kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z	1
1	1100	kkkk	kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None	2
1	1101	kkkk	kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC	1
1	1110	0000	0001	1E01	INT	PC+1 → [SP] 001H → PC	None	1
1	1110	100k	kkkk	1E8k	PAGE k	K->R5(4:0)	None	1
1	1111	kkkk	kkkk	1Fkk	ADD A,k	k+A → A	Z,C,DC	1

VIII. Data RAM

There are a total of 256 bytes sizes at data RAM for ePV6200 chip. On the other hand, display Segment Data Buffers can be stored either in data RAM of 256 bytes sizes (00h~40h) or in common registers of bank2 and bank3(20h~3Fh).

Data RAM Address

00h~38h	57X8 Segment Data Buffers
39h~3Eh	6X8 Key Scanning Data Buffers
3Fh	SW data register
40h	LED data register

Common registers Address

20	Bank0~Bank3		
:	Common registers		
3F	(32x8 for each bank)		

Segment Data Buffers

This buffers store display RAM. The display RAM stores the data transmitted from an external device to the ePV6200 through the serial interface and is assigned addresses as follows, in units of 8 bits:

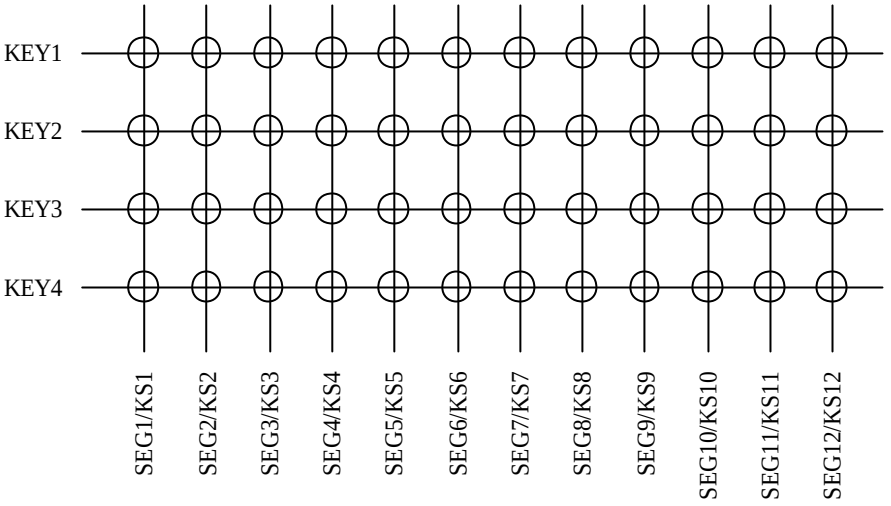
b0	b3	b4	b7
X X H_L		X X H_U	
Lower 4 bits		Higher 4 bits	

Only the lower 4 bits of the addresses assigned to SEG17 through SEG20 are valid and the higher 4 bits are ignored.

Display memory addresses table:

Seg1	Seg4	Seg8	Seg12	Seg16	Seg20	
00 HL	00 HU	01 HL	01 HU	02 HL		DIG1
03 HL	03 HU	04 HL	04 HU	05 HL		DIG2
06 HL	06 HU	07 HL	07 HU	08 HL		DIG3
09 HL	09 HU	0A HL	0A HU	0B HL		DIG4
0C HL	0C HU	0D HL	0D HU	0E HL		DIG5
0F HL	0F HU	10 HL	10 HU	11 HL		DIG6
12 HL	12 HU	13 HL	13 HU	14 HL		DIG7
15 HL	15 HU	16 HL	16 HU	17 HL		DIG8
18 HL	18 HU	19 HL	19 HU	1A HL		DIG9
1B HL	1B HU	1C HL	1C HU	1D HL		DIG10
1E HL	1E HU	1F HL	1F HU	20 HL		DIG11
21 HL	21 HU	22 HL	22 HU	23 HL		DIG12
24 HL	24 HU	25 HL	25 HU	26 HL		DIG13
27 HL	27 HU	28 HL	28 HU	29 HL		DIG14
2A HL	2A HU	2B HL	2B HU	2C HL		DIG15
2D HL	2D HU	2E HL	2E HU	2F HL		DIG16
30 HL	30 HU	31 HL	31 HU	32 HL		DIG17
33 HL	33 HU	34 HL	34 HU	35 HL		DIG18
36 HL	36 HU	37 HL	37 HU	38 HL		DIG19

Key Scanning Data Buffers:



The key matrix is of 12 x 4 configuration, as show upper.

The data of each key is stored as illustrated below, and is read by a read command, starting from the least significant bit.

KEY1….KEY4	KEY1….KEY4
SEG1/KS1	SEG2/KS2
SEG3/KS3	SEG4/KS4
SEG5/KS5	SEG6/KS6
SEG7/KS7	SEG8/KS8
SEG9/KS9	SEG10/KS10
SEG11/KS11	SEG12/KS12
b0 -- -- b3	b4 -- -- b7

Reading sequence

When the most significant bit of data (SEG12 b7) has been read, the least significant bit of the next data (SEG1 b0) is read.

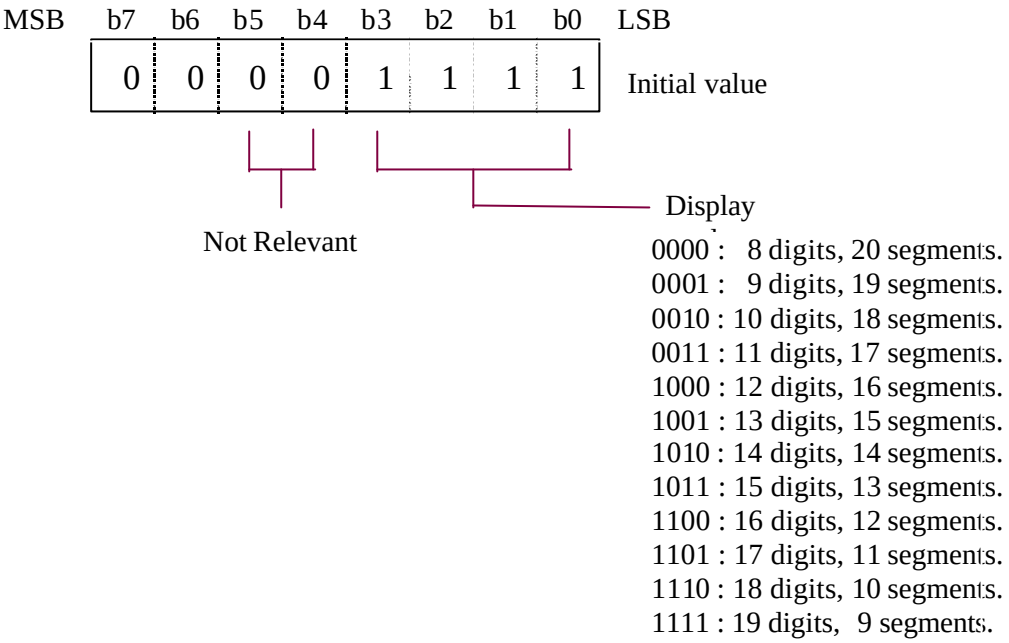
COMMANDS

A command sets the display mode and status of the VFD driver.
The first 1 byte (b0 to b7) inputted to the ePV6200 through the DIN pin after the STB pin has fallen is regarded as a command, and STB pin has fallen will occur interrupt event.
If STB is mode high while a command/data is transmitted, serial communication is initialized, and the command/data being t ransmitted is invalid (however, the command/data already transmitted remains valid).

(1) Display mode setting command [00]

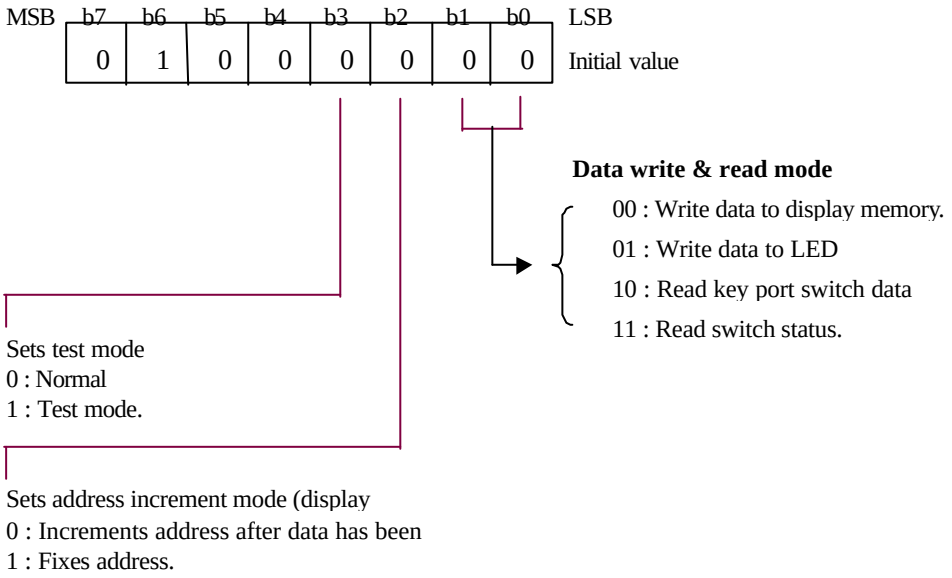
This command initializes the ePV6200, selects the number of segments and number of grids (1/8 to 1/19-duty, 9 segments to 20 segments).
When this command is executed, display is forcibly turned off, and key scanning is also stopped. To resume display, a display ON command must be executed. If the same mode is selected, however, nothing is performed.

When power is turned “ON”.
Display mode: 19-digit, 9-segment.



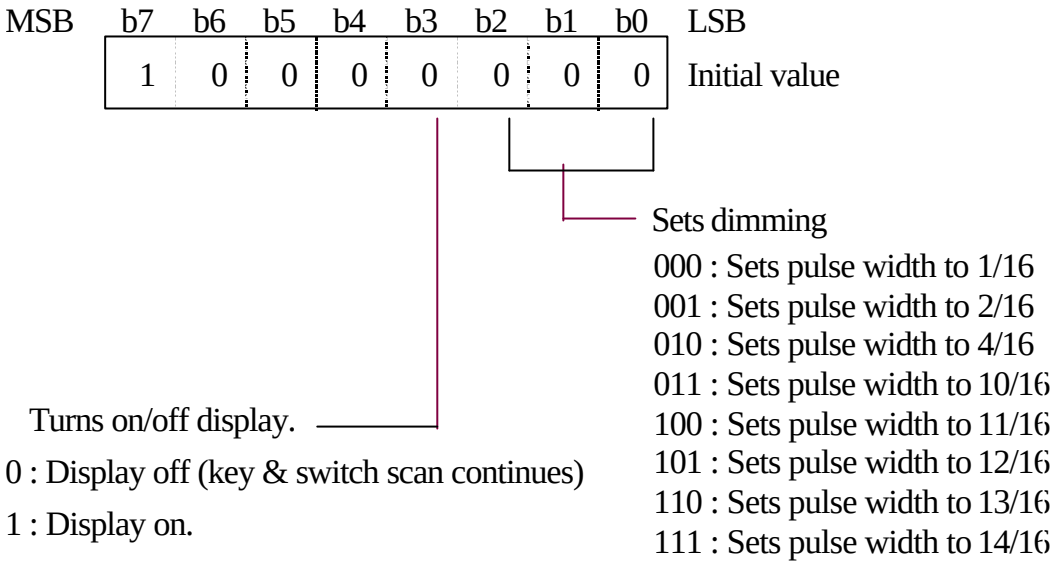
(2) Data setting command [01]

This command sets data write and data read modes.
When power is turned "ON".
Address increment mode: Address increment mode.
Mode setting: Normal operation mode.



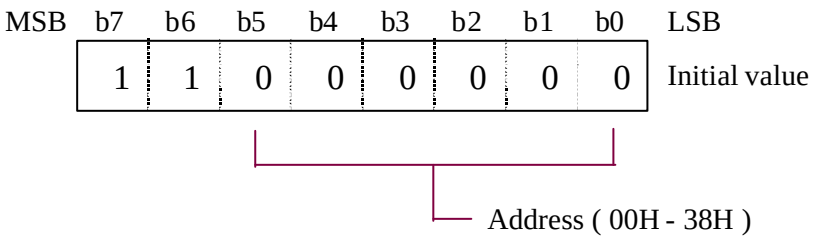
(3) Display control command [10]

When power is turned "ON".
4/64-pulse width is set and the display is turned off..
Key & switch scanning is stopped.



(4) Address setting command [11]

This command sets an address of the display memory
When power is turned "ON", the address is set to 00H.



If address 39H or higher is set, the data is ignored, until a correct address is set.

VIII. RC/Crystal OSC

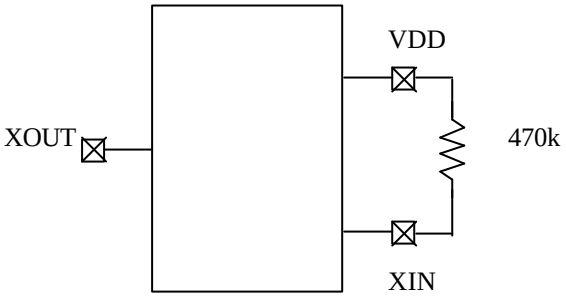
(i) General Description

This oscillator is designed for the ePV6200 chip as clock source.

(ii) Feature

- RC oscillator: 32.768K Hz
- Operating voltage: 2.2~5.5V.
- Operating temperature: -20°C ~ 70°C

(iii) Block Diagram



(iv) Pin Description

Name	I/O type	Description	Note
XIN	I	Crystal or RC oscillator connection pin	
XOUT	O	Crystal oscillator output pin	
VDD	-	Power supply (+) pin	
VSS	-	Power supply (-) pin	

(v) Electrical

(condition : VDD = 4.5 to 5.5V, Ta = -20°C to 70°C)

Parameters	Sym.	Min.	Typ.	Max.	Unit	Conditions
Starting oscillation voltage	Vs	-	2.0	3.2	V	
Stable time	Ts	-	5	10	clk	Vdd = 5.0V
Current consumption	Idd	-	2	3	mA	Vdd = 5.0V
Duty cycle		45	50	55	%	
Frequency/Voltage deviation	∂f/∂V	-	1	1.5	%	
Frequency/Temperature deviation	Δf	-	1	2	%	
Frequency v.s. Process deviation		-	±6	±10	%	

IX. Absolute Operation Maximum Ratings

Absolute maximum ratings (Ta = 25°C, Vss = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	V_{DD}	-0.5 to + 6	V
Driver supply voltage	V_{EE}	VDD +0.5 to VDD - 45	V
Logic input voltage	V_I	-0.5 to VDD +0.5	V
VFD driver output voltage	V_O	VEE -0.5 to VDD +0.5	V
LED driver output current	I_{O1}	+25	mA
VFD driver output current	I_{O2}	-40 (Grid) -15 (Segment)	mA
Operating ambient temperature	T_{opt}	-40 to +85	°C
Storage temperature	T_{stg}	-65 to +150	°C

IIX. DC Electrical Characteristic

(Ta = -20 to +70°C, V_{DD} = 4.5 to 5.5V, Vss = 0V, V_{EE} = V_{DD} - 45V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Digital Input Voltage High	V_{IH}	$0.8V_{DD}$	-	V_{DD}	V	GPIOB
Digital Input Voltage Low	I_{OL}	V_{SS}	-	$0.2V_{DD}$	V	
Schmitt Trigger Negative Going Threshold Voltage	V_{T-}	1.5	1.8	2.1		GPIOC, GPO9, CLK, STB, DIN and /RESET
Schmitt Trigger Positive Going Threshold Voltage	V_{T+}	2.9	3.2	3.5	V	
Pull Up Resister	R_{PU}	50	75	100	KΩ	GPIOC, GPO9, CLK, STB, DOUT, DIN , CRYXRC and /RESET @ VDD=5V ,
Digital Output Voltage High	V_{OH}	$0.8V_{DD}$	-	V_{DD}	V	DOUT, GPIOB, GPIOC
Digital Output Voltage Low	V_{OL}	V_{SS}	-	$0.2V_{DD}$	V	
Digital Output High Current	I_{OH1}	-2	-3	-4	mA	V_{OH}=2.4V / DOUT, GPIOC
Digital Output Low Current	I_{OL1}	2	3	4	mA	V_{OL}=0.4V / DOUT, GPIOC
Digital Output High Current	I_{OH2}	-15	-18	-20	mA	V_{OH}=2.4V / GPIO9
Digital Output Low Current	I_{OL2}	15	18	20	mA	V_{OL}=0.4V / GPIO9
HV Output Current	I_{OH1}	-3	-2.7	-2.4	mA	Vo = VDD –2V,(VDD=5V) SEG1/KS1 to SEG6/KS6, SG7 to SG11
HV Output Current	I_{OH2}	-15	-14	-12	mA	Vo = VDD –2V,(VDD=5V) GR1 to GR6, GR7/SG16 to GR11/SG12,
HV leakage current	I_{HVLEAK}	5	8	10	uA	Vo = VDD –40V, driver off
HV Output pull-down resistor	R_L	50	100	150	KΩ	Driver output
Power down current (SLEEP mode)	I_{SB1}		-	1	μA	All input and I/O pin at VDD, output pin floating, WDT disabled
Low clock current (GREEN mode)	I_{SB2}		35	50	μA	CLK=32.768KHz, All analog circuits disabled, All input and I/O pin at VDD, output
Low clock current (IDLE mode)	I_{SB3}		30	45	μA	CLK=32.768KHz, All analog circuits disabled, All input and I/O pin at VDD, output
Operating supply current (Normal mode)	I_{CC}		1.3	2	mA	/RESET=High, CLK=3.582MHz, All analog circuits disabled, output pin floating

IIX. AC Electrical Characteristic

CPU instruction timing (Ta = -20°C ~ 70°C, V_{DD}=5V, V_{SS}=0V)

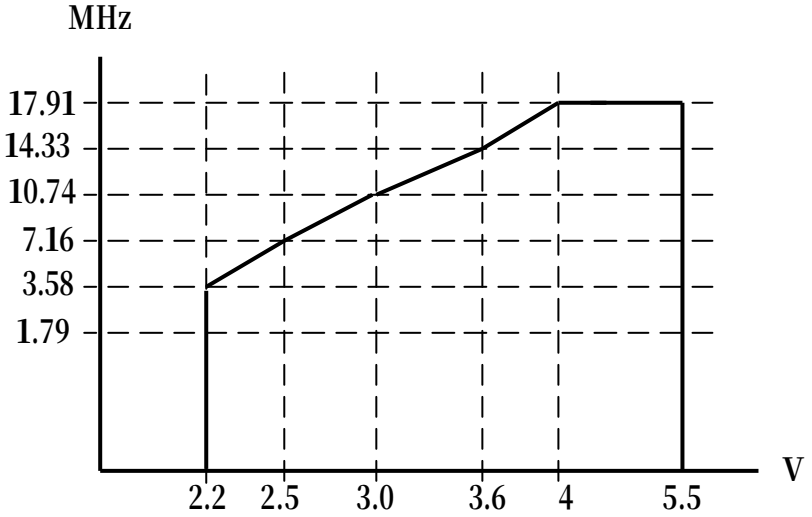
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input CLK duty cycle	Dclk		45	50	55	%
Instruction cycle time	Tins	32.768kHz 3.582MHz		60 550		us ns
Device delay hold time	Tdrh			16		ms
TCC input period	Ttcc	Note 1	(Tins+20)/N			ns
Watchdog timer period	Twdt	Ta = 25°C		16		ms

Note 1: N= selected prescaler ratio.

Timing characteristic (VDD=5V,Ta=+25°C)

Description		Symbol	Min	Typ	Max	Unit
Oscillator timing characteristic						
OSC start up	32.768kHz	Tosc	400		1500	ms
	3.579MHz PLL			5	10	us
SPI timing characteristic (CPU clock 3.58MHz and Fsco = 3.58Mhz /2)						
/SS set-up time		Tcss	560			ns
/SS hold time		Tcsh	250			
SCLK high time		Thi	250			ns
SCLK low time		Tlo	250			ns
SCLK rising time		Tr		15	30	ns
SCLK falling time		Tf		15	30	ns
SDI set-up time to the reading edge of SCLK		Tisu	25			ns
SDI hold time to the reading edge of SCLK		Tihd	25			ns
SDO disable time		Tdis			560	ns

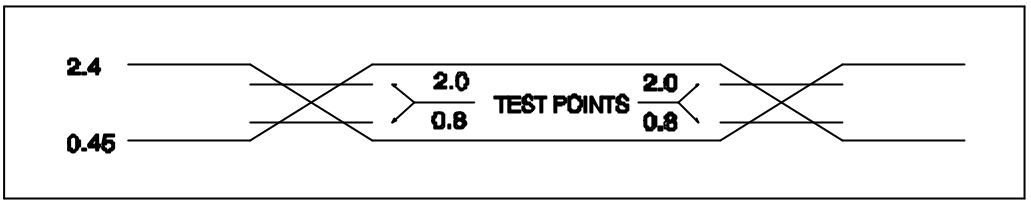
ePV6200 operation voltage(X axis → min VDD ; Y axis → main CLK):



IIIX. Timing Diagrams

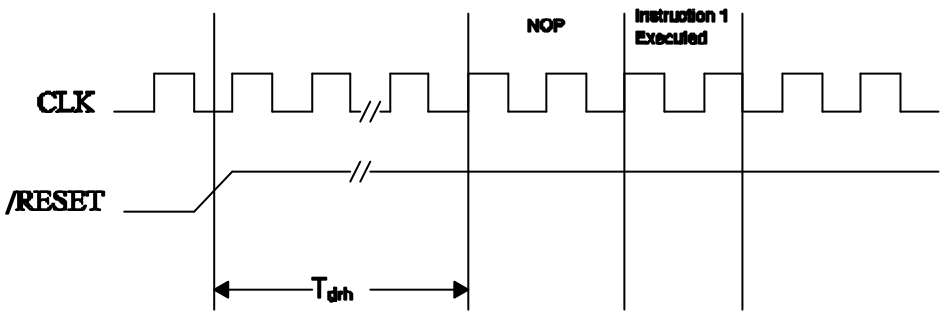
Fig. AC timing

AC Test Input/Output Waveform

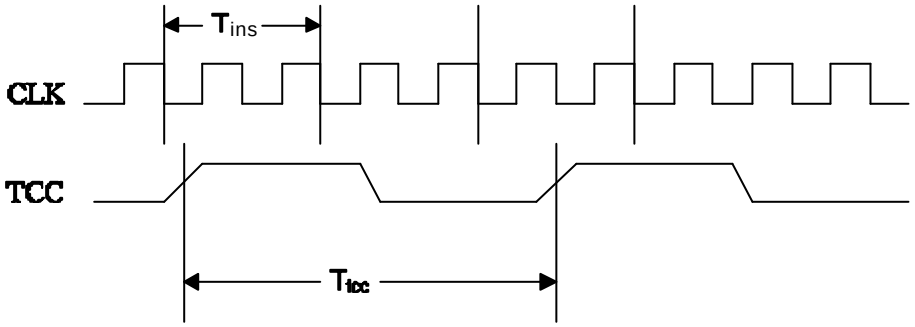


AC Testing: Input are driven at 2.4V for logic "1", and 0.45V for logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for logic "0".

RESET Timing

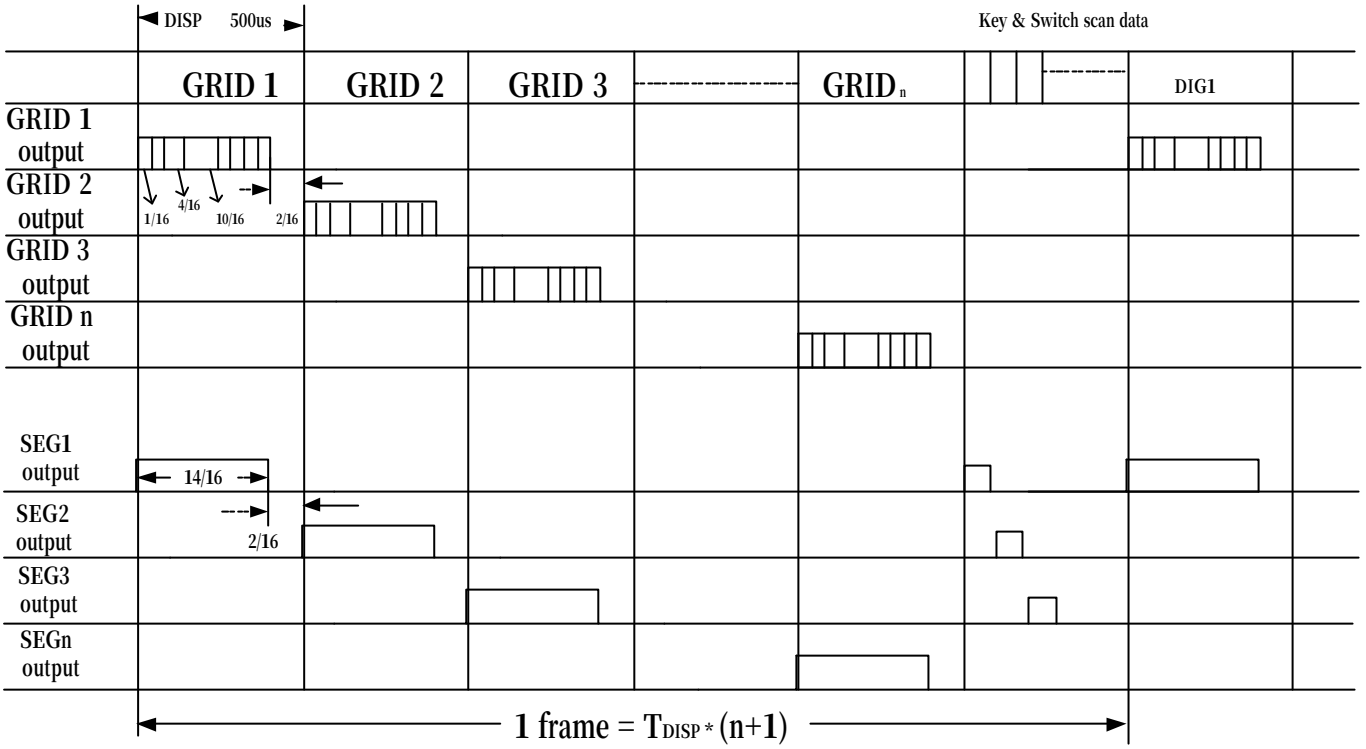


TCC Input Timing



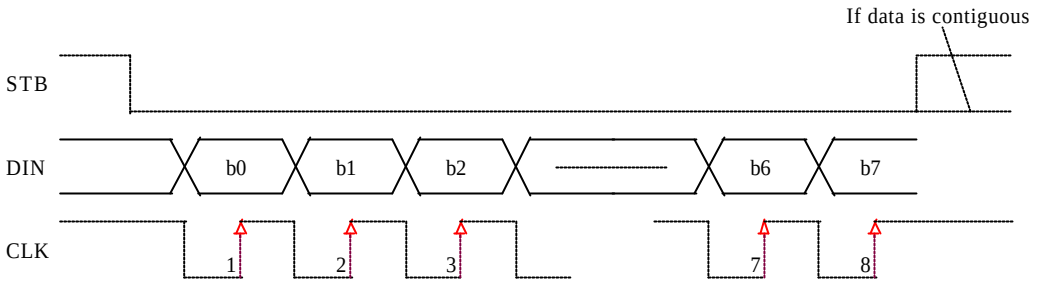
Key & Switch scanning and display timing

The key & switch scanning and display timing diagram is given below. One cycle of key & switch scanning consists of 2 frames. The data of the are 12 x 4 matrix is stored in the RAM.

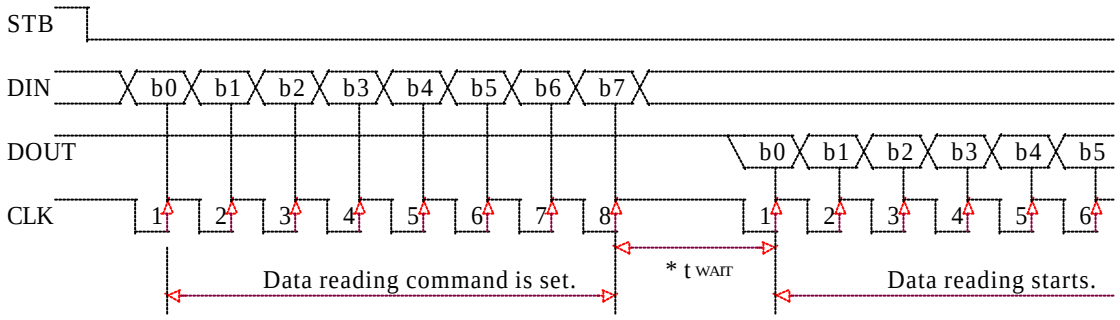


Serial or Parallel communication format

Reception (command/data write)



Transmission (data read)



When data is read, a wait time t_{WAIT} of is necessary between the rising of the eighth clock that has set the command and the falling of the first clock that has read the data.

The wait time is adjustable according to different application.

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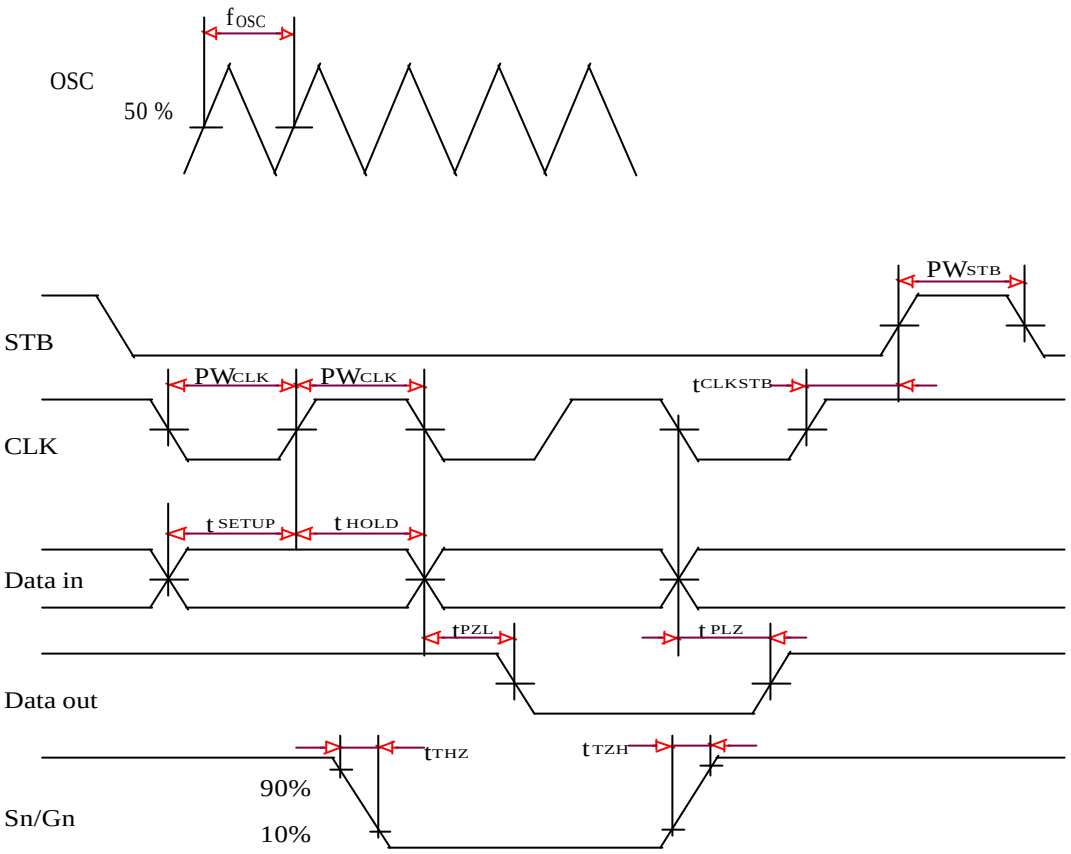
Switching characteristic waveform

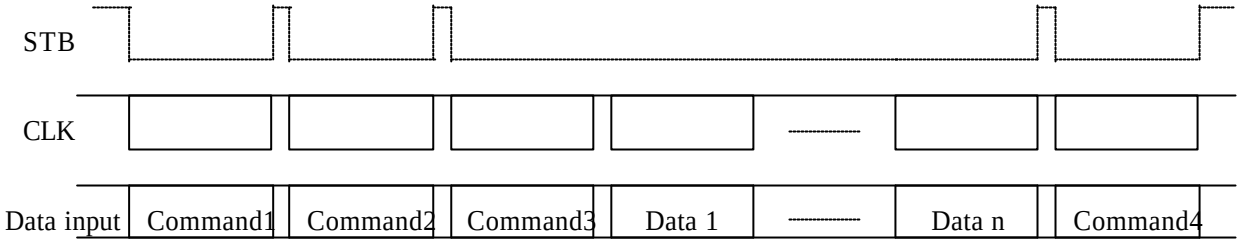


Switching characteristics (Ta = - 20 to + 70°C, VDD = 4.5 to 5.5V, VEE = VDD - 45V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Oscillation frequency	**t**OSC	-	32.768	-	KHz		
Propagation delay	**t**PLZ	-	-	300	ns	CLK→DOUT	
time	**t**PZL	-	-	100	ns	CL = 15pF, RL = 10KΩ	
Rise time	**t**TZH1			2	us	CL = 300pF	SEG1/KS1 to SEG4/KS4, SG5/KS5 to SG9/KS9.
	tTZH2			0.5	us		GR1 to GR8 GR9 /SG20 to GR9 /SG13, GR17/ SG12/KS12 to GR19 /SG10/KS10
Fall time	**t**THZ	100	110	120	us	CL = 300pF, SEGn, GRIDn	
Data input clock freq.	**f**max	-	1	1.25	MHz	Duty = 50 %, CLK	
Input capacitance	**C**I			15	pF		
Clock pulse width	**PW**CLK	400	500	-	ns		
Storbe pulse width	**PW**STB	0.8	1	-	us		
Data setup time	**t**SETUP	100	-	-	ns		
Data hold time	**t**HOLD	100	-	-	ns		
Clock-Strobe time	**t**CLKSTB	0.8	1	-	us	CLK↑→STB↑	
Wait time	**t**WAIT	-	3	-	us	CLK↑→CLK↑*	

Serial I/F sets display data sequence:

Updating display memory by incrementing address



Command 1: Display mode.

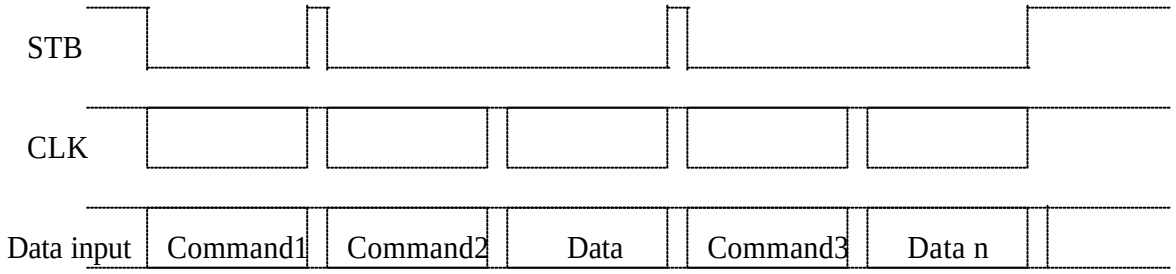
Command 2: Sets data.

Command 3: Sets address.

Data 1 to n: Transfers display data. (57 bytes max.)

Command 4: Controls display.

Updating specific address



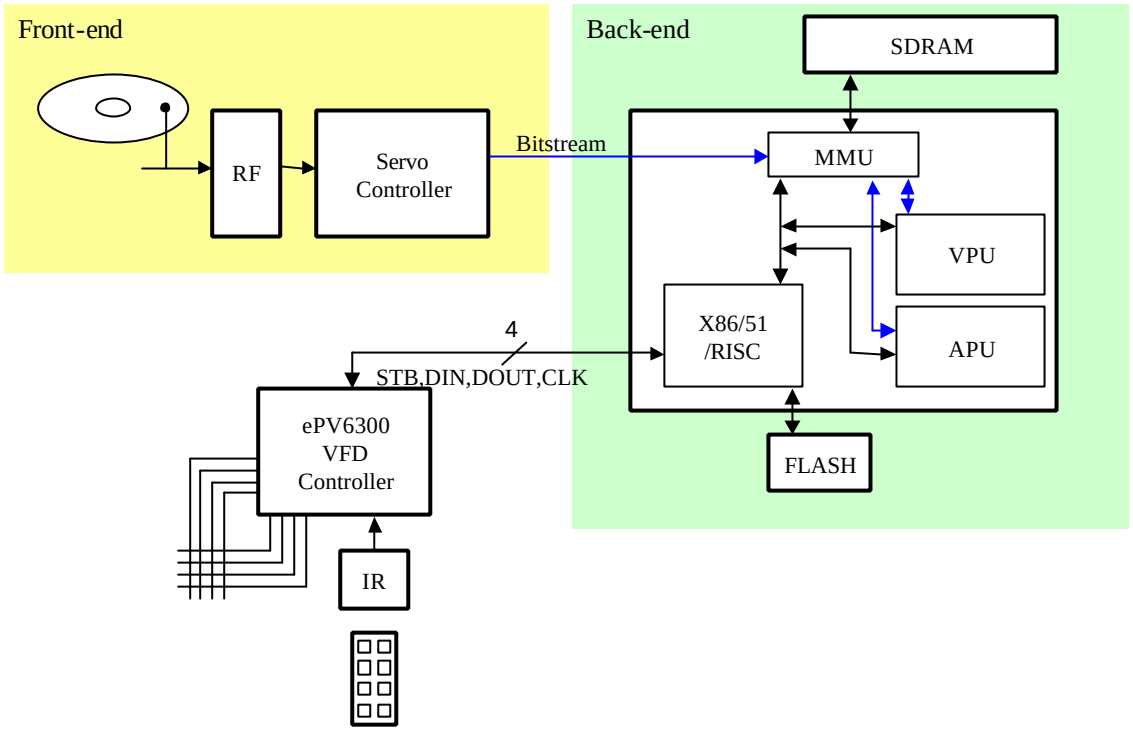
Command 1: Sets data.

Command 2: Sets address.

Data: Display data

XIII. Application

VFD Controller For DVD Player



VFD Controller For DVD R/W