

January 2013

FPF1203 / FPF1203L / FPF1204 / FPF12045 IntelliMAX™ Ultra-Small, Slew-Rate-Controlled Load Switch

Features

- 1.2 V to 5.5 V Input Voltage Operating Range
- Typical R_{ON}:
 - 45 mΩ at V_{IN}=5.5 V
 - 55 mΩ at V_{IN}=3.3 V
 - 90 mΩ at V_{IN}=1.8 V
 - 185 mΩ at V_{IN}=1.2 V
- Slew Rate Control with t_R:
 - FPF1203/FPF1203I/FPF1204: 100 μs
 - FPF12045: 2 μs
- Output Discharge Function on FPF1204 / 45
- Low <1.5 µA Quiescent Current
- ESD Protected: Above 7 kV HBM, 2 kV CDM
- GPIO / CMOS-Compatible Enable Circuitry
- 4-Bump, WLCSP 0.76 mm x 0.76 mm, 0.4 mm Pitch

Applications

- Mobile Devices and Smart Phones
- Portable Media Devices
- Tablet PCs
- Advanced Notebook, UMPC, MID
- Portable Medical Devices
- GPS and Navigation Equipment

Description

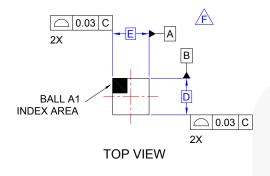
The FPF1203 / 03L / 04 / 45 are ultra-small integrated IntelliMAX™ load switches with integrated P-channel switch and analog control features. Integrated slew-rate control prevents inrush current and the resulting excessive voltage drop on the power rail. The input voltage range operates from 1.2 V to 5.5 V to provide power-disconnect capability for post-regulated power rails in portable and consumer products. The low shut-off current allows power designs to meet standby and off-power drain specifications.

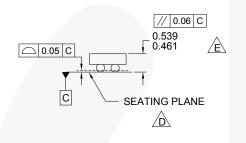
The FPF120x are controlled by a logic input (ON pin) compatible with standard CMOS GPIO circuitry found on Field Programmable Gate Array (FPGA) embedded processors. The FPF120x are available in 0.76 mm x 0.76 mm 4-bump WLCSP.

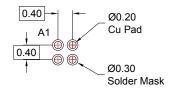
Ordering Information

Part Number	Top Mark	Switch (Typical) at 3.3V _{IN}	Output Discharge	ON Pin Activity	t _R	Package
FPF1203UCX	QL	55 mΩ	NA	Active HIGH	100 µs	
FPF1203LUCX	QP	55 mΩ	NA	Active LOW	100 µs	
FPF1204UCX	QM	55 mΩ	65Ω	Active HIGH	100 µs	4-Bump, Wafer-Level Chip-Scale Package (WLCSP), 0.76 mm x
FPF1204BUCX (Backside Laminate)	QM	55 mΩ	65Ω	Active HIGH	100 µs	0.76 mm, 0.4 mm Pitch
FPF12045UCX	NC	55 mΩ	65Ω	Active HIGH	2 µs	

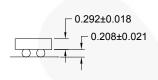
Physical Dimensions







RECOMMENDED LAND PATTERN (NSMD PAD TYPE)



SIDE VIEWS

NOTES:

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.
- DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).
- FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.
 - G. DRAWING FILNAME: MKT-UC004AFrev1.

BOTTOM VIEW

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В

 $(X)\pm0.018$

Figure 24. 4-Bump, 0.76 x 0.76 mm, Wafer-Level Chip-Scale Packaging

Product Dimensions

0.40

0.40

D	E	X	Y
760 μm ± 30 μm	760 μm ± 30 μm	0.180 mm± 0.018 μm	0.180 mm± 0.018 μm

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/packaging/.

⊕ 0.005∭ C A B

Ø0.260±0.020

 $(Y)\pm0.018$

/F\





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OPTOPLANAR®

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Definition of Terms

Definition of Terms					
Datasheet Identification	Product Status	Definition			
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.			
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