T-45-17

P33PCT480/A/B DUAL ODD-PARITY GENERATOR/CHECKER

ADVANCE INFORMATION

FEATURES

- 3.3V ± 0.2V Power Supply
- Center Power and Ground Pins to Minimize High Speed Switching Noise
- Two 8-Bit Parity Generator/Checker
- Three Speed Grades
  - Standard
  - Fast
  - Ultra-Fast
- Open Drain Low-Active Parity Error Output
- Expandable For Larger Word Widths
- CMOS For Low Power Dissipation
- Fully TTL Compatible Input and Output Levels
- Produced with PACE III Technology™
- Low Ground Bounce
- Compact Pinout
  - 28-Pin 300 mil DIP, SOIC

DESCRIPTION

The P33PCT480/A/B are high speed dual 8-bit parity generator/checkers. The device accepts eight data bits and one parity bit as inputs, and generates a parity and a parity error output. The 'PCT480/A/B generates and checks odd parity. In the CHECK mode, the parity output for each generator is low whenever an odd number of inputs is high; the common parity error output in the 'PCT480 is low, indicating an error, if either of the generated parity outputs is high. In the GENERATE mode, the two input parity bits are disabled and each device functions as in the CHECK mode.

The parity error output is open-drain, designed for easy expansion of the word width by a simple wired-OR connection of several 'PCT480 type devices. Since additional logic is not needed, the parity generation and checking times remain the same as for each 'PCT480 device.

The P33PCT480 is manufactured with PACE III Technology™ which is Performance Advanced CMOS Engineered with two-level metal and epitaxial substrates to use 0.4 micron effective channel lengths giving 250 picosecond loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.0V to 3.3V, thus reducing output swings dramatically. This, together with the (lower inductance) center power and ground pins, and the extra power and extra ground pins, significantly reduces noise and ground bounce that would otherwise occur for very high speed circuitry.

The 'PCT480/A/B are available in 28-pin 300 mil DIP and SOIC packages providing excellent board level densities.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 3.3V.

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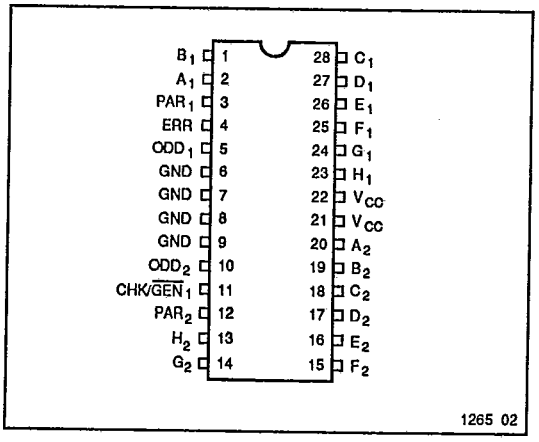
PIN CONFIGURATIONS



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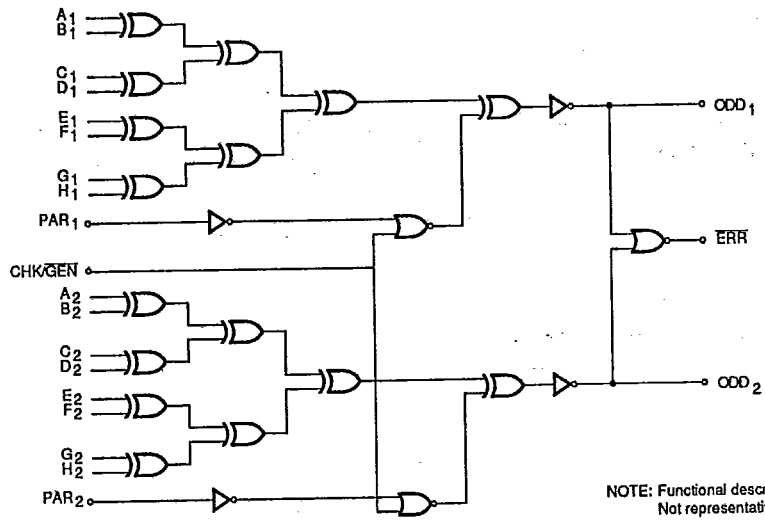
FUNCTIONAL BLOCK DIAGRAM



NOTE: Functional description only.
Not representative of propagation delays.

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