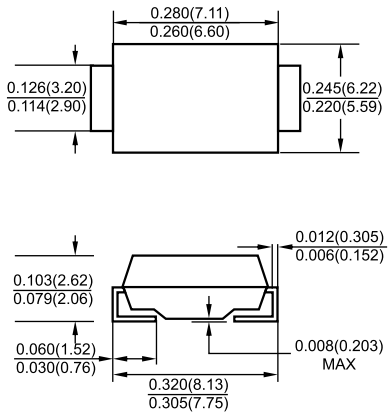
SSL32-SSL34

3.0AMP. Surface Mount Low V_F Schottky Barrier Rectifiers

SMC/DO-214AB



Dimensions in inches and (millimeters)

Features

- ✧ For surface mounted application
- ✧ Metal silicon junction, majority carrier conduction
- ✧ Low forward voltage drop
- ✧ Easy pick and place
- ✧ High surge current capability
- ✧ Plastic material used carries Underwriters Laboratory Classification 94V-0
- ✧ Epitaxial construction
- ✧ High temperature soldering: 260°C / 10 seconds at terminals

Mechanical Data

- ✧ Cases: Molded plastic
- ✧ Terminals: Matte tin plating
- ✧ Polarity: Indicated by cathode band
- ✧ Weight: 0.21gram

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.
Single phase, half wave, 60 Hz, resistive or inductive load.
For capacitive load, derate current by 20%

Type Number	Symbol	SSL32	SSL33	SSL34	Units
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	20	30	40	V
Maximum RMS Voltage	V_{RMS}	14	21	28	V
Maximum DC Blocking Voltage	V_{DC}	20	30	40	V
Maximum Average Forward Rectified Current See Fig. 1	$I_{(AV)}$	3.0			A
Peak Forward Surge Current, 8.3 ms Single Half Sine-wave Superimposed on Rated Load (JEDEC method)	I_{FSM}	100			A
Maximum Instantaneous Forward Voltage (Note 1) @3.0A	V_F	0.41			V
Maximum DC Reverse Current @ T_A =25°C	I_R	0.2		0.5	mA
at Rated DC Blocking Voltage @ T_A=100°C		50		100	mA
Maximum Thermal Resistance (Note 2)	$R_{\theta JL}$ $R_{\theta JA}$	17 55			°C /W
Marking Code		SL32	SL33	SL34	
Operating Temperature Range	T_J	-55 to +125			°C
Storage Temperature Range	T_{STG}	-55 to + 150			°C

Notes: 1. Pulse Test with PW=300 usec, 1% Duty Cycle.
2. Measured on P.C. Board with 0.6 x 0.6"(16.0 x 16.0mm) Copper Pad Areas.

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RATINGS AND CHARACTERISTIC CURVES (SSL32 THRU SSL34)

FIG.1- MAXIMUM FORWARD CURRENT DERATING CURVE

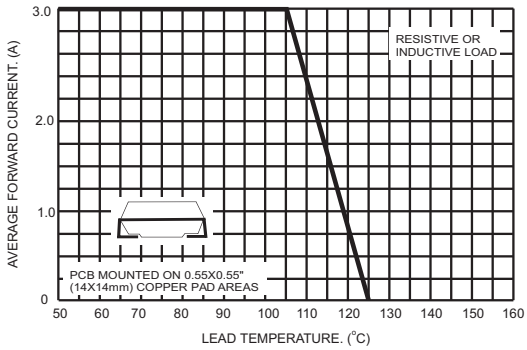

FIG.2- MAXIMUM NON-REPETITIVE PEAK FORWARD SURGE CURRENT

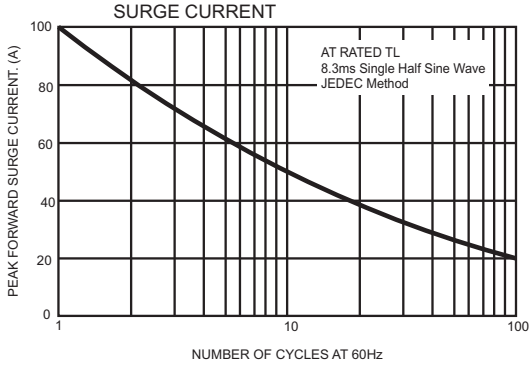

FIG.3- TYPICAL FORWARD CHARACTERISTICS

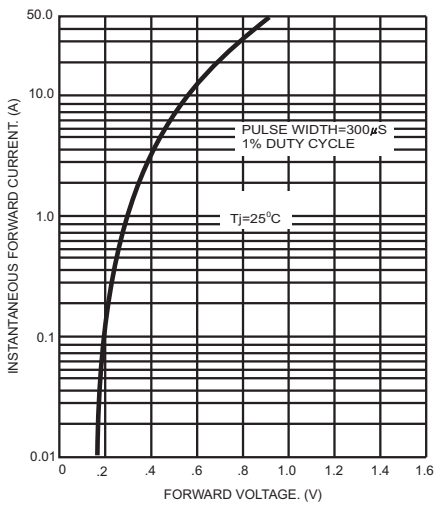

FIG.4- TYPICAL REVERSE CHARACTERISTICS

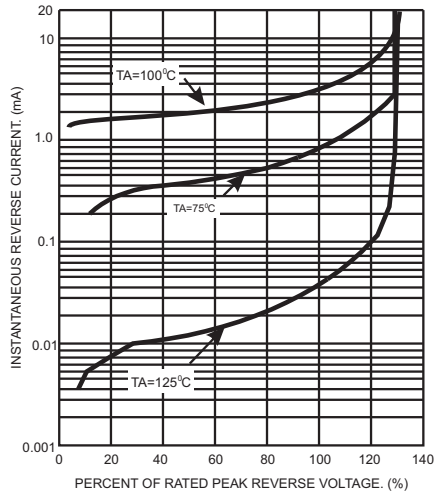

FIG.5- TYPICAL JUNCTION CAPACITANCE