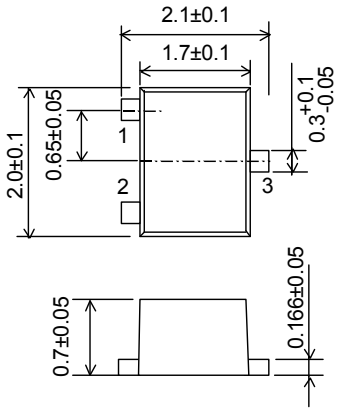
TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

# SSM3J36TU

## ○ Power Management Switches

- 1.5-V drive
- Low ON-resistance: $R_{on}$ = 3.60 Ω (max) (@$V_{GS}$ = -1.5 V)
  : $R_{on}$ = 2.70 Ω (max) (@$V_{GS}$ = -1.8 V)
  : $R_{on}$ = 1.60 Ω (max) (@$V_{GS}$ = -2.8 V)
  : $R_{on}$ = 1.31 Ω (max) (@$V_{GS}$ = -4.5 V)

Unit: mm




| | |
|---|---|
| UFM | 1: Gate<br>2: Source<br>3: Drain |
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-2U1A |

Weight: 6.6 mg (typ.)

## Absolute Maximum Ratings (Ta = 25 °C)

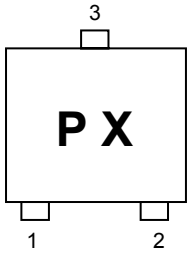
| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | -20 | V |
| Gate-source voltage | | $V_{GSS}$ | ±8 | V |
| Drain current | DC | $I_D$ | -330 | mA |
| | Pulse | $I_{DP}$ | -660 | |
| Drain power dissipation | | $P_D$ (Note1) | 500 | mW |
| | | $P_D$ (Note2) | 800 | |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55 to 150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

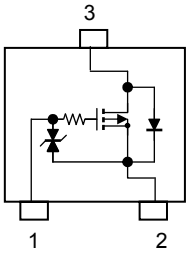
Note1: Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 $mm^2$)

Note2: Mounted on a ceramic board.
(25.4 mm × 25.4 mm × 0.8 mm, Cu Pad: 645 $mm^2$ )

## Marking




## Equivalent Circuit (top view)




## Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

## Usage Considerations

Let $V_{th}$ be the voltage applied between gate and source that causes the drain current ($I_D$) to below −1 mA for the SSM3J36TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th}$, and $V_{GS(off)}$ must be lower than $V_{th}$. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$. Take this into consideration when using the device.

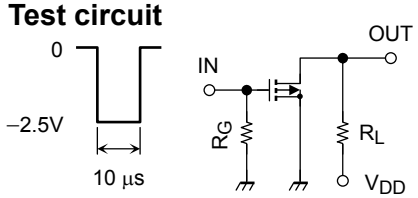
## Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = -1 mA, $V_{GS}$ = 0 V | -20 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = -1 mA, $V_{GS}$ = 8 V | -12 | — | — | |
| Drain cutoff current | | $I_{DSS}$ | $V_{DS}$ = -16 V, $V_{GS}$ = 0 V | — | — | -10 | μA |
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 V | — | — | ±1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = -3 V, $I_D$ = -1 mA | -0.3 | — | -1.0 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = -3 V, $I_D$ = -100mA (Note3) | 190 | — | — | mS |
| Drain-source ON-resistance | | $R_{DS\ (ON)}$ | $I_D$ = -100mA, $V_{GS}$ = -4.5 V (Note3) | — | 0.95 | 1.31 | Ω |
| | | | $I_D$ = -80mA, $V_{GS}$ = -2.8 V (Note3) | — | 1.22 | 1.60 | |
| | | | $I_D$ = -40mA, $V_{GS}$ = -1.8 V (Note3) | — | 1.80 | 2.70 | |
| | | | $I_D$ = -30mA, $V_{GS}$ = -1.5 V (Note3) | — | 2.23 | 3.60 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = -10 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 43 | — | pF |
| Output capacitance | | $C_{oss}$ | | — | 10.3 | — | |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 6.1 | — | |
| Total Gate Charge | | $Q_g$ | $V_{DS}$ = -10 V, $I_{DS}$= -330mA $V_{GS}$ = -4 V | — | 1.2 | — | nC |
| Gate−Source Charge | | $Q_{gs}$ | | — | 0.85 | — | |
| Gate−Drain Charge | | $Q_{gd}$ | | — | 0.35 | — | |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = -10 V, $I_D$ = -100mA $V_{GS}$ = 0 to -2.5 V, $R_G$ = 50Ω | — | 90 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 200 | — | |
| Drain-source forward voltage | | $V_{DSF}$ | $I_D$ =330mA, $V_{GS}$ = 0 V (Note3) | — | 0.88 | 1.2 | V |

Note3: Pulse test

## Switching Time Test Circuit

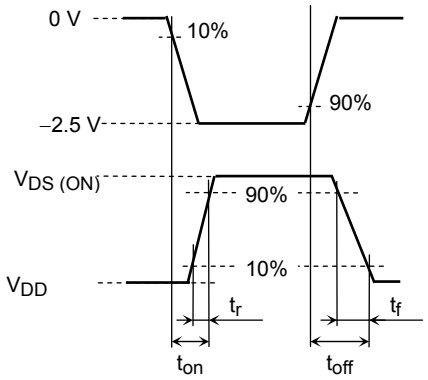
**(a) Test circuit**



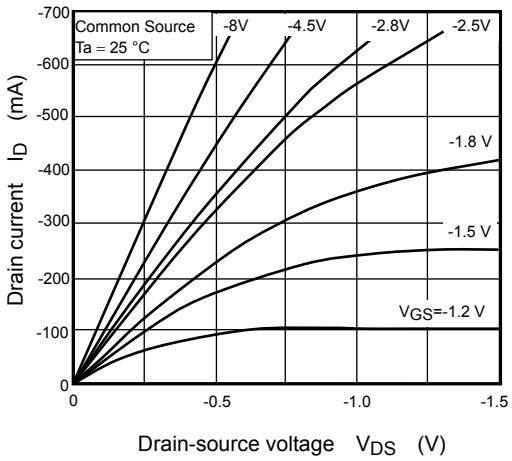

$V_{DD}$ = −10 V
Duty ≤ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
($Z_{out}$ = 50 Ω)
Common Source
Ta = 25°C

**(b) $V_{IN}$**

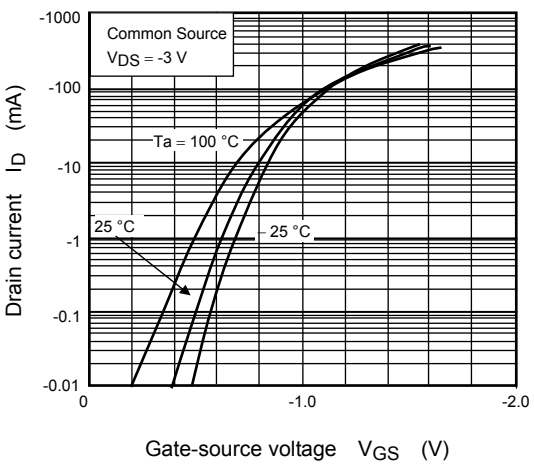
**(c) $V_{OUT}$**



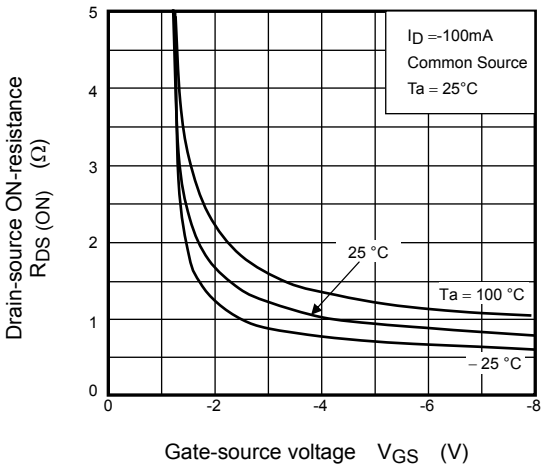
$I_D - V_{DS}$



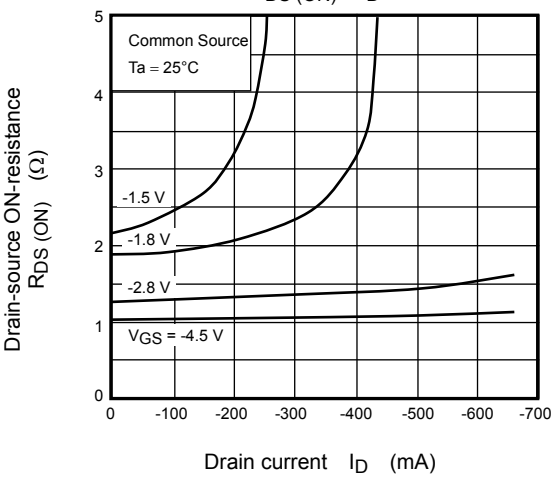

$I_D - V_{GS}$



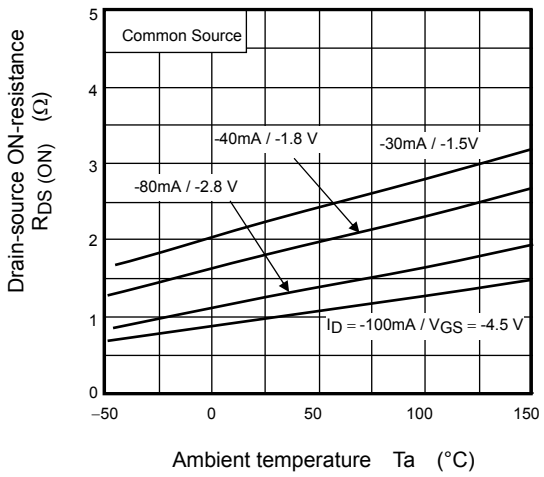

$R_{DS\ (ON)} - V_{GS}$



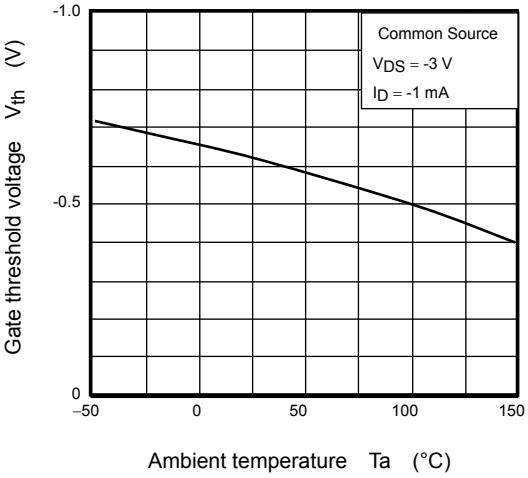

$R_{DS\ (ON)} - I_D$

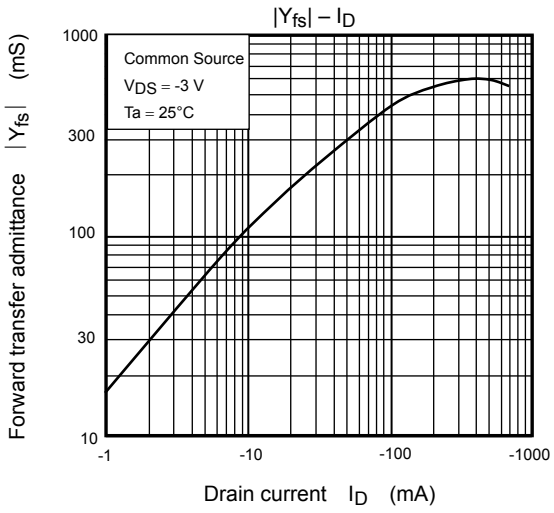


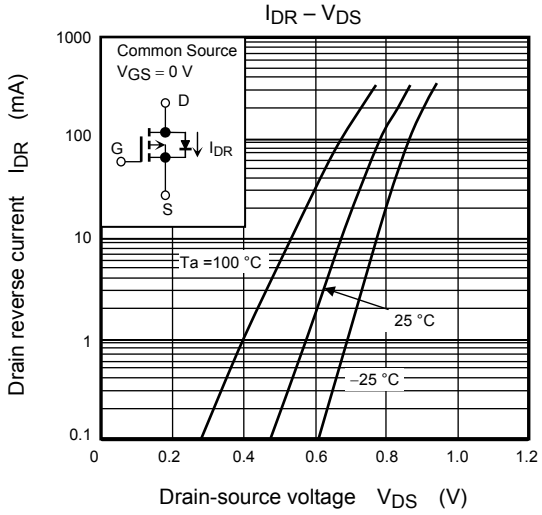

$R_{DS\ (ON)} - Ta$

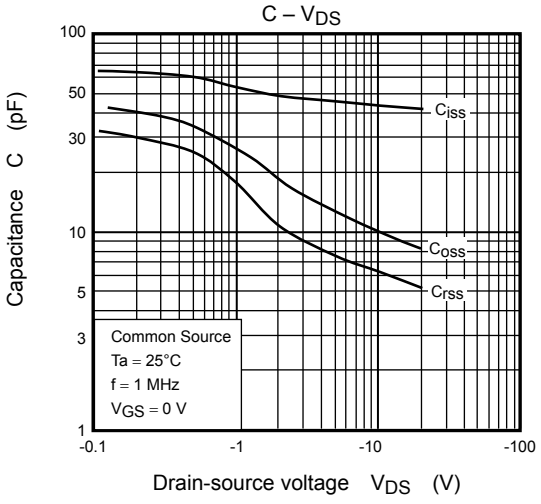


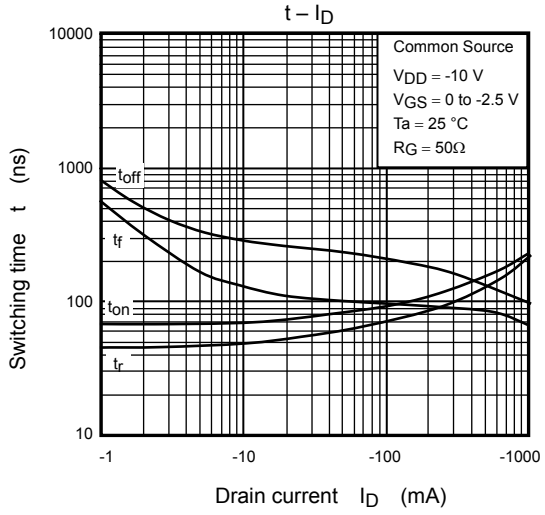

$V_{th} - Ta$

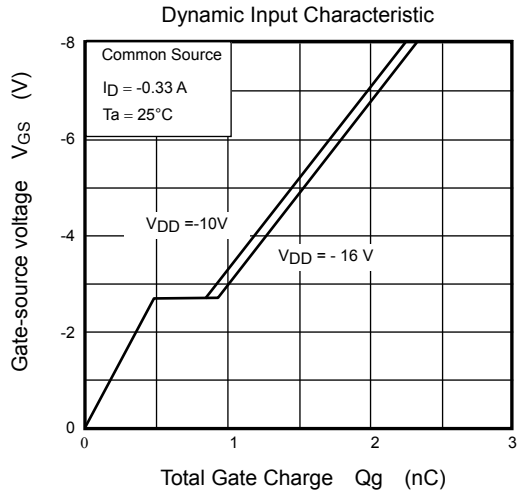


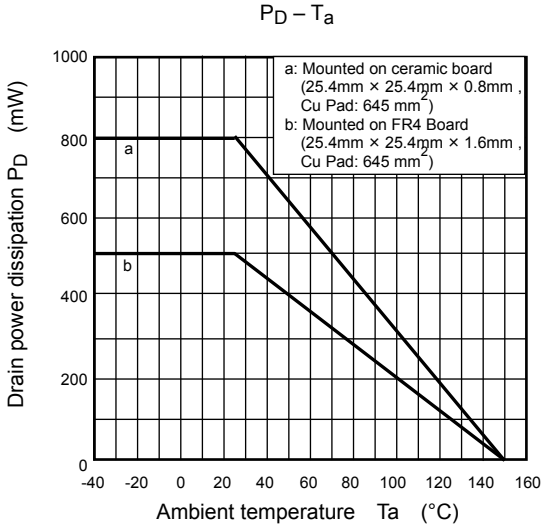

|Yfs| – ID
Common Source
VDS = -3 V
Ta = 25°C
Forward transfer admittance |Yfs| (mS)
Drain current ID (mA)
1000
300
100
30
10
-1
-10
-100
-1000


IDR – VDS
Common Source
VGS = 0 V
D
G
S
IDR
Ta =100 °C
25 °C
−25 °C
Drain reverse current IDR (mA)
Drain-source voltage VDS (V)
1000
100
10
1
0.1
0
0.2
0.4
0.6
0.8
1.0
1.2


C – VDS
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V
Capacitance C (pF)
Drain-source voltage VDS (V)
100
50
30
10
5
3
1
-0.1
-1
-10
-100


t – ID
Common Source
VDD = -10 V
VGS = 0 to -2.5 V
Ta = 25 °C
RG = 50Ω
toff
tf
ton
tr
Switching time t (ns)
Drain current ID (mA)
10000
1000
100
10
-1
-10
-100
-1000


Dynamic Input Characteristic
Common Source
ID = -0.33 A
Ta = 25°C
VDD =-10V
VDD = - 16 V
Gate-source voltage VGS (V)
Total Gate Charge Qg (nC)
-8
-6
-4
-2
0
0
1
2
3


PD – Ta
a: Mounted on ceramic board
(25.4mm × 25.4mm × 0.8mm ,
Cu Pad: 645 mm2)
b: Mounted on FR4 Board
(25.4mm × 25.4mm × 1.6mm ,
Cu Pad: 645 mm2)
a
b
Drain power dissipation PD (mW)
Ambient temperature Ta (°C)
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160

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