SONY

High Power DP3T Switch with Logic Control

CXG1215UR

Description

The CXG1215UR can be used in wireless communication systems, for example, dual-band CDMA handsets.
This IC has on-chip logic for operation with 3 COMS control inputs.
The Sony JPHEMT process is used for low insertion loss and on-chip logic circuit.
(Applications: Antenna switch for cellular handsets, dual-band CDMA)

Features

- ◆ Low insertion loss: 0.35dB@900MHz, 0.5dB@2GHz
- ◆ 3 CMOS compatible control line

Package

Small package size: 16-pin UQFN

Structure

GaAs JPHEMT MMIC

Absolute Maximum Ratings

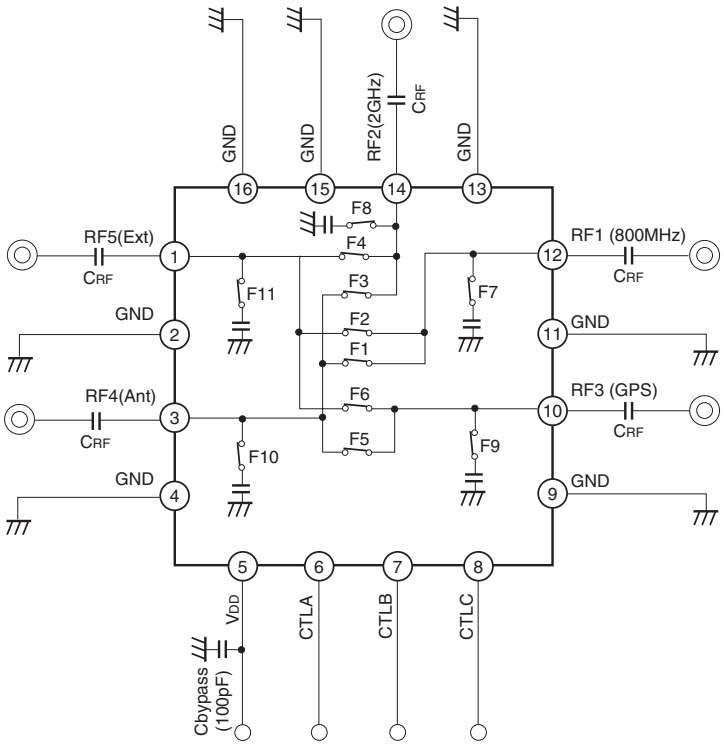
(Ta = 25℃)

◆ Input power max (RF port)	Pin	37	dBm
◆ Bias voltage	V_{DD}	7	V
◆ Control voltage	Vctl	5	V
◆ Operating temperature	Topr	–35 to +85	℃
◆ Storage temperature	Tstg	–65 to +150	℃

This IC is ESD sensitive device. Special handling precautions are required.

E06233B74

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

C_{RF}: This capacitor is used for RF decoupling and must be used for all applications.

Cbypass: This capacitor is used for DC line filtering.

Truth Table

State	CTLA	CTLB	CTLC	ON state	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11
1	L	L	H	RF4 – 1 (Ant-800MHz)	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON
2	L	H	H	RF4 – 2 (Ant-2GHz)	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	ON
3	H	L	H	RF4 – 3 (Ant-GPS)	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	ON
4	L	L	L	RF5 – 1 (EXT-800MHz)	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF
5	L	H	L	RF5 – 2 (EXT-2GHz)	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF
6	H	L	L	RF5 – 3 (EXT-GPS)	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF

DC Bias Conditions

(Ta = 25℃)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.6	3.2	V
Vctl (L)	0	—	0.5	V
V_{DD}	2.6	2.85	3.2	V

Electrical Characteristics

(Ta = 25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	830 to 930MHz		0.35	0.50	dB
		1575.42MHz		0.40	0.55	dB
		1.92 to 2.17GHz		0.50	0.65	dB
Isolation	ISO	830 to 930MHz	25	30		dB
		1575.42MHz	23	30		dB
		1.92 to 2.17GHz	20	30		dB
VSWR	VSWR	50Ω		1.2	1.4	—
Switching speed	TSW			5	10	μs
1dB compression input power	P1dB	V_{DD} = 2.85V		32		dBm
Harmonics	2fo	*1		–70	–65	dBc
	3fo	*1		–70	–65	dBc
	2fo	*2		–65	–60	dBc
	3fo	*2		–65	–60	dBc
Input IP3	IP3	*3	55	60		dBm
		*4	55	60		dBm
Bias current	Idd	V_{DD} = 2.85V		150	190	μA
Control current	Ictl	Vctl(H) = 2.6V		15	20	μA

*1 Pin = 25dBm, 0/2.6V control, V_{DD} = 2.85V, 890 to 930MHz

*2 Pin = 25dBm, 0/2.6V control, V_{DD} = 2.85V, 1.92 to 1.98GHz

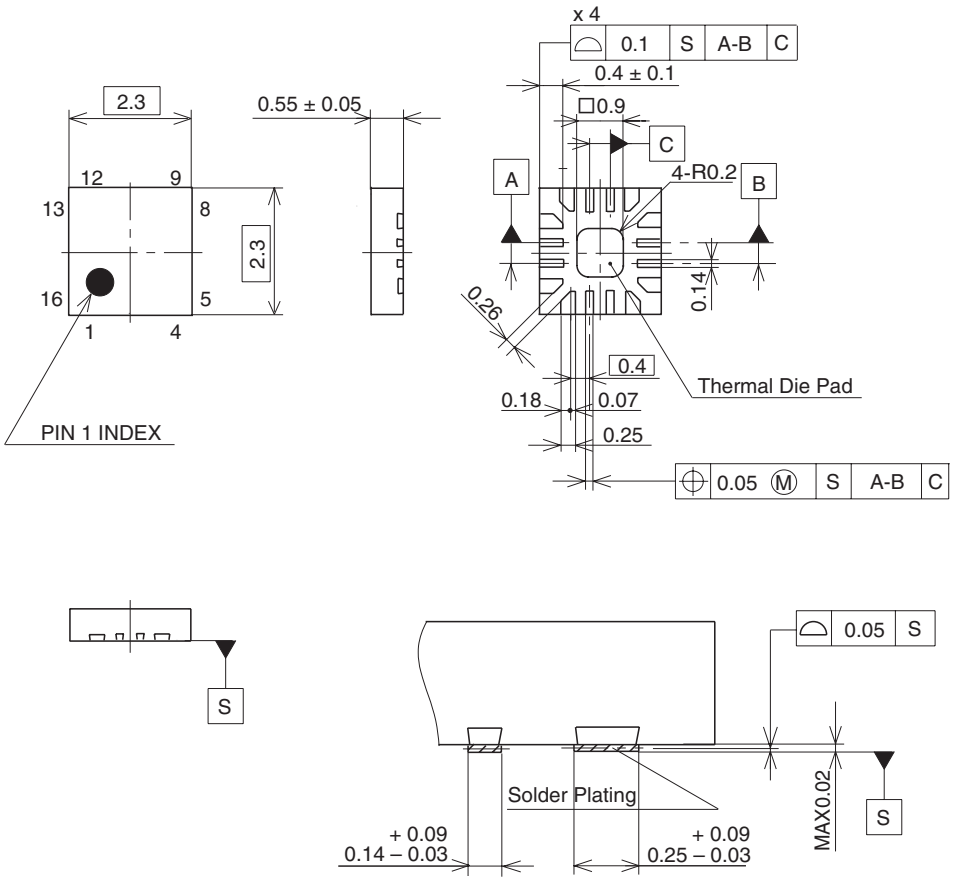
*3 Pin = 25dBm (900MHz) + 25dBm (901MHz), 0/2.6V control, V_{DD} = 2.85V

*4 Pin = 25dBm (1.9GHz) + 25dBm (1.901GHz), 0/2.6V control, V_{DD} = 2.85V

Package Outline

(Unit: mm)

16PIN UQFN（PLASTIC）



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-16P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm