MC10EP451, MC100EP451

3.3V / 5V ECL 6-Bit Differential Register with Master Reset

The MC10/100EP451 is a 6–bit fully differential register with common clock and single ended Master Reset (MR). It is ideal for very high frequency applications where a registered data path is necessary.

All inputs have a 75 kΩ pulldown resistor internally. Differential inputs have an override clamp. Unused differential register inputs can be left open and will default LOW. When the differential inputs are forced to $<V_{EE}$ + 1.2 V, the clamp will override and force the output to a default state. When in the default state, and since the flip–flop is edge triggered, the output reaches a determined, but not predicted, valid state.

The positive transition of CLK (pin 4) will latch the registers. Master Reset (MR) HIGH will asynchronously reset all registers forcing Q outputs to go LOW.

The 100 Series contains temperature compensation.

- 450 ps Typical Propagation Delay
- Maximum Frequency > 3.0 GHz Typical
- Asynchronous Master Reset
- 20 ps Skew Within Device, 35 ps Skew Device–To–Device
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V
  With V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V
  With V_{EE} = –3.0 V to –5.5 V
- Open Input Default State
- Safety Clamp on Inputs

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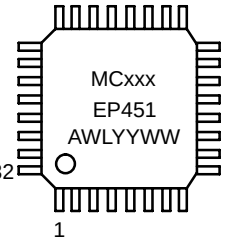
MARKING DIAGRAM*

LQFP–32
FA SUFFIX
CASE 873A

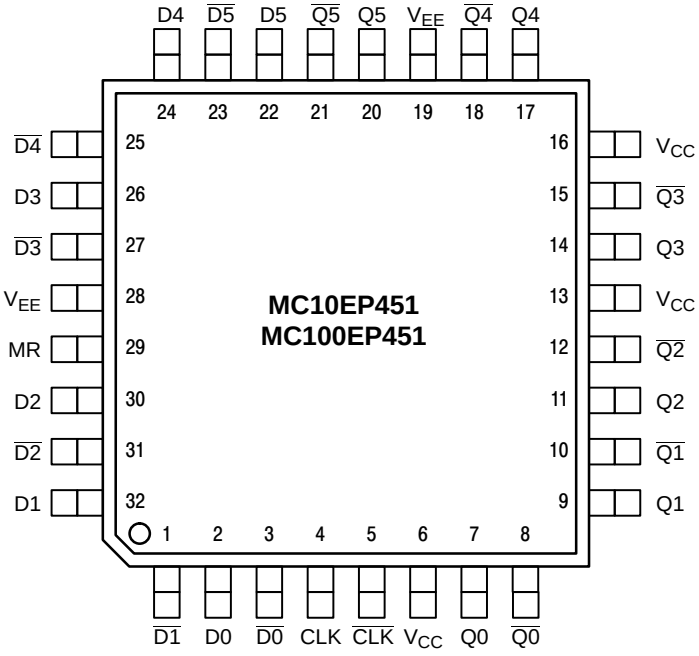


xxx = 10 or 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP451FA	LQFP–32	250 Units/Tray
MC10EP451FAR2	LQFP–32	2000 Tape & Reel
MC100EP451FA	LQFP–32	250 Units/Tray
MC100EP451FAR2	LQFP–32	2000 Tape & Reel



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32–Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
D [0:5]*, $\overline{D}$ [0:5]*	ECL Differential Data Inputs
$\overline{MR}$*	ECL Master Reset Input
CLK*, $\overline{CLK}$*	ECL Differential Clock Inputs
Q [0:5], $\overline{Q}$ [0:5]	ECL Differential Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.

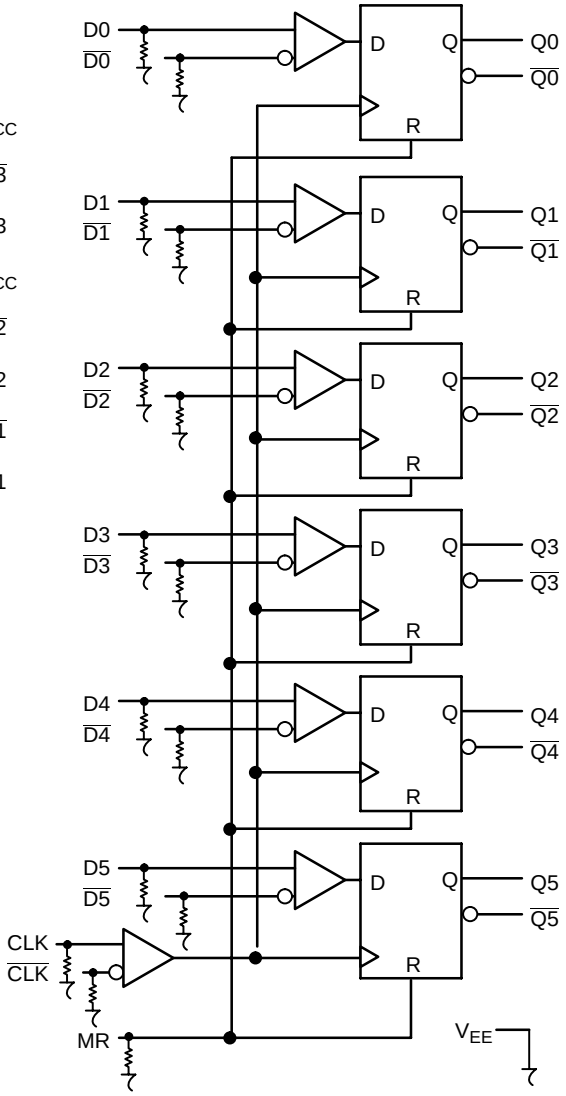


Figure 2. Logic Diagram

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		N/A
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV
Moisture Sensitivity (Note 1)		Level 2
Flammability Rating Oxygen Index		UL–94 code V–0 A 1/8” 28 to 34
Transistor Count		919 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		–6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 –6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	80	95	125	80	95	125	80	95	125	mA
V_{OH}	Output HIGH Voltage (Note 4)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 4)	1365	1490	1615	1430	1555	1680	1470	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single Ended)	1365		1690	1430		1755	1490		1815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to –2.2 V.
4. All loading with 50 ohms to V_{CC}–2.0 volts.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 6)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current	80	95	125	80	95	125	80	95	125	mA
V_{OH}	Output HIGH Voltage (Note 7)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 7)	3065	3190	3315	3130	3255	3380	3170	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single Ended)	3065		3390	3130		3455	3190		3515	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to –0.5 V.
7. All loading with 50 ohms to V_{CC}–2.0 volts.
8. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = –5.5 V to –3.0 V (Note 9)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	80	95	125	80	95	125	80	95	125	mA
V_{OH}	Output HIGH Voltage (Note 10)	–1135	–1010	–885	–1070	–945	–820	–1010	–885	–760	mV
V_{OL}	Output LOW Voltage (Note 10)	–1935	–1810	–1685	–1870	–1745	–1620	–1830	–1685	–1560	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1210		–885	–1145		–820	–1085		–760	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1935		–1610	–1870		–1545	–1810		–1485	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 11)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

9. Input and output parameters vary 1:1 with V_{CC}.
10. All loading with 50 ohms to V_{CC}–2.0 volts.
11. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 12)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	85	105	135	85	105	135	85	105	135	mA
V_{OH}	Output HIGH Voltage (Note 13)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 13)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 14)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to –2.2 V.
13. All loading with 50 ohms to V_{CC}–2.0 volts.
14. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 15)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	85	105	135	85	105	135	85	105	135	mA
V_{OH}	Output HIGH Voltage (Note 16)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 16)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single Ended)	3055		3375	3055		3375	3055		3375	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 17)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

15. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to –0.5 V.
16. All loading with 50 ohms to V_{CC}–2.0 volts.
17. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = –5.5 V to –3.0 V (Note 18)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	85	105	135	85	105	135	85	105	135	mA
V_{OH}	Output HIGH Voltage (Note 19)	–1145	–1020	–895	–1145	–1020	–895	–1145	–1020	–895	mV
V_{OL}	Output LOW Voltage (Note 19)	–1945	–1820	–1695	–1945	–1820	–1695	–1945	–1820	–1695	mV
V_{IH}	Input HIGH Voltage (Single Ended)	–1225		–880	–1225		–880	–1225		–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	–1945		–1625	–1945		–1625	–1945		–1625	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 20)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

18. Input and output parameters vary 1:1 with V_{CC}.
19. All loading with 50 ohms to V_{CC}–2.0 volts.
20. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.0 V to –5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 21)

Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency (See Figure 3. F_{max}/JITTER) (Note 22)			> 3.0			> 3.0			> 3.0		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	CLK to Q, $\overline{Q}$	330 430	430 530	530 630	350 450	450 550	550 650	390 490	490 590	590 690	ps
		MR to Q, $\overline{Q}$										
t_{RR}	Reset Recovery	MR to CLK	240	145		250	150		260	160		ps
t_S	Setup Time	D to CLK	80	40		80	40		80	40		ps
t_H	Hold Time	CLK to D	80	40		80	40		80	40		
t_{PW}	Minimum Pulse Rate	MR	400			400			400			ps
t_{SKEW}	Within–Device Skew (Note 23) Device–To–Device Skew (Note 24)			20 35	40 100		20 35	40 100		20 35	40 100	
t_{JITTER}	Cycle–to–Cycle Jitter (See Figure 3. F_{max}/JITTER)			0.2	< 1		0.2	< 1		0.2	< 1	ps
t_r	Output Rise/Fall Times	Q, $\overline{Q}$	100	150	250	110	160	260	130	180	280	ps
t_f	(20% – 80%)		100	150	250	110	160	260	130	180	280	

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.
22. V_{OL} and V_{OH} specifications not guaranteed for F_{max} testing.
23. Skew is measured between outputs under identical transitions and conditions on any one device.
24. Device–To–Device skew for identical transitions at identical V_{CC} levels.

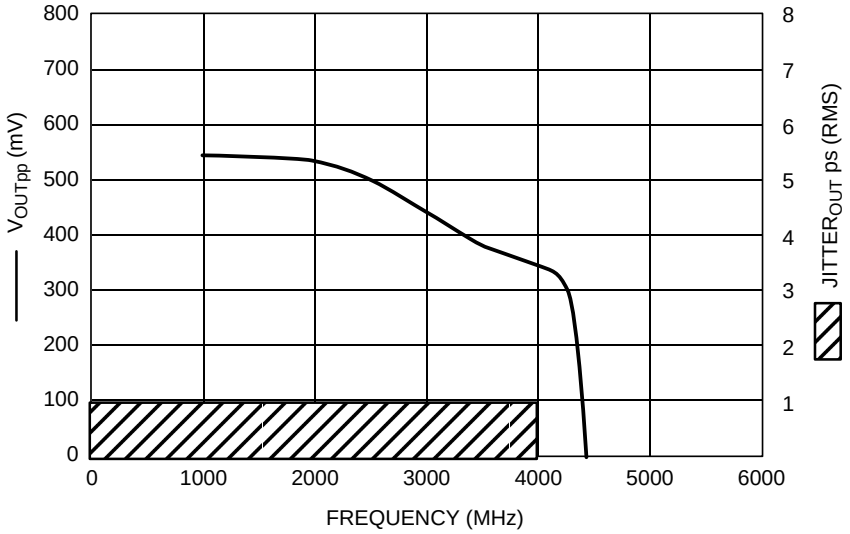


Figure 3. F_{max}/Jitter

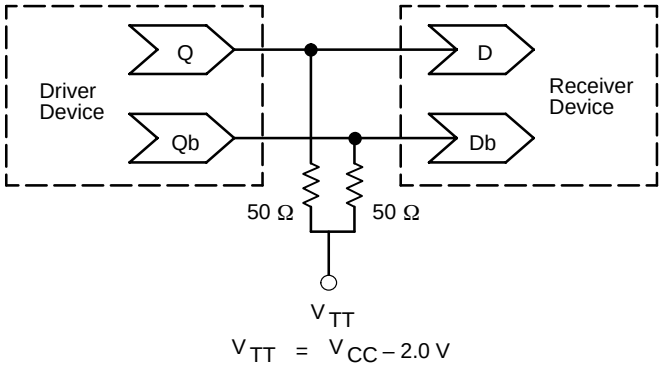


Figure 4. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices.)

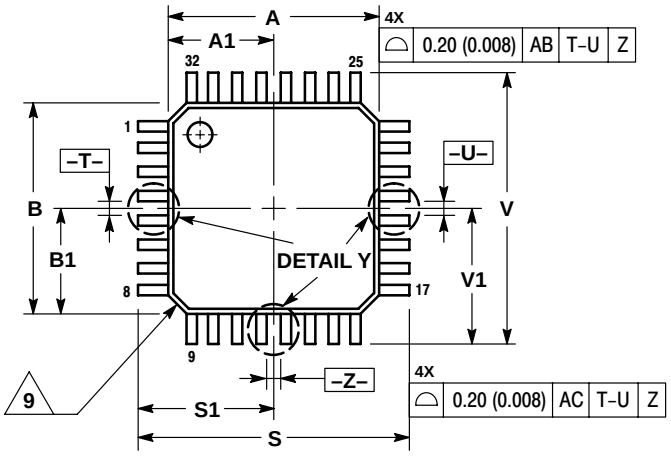
Resource Reference of Application Notes

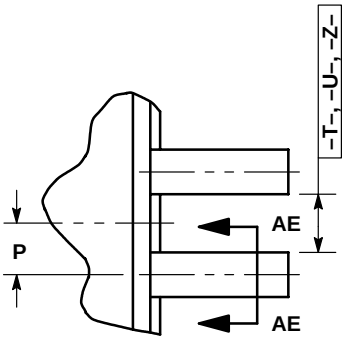
AN1404	–	ECLinPS Circuit Performance at Non–Standard V_{IH} Levels
AN1405	–	ECL Clock Distribution Techniques
AN1406	–	Designing with PECL (ECL at +5.0 V)
AN1504	–	Metastability and the ECLinPS Family
AN1568	–	Interfacing Between LVDS and ECL
AN1650	–	Using Wire–OR Ties in ECLinPS Designs
AN1672	–	The ECL Translator Guide
AND8001	–	Odd Number Counters Design
AND8002	–	Marking and Date Codes
AND8009	–	ECLinPS Plus Spice I/O Model Kit
AND8020	–	Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

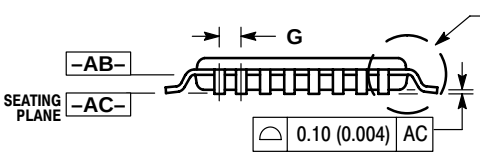
PACKAGE DIMENSIONS

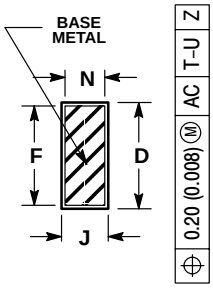
LQFP–32
FA SUFFIX
CASE 873A–02
ISSUE A



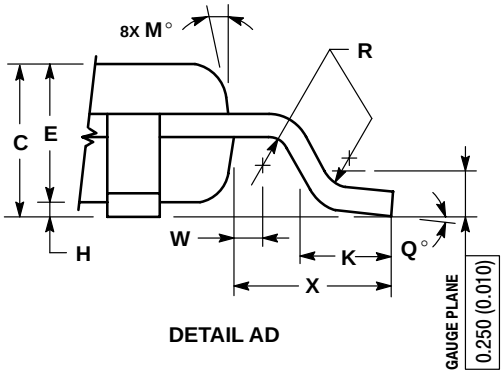


DETAIL Y





SECTION AE–AE



DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

PUBLICATION ORDERING INFORMATION

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N. American Technical Support: 800–282–9855 Toll Free USA/Canada

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