

RJK0636JPD

Silicon N Channel Power MOS FET
High Speed Power Switching

R07DS0365EJ0100
Rev.1.00
Aug 24, 2011

Features

- For Automotive application
- AEC-Q101 compliant
- Low on-resistance : $R_{DS(on)} = 18 \text{ m}\Omega$ typ.
- Capable of 4.5 V gate drive
- Low input capacitance : $C_{iss} = 750 \text{ pF}$ typ

Outline

RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))

1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} ^{Note2}	19	A
Avalanche energy	E_{AR} ^{Note2}	30.9	mJ
Channel dissipation	P_{ch} ^{Note3}	30	W
Channel temperature	T_{ch} ^{Note4}	175	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$
 4. AEC-Q101 compliant

Thermal Impedance Characteristics

- Channel to case thermal impedance θ_{ch-c} : $5^\circ\text{C}/\text{W}$

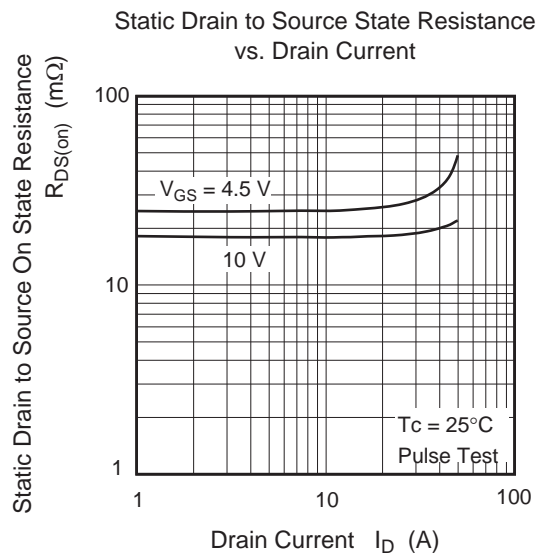
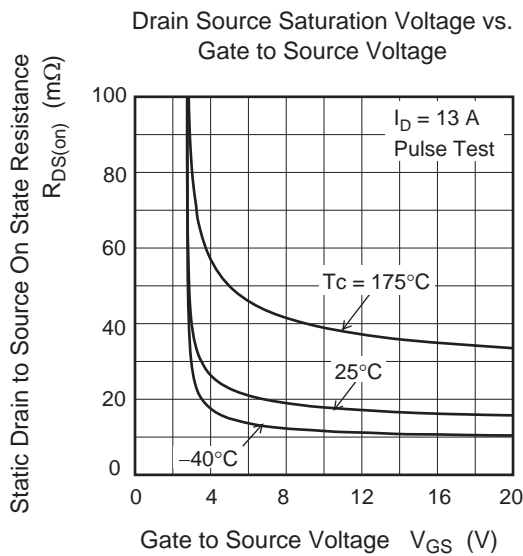
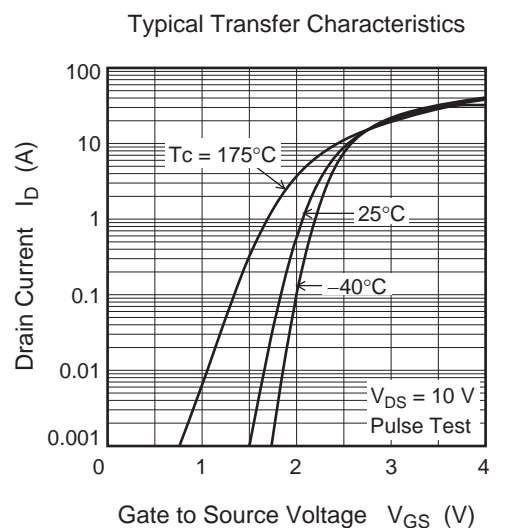
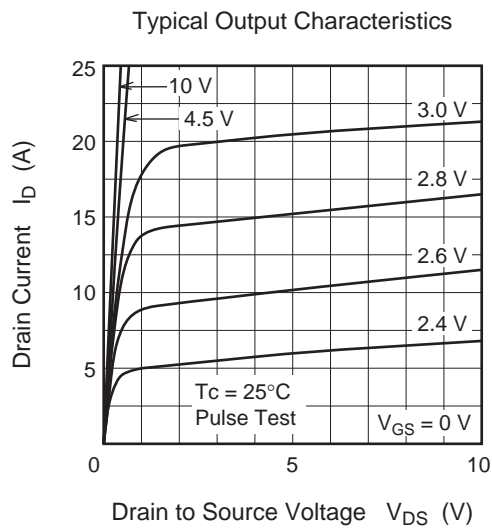
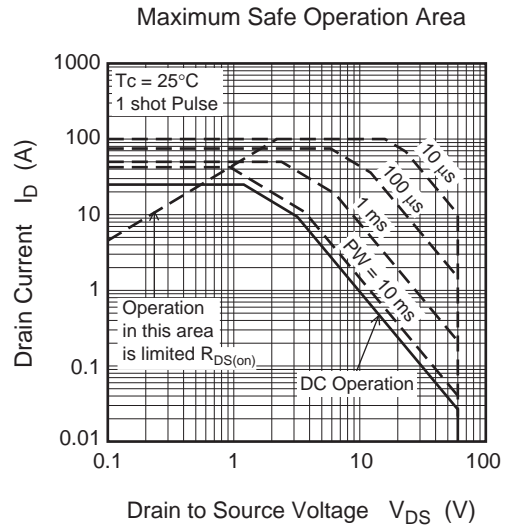
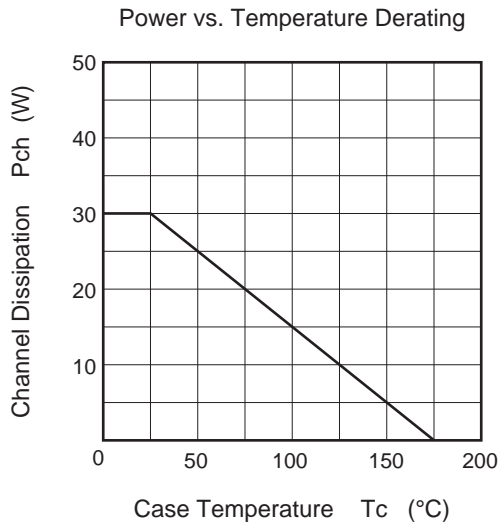
Electrical Characteristics

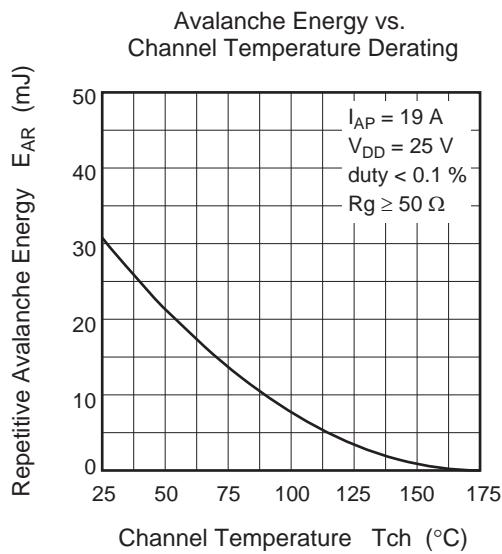
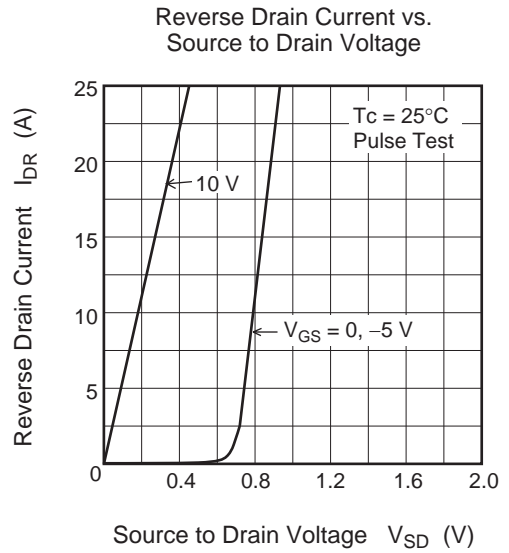
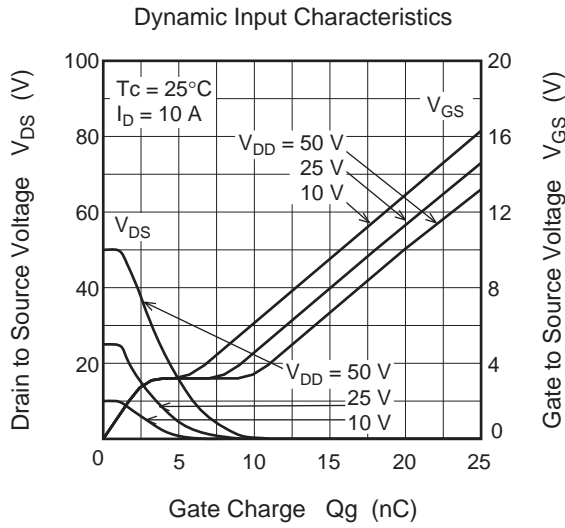
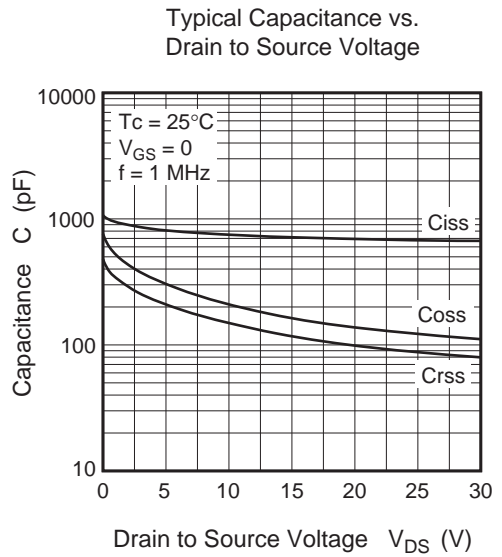
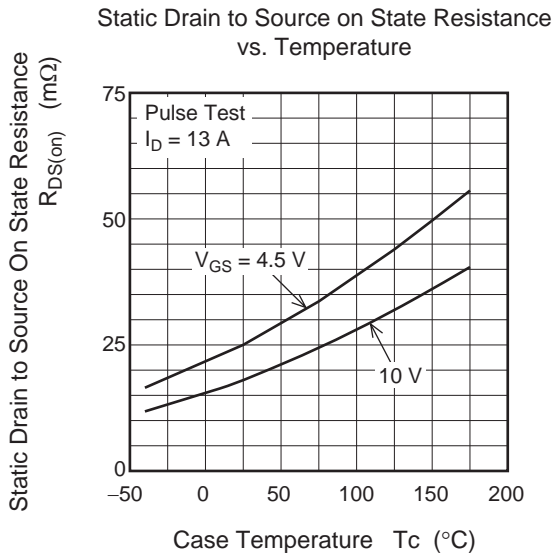
(Ta = 25°C)

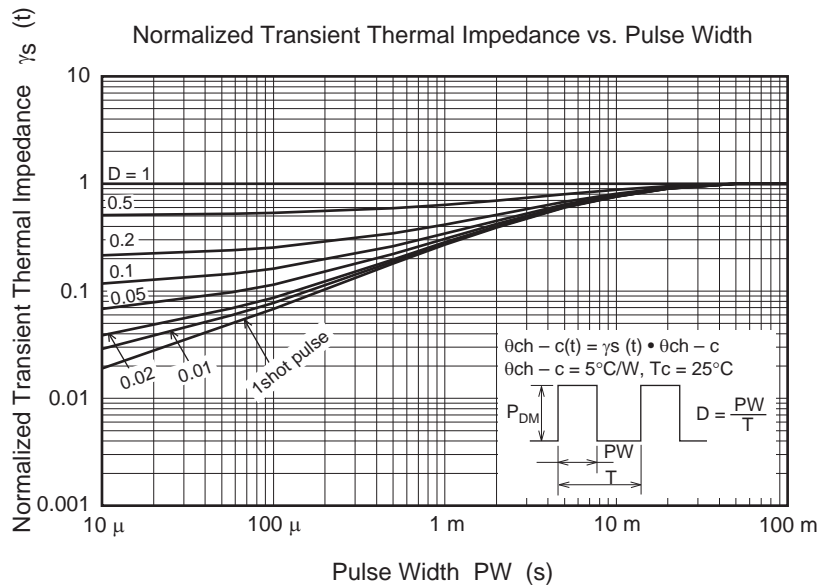
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$ ^{Note5}
Static drain to source on state resistance	$R_{DS(on)}$	—	18	22	mΩ	$I_D = 13 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note5}
	$R_{DS(on)}$	—	25	34	mΩ	$I_D = 13 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note5}
Input capacitance	C_{iss}	—	750	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	210	—	pF	
Reverse transfer capacitance	C_{rss}	—	150	—	pF	
Total gate charge	Q_g	—	18	—	nC	$V_{DD} = 25 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 25 \text{ A}$
Gate to source charge	Q_{gs}	—	2.5	—	nC	
Gate to drain charge	Q_{gd}	—	5.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$I_D = 13 \text{ A}, R_L = 2.3 \Omega,$ $V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$
Rise time	t_r	—	13	—	ns	
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	
Fall time	t_f	—	13	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.93	—	V	$I_F = 25 \text{ A}, V_{GS} = 0$ ^{Note5}
Body-drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 25 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 5. Pulse test

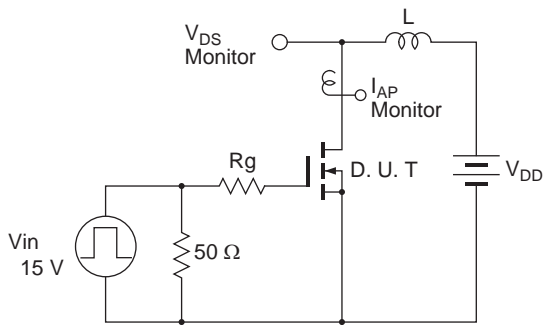
Main Characteristics





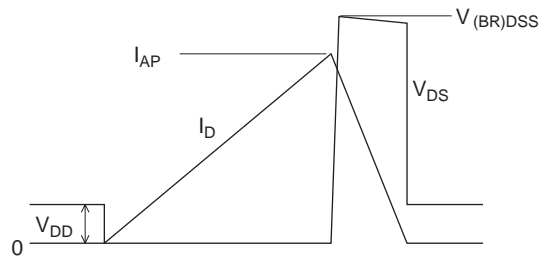


Avalanche Test Circuit

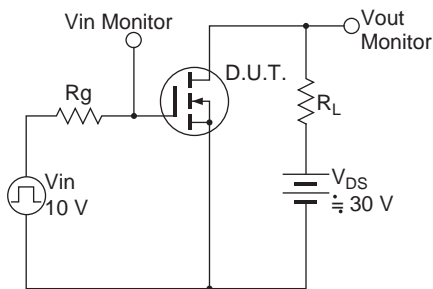


Avalanche Waveform

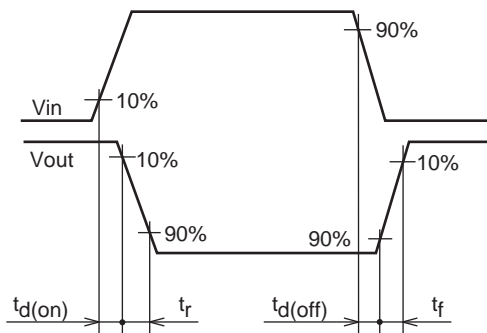
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



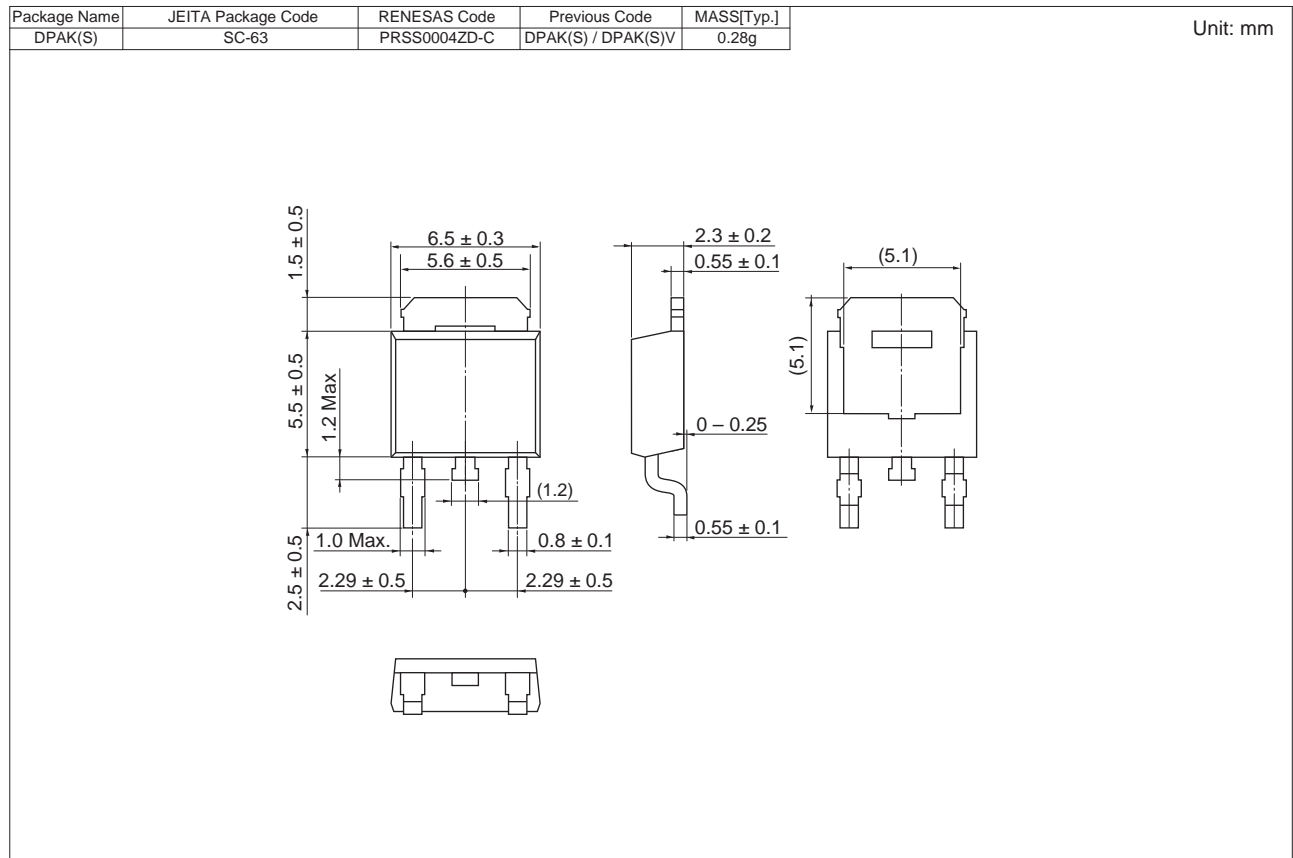
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK0636JPD-00-J3	3000 pcs	Taping (Sinistrorse)

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141