DATA SHEET

74AHC32; 74AHCT32
Quad 2-input OR gate

Product specification
Supersedes data of 1999 Sep 27

2004 May 19

Philips
Semiconductors

PHILIPS

Quad 2-input OR gate 74AHC32; 74AHCT32

FEATURES

- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101 exceeds 1000 V.
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accepts voltages higher than V_{CC}
- For 74AHC32 only: operates with CMOS input levels
- For 74AHCT32 only: operates with TTL input levels
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74AHC32; 74AHCT32 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC32; 74AHCT32 provides the 2-input OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74AHC32	74AHCT32	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	2.8	3.1	ns
C_I	input capacitance	$V_I = V_{CC}$ or GND	3.0	3.0	pF
C_O	output capacitance		4.0	4.0	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; notes 1 and 2	10	12	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

Table 1 See note 1.

INPUT		OUTPUT
nA	**nB**	**nY**
L	L	L
L	H	H
H	L	H
H	H	H

Note

1. H = HIGH voltage level
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74AHC32D	–40 °C to +125 °C	14	SO14	plastic	SOT108-1
74AHCT32D	–40 °C to +125 °C	14	SO14	plastic	SOT108-1
74AHC32PW	–40 °C to +125 °C	14	TSSOP14	plastic	SOT402-1
74AHCT32PW	–40 °C to +125 °C	14	TSSOP14	plastic	SOT402-1
74AHC32BQ	–40 °C to +125 °C	14	DHVQFN14	plastic	SOT762-1
74AHCT32BQ	–40 °C to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V_{CC}	supply voltage

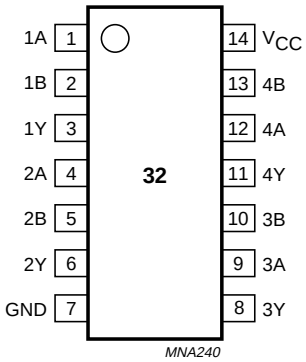
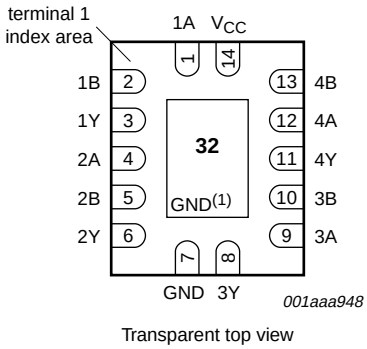


Fig.1 Pin configuration SO14 and TSSOP14.



Transparent top view

(1) The die substrate is attached to the exposed die pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

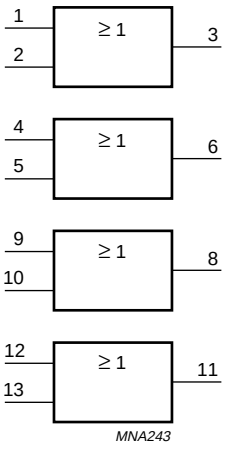


Fig.3 IEC logic symbol.

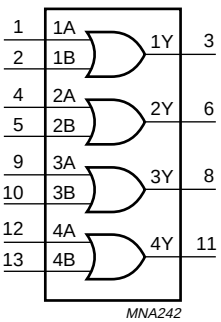


Fig.4 Functional diagram.

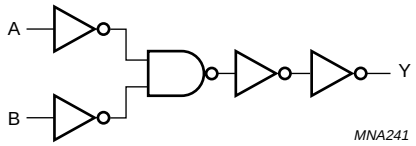


Fig.5 Logic diagram (one gate).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74AHC32			74AHCT32			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	–	5.5	0	–	5.5	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 3.3 V ± 0.3 V	–	–	100	–	–	–	ns/V
		V_{CC} = 5 V ± 0.5 V	–	–	20	–	–	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
V_I	input voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < –0.5 V; note 1	–	–20	mA
I_{OK}	output diode current	V_O < –0.5 V or V_O > V_{CC} + 0.5 V; note 1	–	±20	mA
I_O	output source or sink current	V_O > –0.5 V and V_O < V_{CC} + 0.5 V	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±75	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
   For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
   For DHVQFN14 packages: above 60 °C the value of P_{tot} derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

Type 74AHC32

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA; all outputs	2.0	1.9	2.0	–	V
		I_O = –50 μA; all outputs	3.0	2.9	3.0	–	V
		I_O = –50 μA; all outputs	4.5	4.4	4.5	–	V
		I_O = –4.0 mA	3.0	2.58	–	–	V
		I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA; all outputs	2.0	–	0	0.1	V
		I_O = 50 μA; all outputs	3.0	–	0	0.1	V
		I_O = 50 μA; all outputs	4.5	–	0	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.36	V
		I_O = 8.0 mA	4.5	–	–	0.36	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	0.1	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.5	–	–	±0.25	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	5.5	–	–	2.0	μA
C_I	input capacitance		–	–	3	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA; all outputs	2.0	1.9	–	–	V
		I_O = –50 μA; all outputs	3.0	2.9	–	–	V
		I_O = –50 μA; all outputs	4.5	4.4	–	–	V
		I_O = –4.0 mA	3.0	2.48	–	–	V
		I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA; all outputs	2.0	–	–	0.1	V
		I_O = 50 μA; all outputs	3.0	–	–	0.1	V
		I_O = 50 μA; all outputs	4.5	–	–	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.44	V
		I_O = 8.0 mA	4.5	–	–	0.44	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	1.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.5	–	–	±2.5	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	5.5	–	–	20	μA
C_I	input capacitance		–	–	–	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			3.0	2.1	–	–	V
			5.5	3.85	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			3.0	–	–	0.9	V
			5.5	–	–	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA; all outputs	2.0	1.9	–	–	V
		I_O = –50 μA; all outputs	3.0	2.9	–	–	V
		I_O = –50 μA; all outputs	4.5	4.4	–	–	V
		I_O = –4.0 mA	3.0	2.40	–	–	V
		I_O = –8.0 mA	4.5	3.70	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA; all outputs	2.0	–	–	0.1	V
		I_O = 50 μA; all outputs	3.0	–	–	0.1	V
		I_O = 50 μA; all outputs	4.5	–	–	0.1	V
		I_O = 4.0 mA	3.0	–	–	0.55	V
		I_O = 8.0 mA	4.5	–	–	0.55	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	5.5	–	–	2.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.5	–	–	±10.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	5.5	–	–	40	μA
C_I	input capacitance		–	–	–	10	pF

Type 74AHCT32

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA; all outputs	4.5	4.4	4.5	–	V
		I_O = –8.0 mA	4.5	3.94	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA; all outputs	4.5	–	0	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.36	V
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	0.1	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	5.5	–	–	±0.25	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	5.5	–	–	2.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 2.1 V other inputs at V_{CC} or GND; I_O = 0 A	4.5 to 5.5	–	–	1.35	mA
C_I	input capacitance		–	–	3	10	pF
T_{amb} = –40 °C to +85 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA; all outputs	4.5	4.4	–	–	V
		I_O = –8.0 mA	4.5	3.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA; all outputs	4.5	–	–	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.44	V
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	1.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	5.5	–	–	±2.5	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	5.5	–	–	20	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 2.1 V other inputs at V_{CC} or GND; I_O = 0 A	4.5 to 5.5	–	–	1.5	mA
C_I	input capacitance		–	–	–	10	pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –50 μA; all outputs	4.5	4.4	–	–	V
		I_O = –8.0 mA	4.5	3.70	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 50 μA; all outputs	4.5	–	–	0.1	V
		I_O = 8.0 mA	4.5	–	–	0.55	V
I_{LI}	input leakage current	V_I = V_{IH} or V_{IL}	5.5	–	–	2.0	μA
I_{OZ}	3-state output OFF current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A	5.5	–	–	±10.0	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	5.5	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 2.1 V other inputs at V_{CC} or GND; I_O = 0 A	4.5 to 5.5	–	–	1.5	mA
C_I	input capacitance		–	–	–	10	pF

AC CHARACTERISTICS

Type 74AHC32

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Fig.7.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L				
T_{amb} = 25 °C							
V_{CC} = 3.0 V to 3.6 V; note 1							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	–	3.9	7.9	ns
			50 pF	–	5.6	11.4	ns
V_{CC} = 4.5 V to 5.5 V; note 2							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	–	2.8	5.5	ns
			50 pF	–	4.1	7.5	ns
T_{amb} = −40 °C to +85 °C							
V_{CC} = 3.0 V to 3.6 V							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	9.5	ns
			50 pF	1.0	–	13	ns
V_{CC} = 4.5 V to 5.5 V							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	6.5	ns
			50 pF	1.0	–	8.5	ns
T_{amb} = −40 °C to +125 °C							
V_{CC} = 3.0 V to 3.6 V							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	10.0	ns
			50 pF	1.0	–	14.5	ns
V_{CC} = 4.5 V to 5.5 V							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	7.0	ns
			50 pF	1.0	–	9.5	ns

Notes

1. Typical values are measured at V_{CC} = 3.3 V.
2. Typical values are measured at V_{CC} = 5.0 V.

Type 74AHCT32

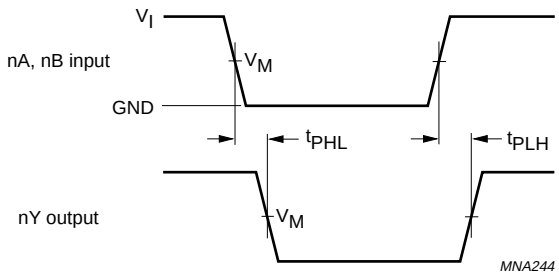
GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Fig.7.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C_L				
T_{amb} = 25 °C							
V_{CC} = 4.5 V to 5.5 V; note 1							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	–	3.1	6.9	ns
			50 pF	–	4.3	7.9	ns
T_{amb} = −40 °C to +85 °C							
V_{CC} = 4.5 V to 5.5 V							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	8.0	ns
			50 pF	1.0	–	9.0	ns
T_{amb} = −40 °C to +125 °C							
V_{CC} = 4.5 V to 5.5 V							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Fig.6	15 pF	1.0	–	9.0	ns
			50 pF	1.0	–	10.0	ns

Note

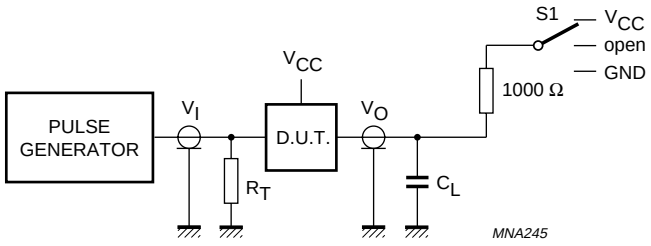
1. Typical values are measured at V_{CC} = 5.0 V.

AC WAVEFORMS



FAMILY	V_I INPUT REQUIREMENTS	V_M INPUT	V_M OUTPUT
AHC	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
AHCT	GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$

Fig.6 The input (nA, nB) to output (nY) propagation delays.



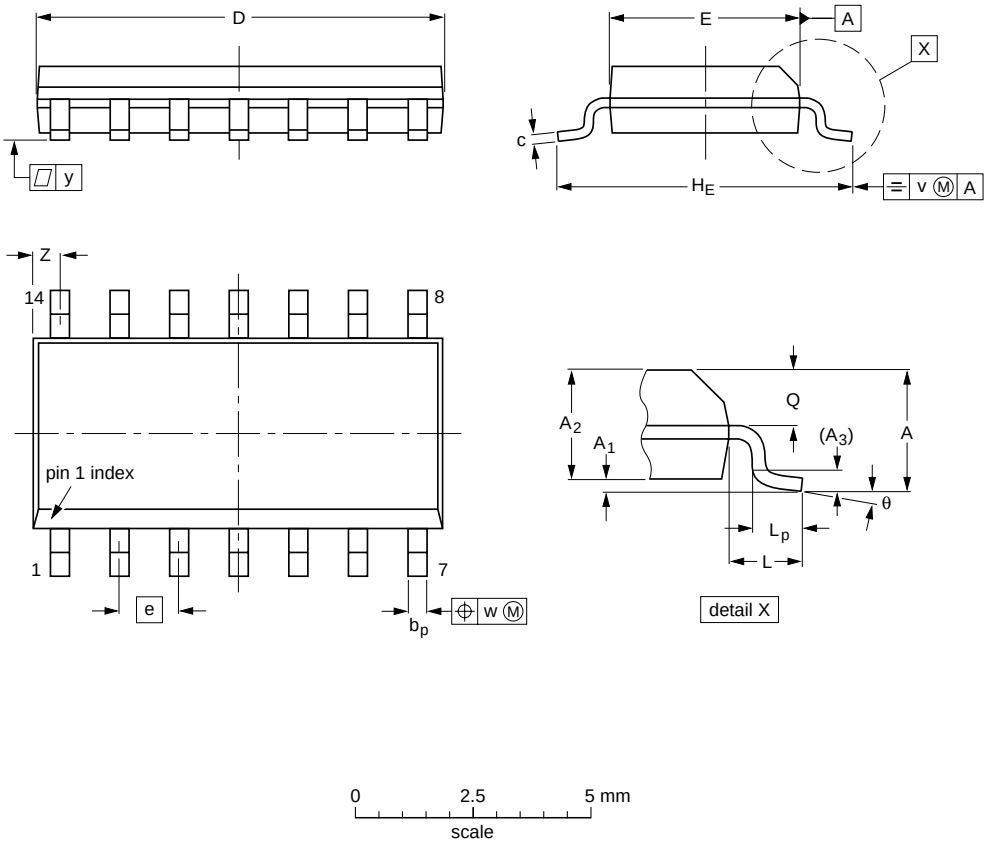
TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
C_L = load capacitance including jig and probe capacitance.
RT = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.7 Load circuitry for switching times.

PACKAGE OUTLINES

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

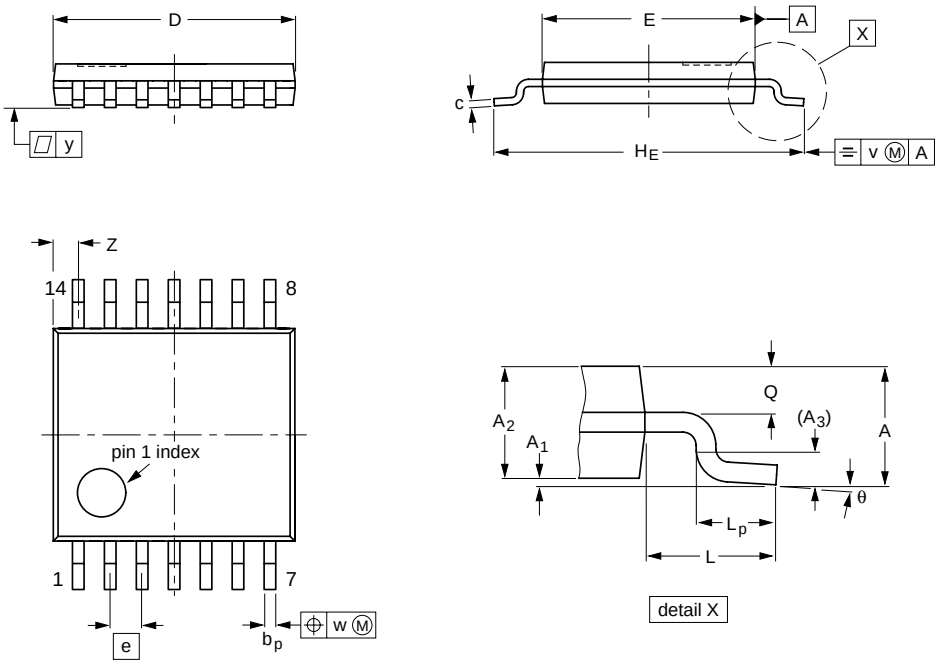
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

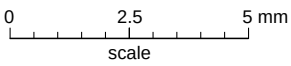
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





DIMENSIONS (mm are the original dimensions)

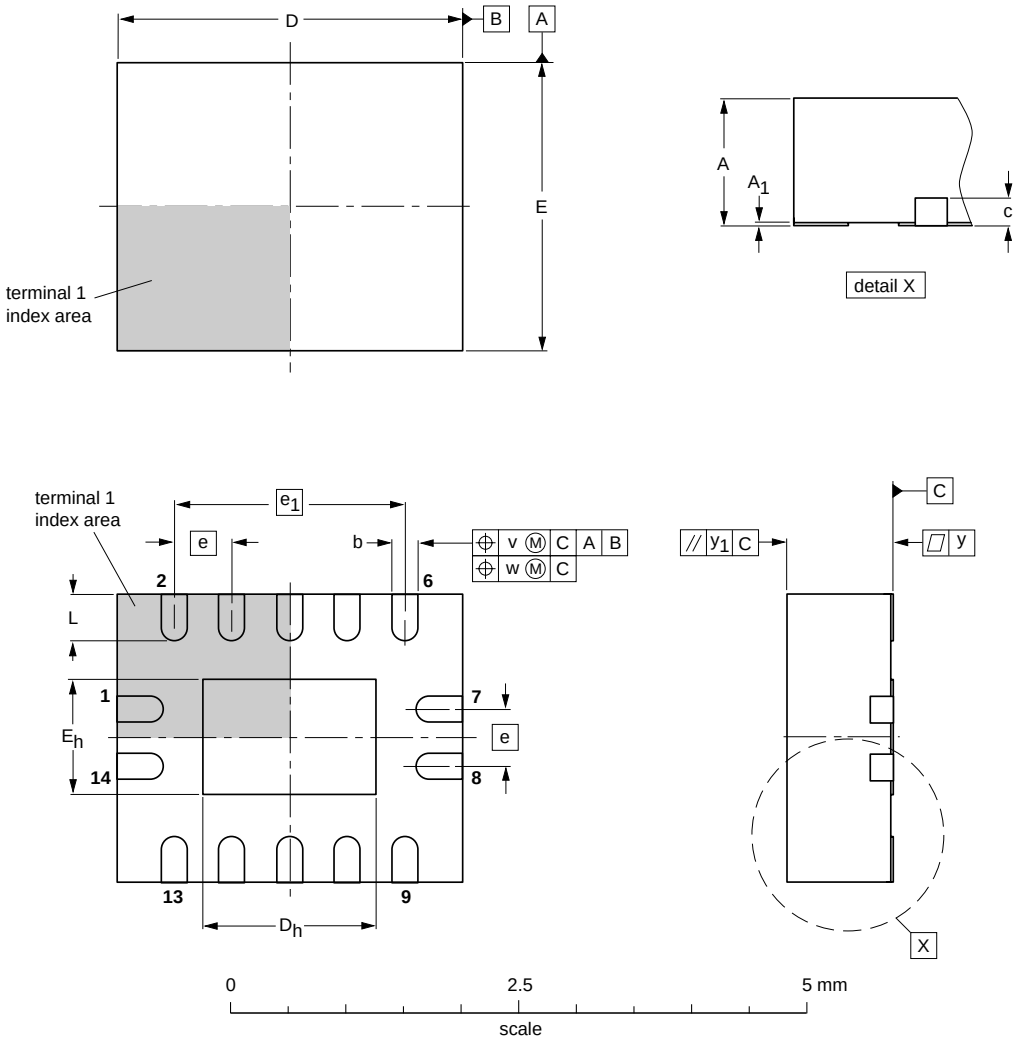
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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