



ADDV1333W8G9
DDR3L-1333(CL9) 240-Pin VLP R-DIMM
8GB(1024Mx72-bits)

ADATA Technology Corp.

Memory Module Data Sheet

DDR3L-1333(CL9) 240-Pin VLP R-DIMM 8GB (1024M x 72-bits)

Version 0.1

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Revision History

Version	Changes	Page	Date
0.1	Initial release	-	2012/05/31



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General Description :

The ADATA's module is a 1024Mx72 bits 8GB(8192MB) DDR3L-1333(CL9)-9-9-24 SDRAM memory module. The SPD is programmed to JEDEC standard latency 1333Mbps timing of 9-9-9-24 at 1.35V. The module is composed of eighteen 512Mx8 bits CMOS DDR3 SDRAMs in FBGA package and one 2Kbit EEPROM in 8pin TDFN package on a 240pin glass-epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 240-pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features :

- Power supply (Normal): VDD & VDDQ = 1.35V ± 0.0675V
- MRS Cycle with address key programs
 - CAS Latency (5,6,7,8,9)
 - Burst Length (BL):8 and 4 with Burst Chop(BC)
- Bi-directional, differential data strobe (DQS and /DQS)
- Differential clock input (CK, /CK) operation
- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture; two data transfers per clock cycle
- 8 independent internal bank
- Internal (self) calibration: Internal self calibration through ZQ pin (RZQ:240 ohm±1%)
- Auto refresh and self refresh
- Average Refresh Period 7.8us at lower then TCASE 85°C, 3.9us at 85°C < TCASE ≤ 95°C
- 8-bit pre-fetch.
- On Die Termination using ODT pin.
- On-board I2C temperature sensor with integrated serial presence-detect (SPD) EEPROM.
- EEPROM software write protect.
- Supports ECC error detection and correction.
- Lead-free products are RoHS Compliant



Pin Assignment :

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREFDQ	41	VSS	81	DQ32	121	VSS	161	TDQS17	201	DQ37
2	VSS	42	/DQS8	82	DQ33	122	DQ4	162	/TDQS17	202	VSS
3	DQ0	43	DQS8	83	VSS	123	DQ5	163	VSS	203	TDQS13
4	DQ1	44	VSS	84	/DQS4	124	VSS	164	CB6	204	/TDQS13
5	VSS	45	CB2	85	DQS4	125	TDQS9	165	CB7	205	VSS
6	/DQS0	46	CB3	86	VSS	126	/TDQS9	166	VSS	206	DQ38
7	DQS0	47	VSS	87	DQ34	127	VSS	167	NC	207	DQ39
8	VSS	48	VTT	88	DQ35	128	DQ6	168	/RESET	208	VSS
9	DQ2	49	VTT	89	VSS	129	DQ7	169	CKE1	209	DQ44
10	DQ3	50	CKE0	90	DQ40	130	VSS	170	VDD	210	DQ45
11	VSS	51	VDD	91	DQ41	131	DQ12	171	A15	211	VSS
12	DQ8	52	BA2	92	VSS	132	DQ13	172	A14	212	TDQS14
13	DQ9	53	/Err_Out	93	/DQS5	133	VSS	173	VDD	213	/TDQS14
14	VSS	54	VDD	94	DQS5	134	TDQS10	174	A12,/BC	214	VSS
15	/DQS1	55	A11	95	VSS	135	/TDQS10	175	A9	215	DQ46
16	DQS1	56	A7	96	DQ42	136	VSS	176	VDD	216	DQ47
17	VSS	57	VDD	97	DQ43	137	DQ14	177	A8	217	VSS
18	DQ10	58	A5	98	VSS	138	DQ15	178	A6	218	DQ52
19	DQ11	59	A4	99	DQ48	139	VSS	179	VDD	219	DQ53
20	VSS	60	VDD	100	DQ49	140	DQ20	180	A3	220	VSS
21	DQ16	61	A2	101	VSS	141	DQ21	181	A1	221	TDQS15
22	DQ17	62	VDD	102	/DQS6	142	VSS	182	VDD	222	/TDQS15
23	VSS	63	CK1	103	DQS6	143	TDQS11	183	VDD	223	VSS
24	/DQS2	64	/CK1	104	VSS	144	/TDQS11	184	CK0	224	DQ54
25	DQS2	65	VDD	105	DQ50	145	VSS	185	/CK0	225	DQ55
26	VSS	66	VDD	106	DQ51	146	DQ22	186	VDD	226	VSS
27	DQ18	67	VREFCA	107	VSS	147	DQ23	187	/EVENT	227	DQ60
28	DQ19	68	Par_In	108	DQ56	148	VSS	188	A0	228	DQ61
29	VSS	69	VDD	109	DQ57	149	DQ28	189	VDD	229	VSS
30	DQ24	70	A10/AP	110	VSS	150	DQ29	190	BA1	230	TDQS16
31	DQ25	71	BA0	111	/DQS7	151	VSS	191	VDD	231	/TDQS16
32	VSS	72	VDD	112	DQS7	152	TDQS12	192	/RAS	232	VSS
33	/DQS3	73	/WE	113	VSS	153	/TDQS12	193	/S0	233	DQ62



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34	DQS3	74	/CAS	114	DQ58		154	VSS	194	VDD	234	DQ63
35	VSS	75	VDD	115	DQ59		155	DQ30	195	ODT0	235	VSS
36	DQ26	76	/S1	116	VSS		156	DQ31	196	A13	236	VDDSPD
37	DQ27	77	ODT1	117	SA0		157	VSS	197	VDD	237	SA1
38	VSS	78	VDD	118	SCL		158	CB4	198	NC	238	SDA
39	CB0	79	NC	119	SA2		159	CB5	199	VSS	239	VSS
40	CB1	80	VSS	120	VTT		160	VSS	200	DQ36	240	VTT



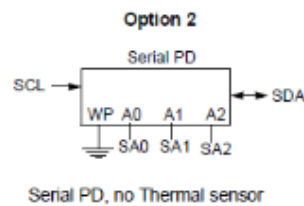
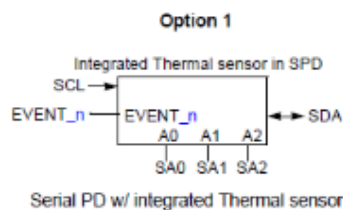
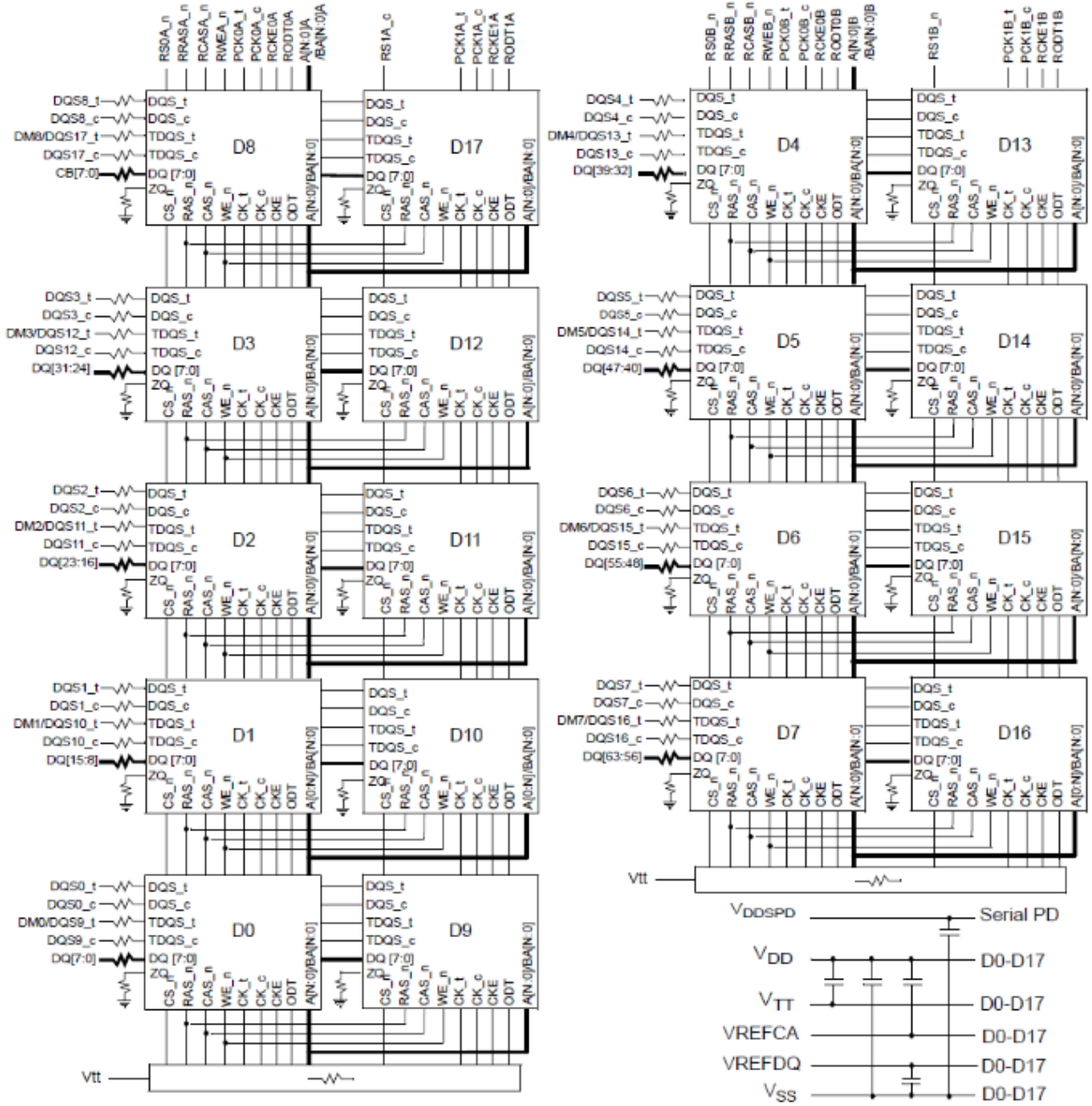
Pin Description :

PIN	NAME	FUNCTION
CK0, /CK0	System Clock	Active on the positive and negative edge to sample all inputs.
CKE0~CKE1	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/S0~/S1	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
A0~A15	Address	Row / Column address are multiplexed on the same pins. (Row Address: A0~A15 , Column Address: A0~A9 , Auto precharge: A10/AP)
BA0~BA2	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ63 CB0~CB7	Data	Data and check bit inputs / outputs are multiplexed on the same pins.
DQS0~DQS8, /DQS0~/DQS8	Data Strobe	Bi-directional Data Strobe
TDQS9~TDQS17, /TDQS9~/TDQS17	Termination Data Strobe	Termination Data Strobe
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
VDD / VSS	Power Supply/Ground	Power and Ground for the input buffers and the core logic.
VREFDQ	Power Supply reference	Power Supply for reference.DQ,DM.VDD/2
VREFCA	Power Supply reference	Power Supply for reference. Command , address, & control.VDD/2
VDDQ	Power Supply	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity
SDA	Serial data I/O	EEPROM serial data I/O



SCL	Serial clock	EEPROM clock input
SA0~SA2	Address in EEPROM	EEPROM address input
ODT0~ODT1	On Die Termination	When high, termination resistance is enabled for all DQ, /DQ and DM pins, assuming the function is enabled in the Extended Mode Register Set.
PAR_IN	Parity input	Parity bit for the command and address bus. ("1 " : Odd, "0 " : Even)
/RESET	Reset	/RESET is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times VDD$ and DC LOW $\leq 0.2 \times VDD$. RESET# assertion and deassertion are asynchronous.
/ERR_OUT	Parity error output:	Parity error found on the command and address bus.
/EVENT	Thermal EVENT	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT pin on TS/SPD part.
NC	No Connection	This pin is recommended to be left No Connection on the device.

Block Diagram :



Absolute Maximum Ratings :

Parameter	Symbol	Value	Unit
Voltage on VDD supply relative to Vss	VDD	-0.4 ~ 1.975	V
Voltage on VDDQ pin relative to Vss	VDDQ	-0.4 ~ 1.975	V
Voltage on any pin relative to Vss	VIN, Vout	-0.4 ~ 1.975	V
Storage temperature	TStg	-55 ~ +100	°C

Note: DDR3 SDRAM component specification.

Operation Temperature Condition

Parameter	Symbol	Value	Unit	Note
Normal Operating Temperature Range	TC	0~+85	°C	1
Extended Temperature Range (Optional)	TC	+85~+95	°C	1

Note: (1) If the DRAM case temperature is above 85 °C, the Auto-Refresh command interval has to be reduced to tREFI=3.9us.

DC Operating Condition :

Voltage referenced to Vss = 0V, VDD&VDDQ=1.35V, Tc = 0 to 85 °C

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	VDD	1.283	1.45	V	1,2
	VDDSPD	3	3.6	V	
Supply Voltage for Output	VDDQ	1.283	1.45	V	1,2
I/O Reference Voltage(CMD/ADD)	VREFCA, (DC)	0.49 x VDD	0.51 x VDD	V	3,4
I/O Reference Voltage(DQ)	VREFDQ, (DC)	0.49 x VDD	0.51 x VDD	V	3,4
Termination Voltage	VTT	VDD/2 - TBD	VDD/2 +TBD	V	

Note: (1) Under all conditions VDDQ must be less than or equal to VDD.

(2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

(3) The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than ±1% VDD

(for reference: approx. ±13.5mV)

(4) For reference: approx. VDD/2 ±13.5mV

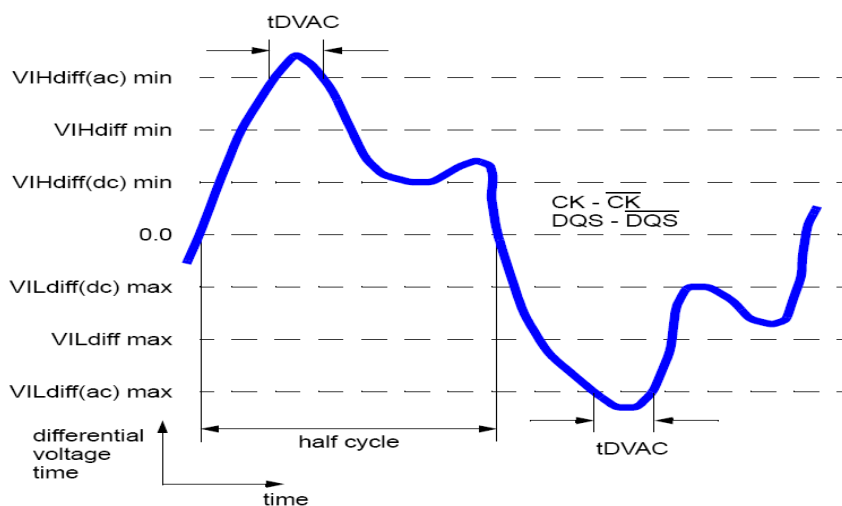
Input DC & AC Logic Level for single-ended signals :

Parameter	Symbol	Min	Max	Unit	Note
DC Input logic high voltage	VIH (DC)	VREF+90	VDD	mV	1
DC Input logic low voltage	VIL (DC)	VSS	VREF-90	mV	1
AC input logic high	VIH(AC)	VREF + 160	-	mV	1,2
AC input logic low	VIL(AC)	-	VREF – 160	mV	1,2

Note: 1. For DQ and DM, VREF = VREFDQ . For input only pins except RESET, or VREF = VREFCA.

2. See "Overshoot and Undershoot specifications" on component datasheet

Definition of differential ac-swing and "time above ac level tDVAC



Input AC Logic Level for differential signals :

Parameter	Symbol	Min	Max	Unit	Note
Differential input high	VIHdiff	+0.18	Note 3	V	1
Differential input low	VILdiff	Note 3	-0.18	V	1
Differential input high AC	VIHdiff(AC)	2 (VIH(ac)-Vref)	Note 3	V	2
Differential input low AC	VILdiff (AC)	Note 3	2 x (VIL(ac) - Vref)	V	2

Notes: 1. Used to define a differential signal slew-rate.

2. For CK - CK use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS, DQSL - DQSL, DQSU - DQSU use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

3. These values are not defined, however they single-ended signals CK, /CK, DQS, /DQS, DQSL, /DQSL, DQSU, /DQSU need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot on Component Datasheet.



IDD Specification :

Symbol	Condition	Typical	Unit
IDD0	Operating One Bank Active-Precharge Current	765	mA
IDD1	Operating One Bank Active-Read-Precharge Current	918	mA
IDD2P0	Precharge Power-Down Current Slow Exit	360	mA
IDD2P1	Precharge Power-Down Current Fast Exit	576	mA
IDD2Q	Precharge Quiet Standby Current	792	mA
IDD2N	Precharge Standby Current	810	mA
IDD3P	Active Power-Down Current	1044	mA
IDD3N	Active Standby Current	1026	mA
IDD4W	Operating Burst Write Current	1485	mA
IDD4R	Operating Burst Read Current	1656	mA
IDD5B	Burst Refresh Current	2070	mA
IDD6	Self Refresh Current: Normal Temperature Range	396	mA
IDD7	Operating Bank Interleave Read Current	2430	mA
IDD8	RESET Low Current	396	mA

Note: IDD current measure method and detail patterns are described on DDR3 component datasheet. Only for reference.

Speed Bins and CL,tRCD,tRP,tRC and tRAS for Corresponding Bin :

Speed	DDR3L-1333	Units
Bin(CL-tRCD-tRP)	9-9-9	
Parameter	Min	
CL	9	tCK
tRCD	13.125	ns
tRC	49.125	ns
tRRD	6	ns
tCK	1.5	ns
tRAS	36	ns
tRP	13.125	ns
tRFC	300	ns

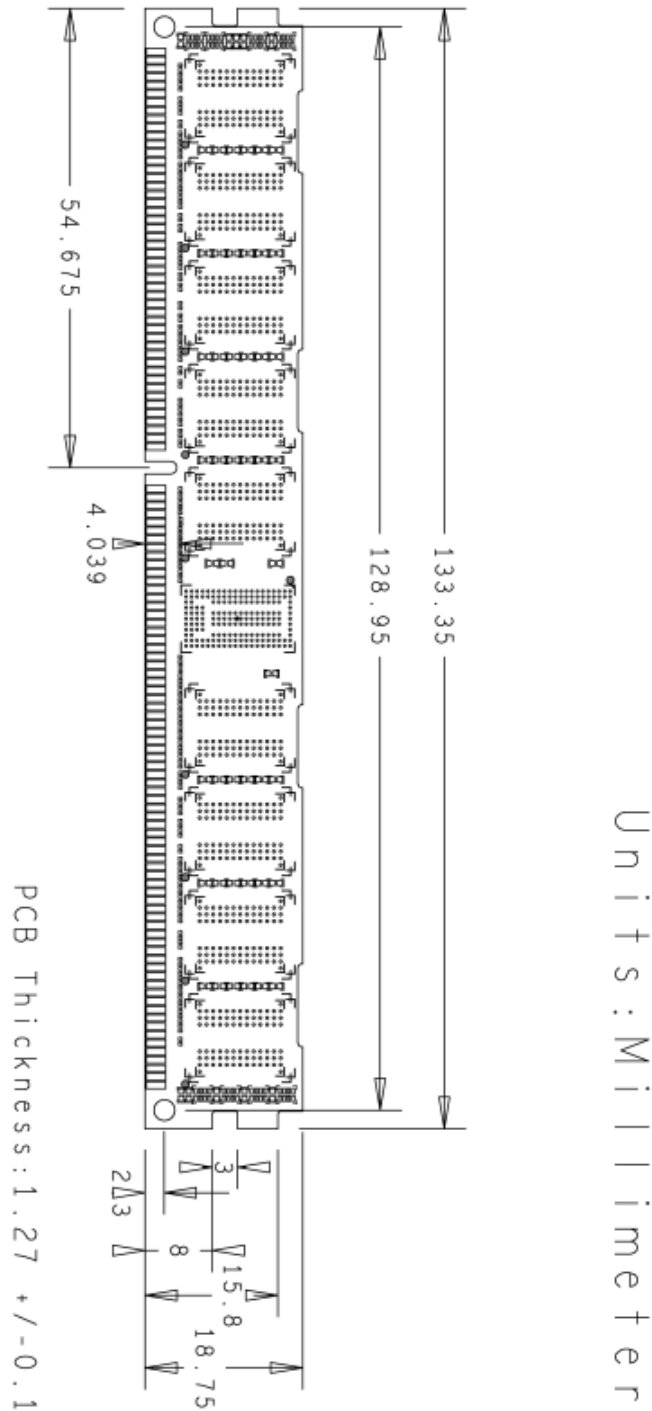
Timing Parameters:

Symbol	AC Characteristics Parameter	Min	Max	Unit
tCK(DLL_OFF)	Minimum Clock Cycle Time (DLL off mode)	8	-	ns
tCH(avg)	Average high pulse width	0.47	0.53	tCK(avg)
tCL(avg)	Average low pulse width	0.47	0.53	tCK(avg)
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	125	ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	30	-	ps
tDH(base)	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	65	-	ps
tDIPW	DQ and DM Input pulse width for each input	400	-	ps
tRPRE	DQS, DQS# differential READ Preamble	0.9	-	tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3	-	tCK(avg)
tQSH	DQS, DQS# differential output high time	0.40	-	tCK(avg)
tQSL	DQS, DQS# differential output low time	0.40	-	tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9	-	tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3	-	tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-255	255	ps
tLZ	DQ, DQS and DQS# low-impedance time	-500	250	ps
tHZ	DQ, DQS and DQS# high-impedance time	-	250	ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.2	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.2	-	tCK(avg)
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	-
tWTR	Delay from start of internal write transaction to internal read command	max(4nCK, 7.5ns)	-	-
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK



tIS(base) AC175	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	65	-	ps
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	140	-	ps
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK,6ns)	-	-
tCKE	CKE minimum pulse width	max(3nCK,5ns)	-	-
tREFI	Average Periodic Refresh interval	85°C < TCASE < 95°C /3.9	0°C < TCASE < 85°C /7.8	us

Package Dimensions :





Ordering Information :

