74AHC74; 74AHCT74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 04 — 7 February 2005 Product data sheet

1. General description

The 74AHC74; 74AHCT74 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC74; 74AHCT74 is a dual positive-edge triggered, D-type flip-flop with individual data (D) inputs, clock (CP) inputs, set ($\overline{S}D$) and reset ($\overline{R}D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input. Information on the data input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features

- Balanced propagation delays
- Inputs accepts voltages higher than V_{CC}
- Input levels:
  - CMOS levels: 74AHC74 only
  - TTL levels: 74AHCT74 only
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74AHC74						
t_{PHL}, t_{PLH}	propagation delay					
	nCP to nQ, n$\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	-	3.7	-	ns
	n$\overline{S}$D, n$\overline{R}$D to nQ, n$\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V	-	3.7	-	ns
f_{max}	maximum clock pulse frequency		-	170	-	MHz

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Table 1: Quick reference data *...continued*

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 3.0$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_I	input capacitance	$V_I = V_{CC}$ or GND		-	4.0	-	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz	[1] [2]	-	12	-	pF
Type 74AHCT74							
t_{PHL}, t_{PLH}	propagation delay						
	nCP to nQ, n$\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V		-	3.3	-	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	C_L = 15 pF; V_{CC} = 5 V		-	3.7	-	ns
f_{max}	maximum clock pulse frequency			-	160	-	MHz
C_I	input capacitance	$V_I = V_{CC}$ or GND		-	4.0	-	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz	[1] [2]	-	16	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC74D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC74PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC74BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT74D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT74PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT74BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

5. Functional diagram

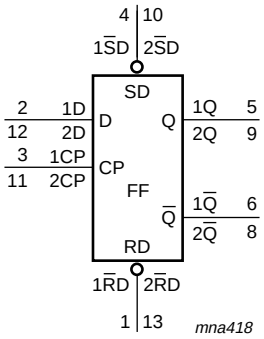


Fig 1. Functional diagram

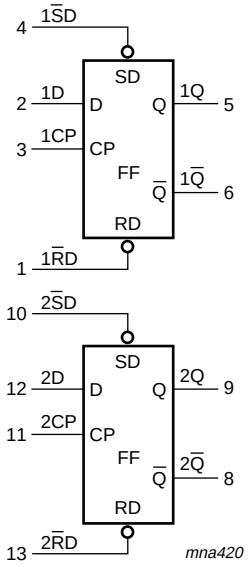


Fig 2. Logic symbol

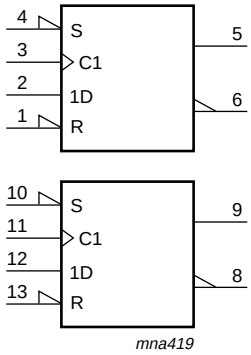


Fig 3. IEC logic symbol

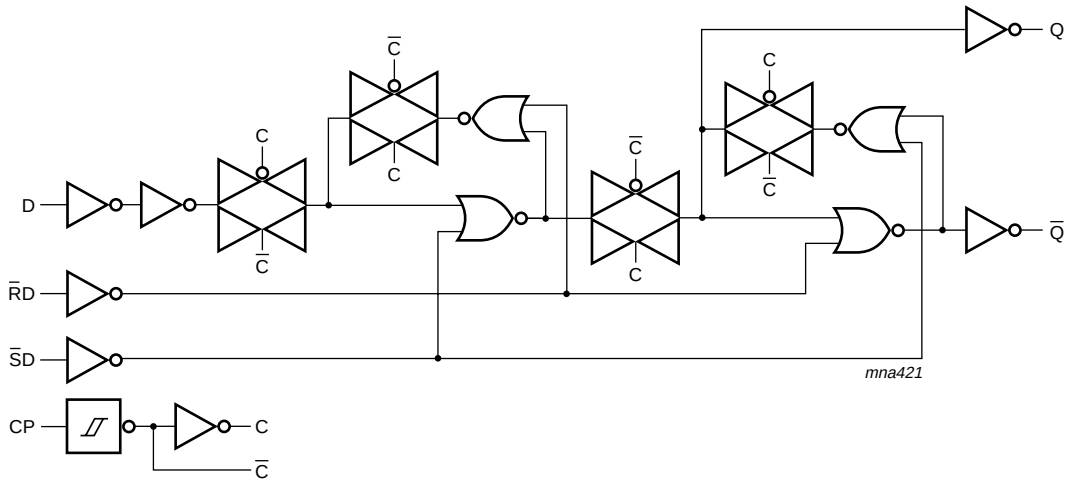


Fig 4. Logic diagram (one flip-flop)

6. Pinning information

6.1 Pinning

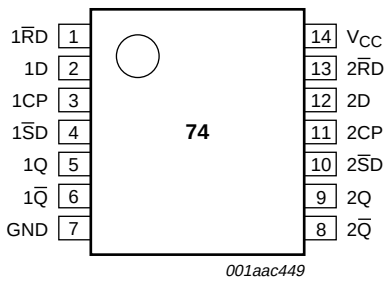
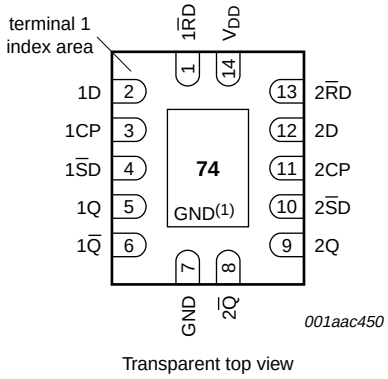


Fig 5. Pin configuration SO14 and TSSOP14



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input

Fig 6. Pin configuration DHVQFN14

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1$\overline{RD}$	1	asynchronous reset-direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH, edge-triggered)

Table 3: Pin description *...continued*

Symbol	Pin	Description
$1\overline{SD}$	4	asynchronous set-direct input (active LOW)
1Q	5	true flip-flop output
$1\overline{Q}$	6	complement flip-flop output
GND	7	ground (0 V)
$2\overline{Q}$	6	complement flip-flop output
2Q	9	true flip-flop output
$2\overline{SD}$	10	asynchronous set-direct input (active LOW)
2CP	11	clock input (LOW-to-HIGH, edge-triggered)
2D	12	data input
$2\overline{RD}$	13	asynchronous reset-direct input (active LOW)
V_{CC}	14	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Input				Output			
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$	nQ_{n+1}	$n\overline{Q}_{n+1}$
L	H	X	X	H	L	L	H
H	L	X	X	L	H	H	L
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition;
X = don't care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input diode current	$V_I < –0.5$ V	[1]	-	–20	mA
I_{OK}	output diode current	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output source or sink current	$V_O = –0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA

Table 5: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{CC}, I_{GND}	V_{CC} or GND current			-	±75	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74AHC74						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 3.3 V ± 0.3 V	-	-	100	ns/V
		V_{CC} = 5 V ± 0.5 V	-	-	20	ns/V
Type 74AHCT74						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 3.3 V ± 0.3 V	-	-	20	ns/V

10. Static characteristics

Table 7: Static characteristics type 74AHC74

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V

Table 7: Static characteristics type 74AHC74 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –50 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = –50 µA; V_{CC} = 3.0 V	2.9	3.0	-	V
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.36	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	0.1	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.25	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2.0	µA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 3.0 V	2.1	-	-	V
		V_{CC} = 5.5 V	3.85	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –50 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –50 µA; V_{CC} = 3.0 V	2.9	-	-	V
		I_O = –50 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.48	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 50 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 3.0 V	-	-	0.44	V
		I_O = 8 mA; V_{CC} = 4.5 V	-	-	0.44	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	1.0	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±2.5	µA

Table 7: Static characteristics type 74AHC74 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	20	µA
C_I	input capacitance		-	-	10	pF
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ µA; $V_{CC} = 2.0$ V	1.9	-	-	V
		$I_O = -50$ µA; $V_{CC} = 3.0$ V	2.9	-	-	V
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4.4	-	-	V
		$I_O = -4.0$ mA; $V_{CC} = 3.0$ V	2.40	-	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.70	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ µA; $V_{CC} = 2.0$ V	-	-	0.1	V
		$I_O = 50$ µA; $V_{CC} = 3.0$ V	-	-	0.1	V
		$I_O = 50$ µA; $V_{CC} = 4.5$ V	-	-	0.1	V
		$I_O = 4$ mA; $V_{CC} = 3.0$ V	-	-	0.55	V
		$I_O = 8$ mA; $V_{CC} = 4.5$ V	-	-	0.55	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	2.0	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±10.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	µA
C_I	input capacitance		-	-	10	pF

Table 8: Static characteristics type 74AHCT74

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5$ V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -50$ µA; $V_{CC} = 4.5$ V	4.4	4.5	-	V
		$I_O = -8.0$ mA; $V_{CC} = 4.5$ V	3.94	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 50$ µA; $V_{CC} = 4.5$ V	-	0	0.1	V
		$I_O = 8$ mA; $V_{CC} = 4.5$ V	-	-	0.36	V

Table 8: Static characteristics type 74AHCT74 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V		-	-	0.1	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V		-	-	±0.25	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V		-	-	2.0	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V		-	-	1.35	mA
C_I	input capacitance			-	3	10	pF
T_{amb} = –40 °C to +85 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –50 µA; V_{CC} = 4.5 V		4.4	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V		3.8	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 50 µA; V_{CC} = 4.5 V		-	-	0.1	V
		I_O = 8 mA; V_{CC} = 4.5 V		-	-	0.44	V
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V		-	-	1.0	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V		-	-	±2.5	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V		-	-	20	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V		-	-	1.5	mA
C_I	input capacitance			-	-	10	pF
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz	[2] [3]	-	16	-	pF
T_{amb} = –40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –50 µA; V_{CC} = 4.5 V		4.4	-	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V		3.70	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 50 µA; V_{CC} = 4.5 V		-	-	0.1	V
		I_O = 8 mA; V_{CC} = 4.5 V		-	-	0.55	V
I_{LI}	input leakage current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V		-	-	2.0	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND per input pin; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V		-	-	±10.0	µA

Table 8: Static characteristics type 74AHCT74 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	40	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND; $I_O = 0$ A; $V_{CC} = 4.5$ V to 5.5 V	-	-	1.5	mA
C_I	input capacitance		-	-	10	pF

11. Dynamic characteristics

Table 9: Dynamic characteristics type 74AHC74

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 9.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C [1]						
t_{PHL}, t_{PLH}	propagation delay					
	nCP to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 7				
		C_L = 15 pF	-	5.2	11.9	ns
		C_L = 50 pF	-	7.4	15.4	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 7				
		C_L = 15 pF	-	3.7	7.3	ns
		C_L = 50 pF	-	5.2	9.3	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 8				
		C_L = 15 pF	-	5.4	12.3	ns
		C_L = 50 pF	-	7.7	15.8	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 8				
		C_L = 15 pF	-	3.7	7.7	ns
		C_L = 50 pF	-	5.3	9.7	ns
f_{max}	maximum clock pulse frequency	V_{CC} = 3.0 V to 3.6 V; see Figure 7				
		C_L = 15 pF	80	125	-	MHz
		C_L = 50 pF	50	75	-	MHz
		V_{CC} = 4.5 V to 5.5 V; see Figure 7				
		C_L = 15 pF	130	170	-	MHz
		C_L = 50 pF	90	115	-	MHz
t_W	pulse width					
	clock pulse HIGH or LOW	C_L = 50 pF; see Figure 7				
		V_{CC} = 3.0 V to 3.6 V	6.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
	set or reset pulse LOW	C_L = 50 pF; see Figure 8				
		V_{CC} = 3.0 V to 3.6 V	6.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns

Table 9: Dynamic characteristics type 74AHC74 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 9.

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
t_{rem}	removal time set or reset	C_L = 50 pF; see Figure 8					
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		3.0	-	-	ns
t_{su}	set-up time nD to nCP	C_L = 50 pF; see Figure 7					
		V_{CC} = 3.0 V to 3.6 V		6.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	ns
t_h	hold time nD to nCP	C_L = 50 pF; see Figure 7					
		V_{CC} = 3.0 V to 3.6 V		0.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	-	-	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz	[2] [3]	-	12	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay						
	nCP to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 7					
		C_L = 15 pF		1.0	-	14.0	ns
		C_L = 50 pF		1.0	-	17.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 7					
		C_L = 15 pF		1.0	-	8.5	ns
		C_L = 50 pF		1.0	-	10.5	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 8					
		C_L = 15 pF		1.0	-	14.5	ns
		C_L = 50 pF		1.0	-	18.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 8					
		C_L = 15 pF		1.0	-	9.0	ns
		C_L = 50 pF		1.0	-	11.0	ns
f_{max}	maximum clock pulse frequency	V_{CC} = 3.0 V to 3.6 V; see Figure 7					
		C_L = 15 pF		45	-	-	MHz
		C_L = 50 pF		70	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V; see Figure 7					
		C_L = 15 pF		110	-	-	MHz
		C_L = 50 pF		75	-	-	MHz
t_W	pulse width						
	clock pulse HIGH or LOW	C_L = 50 pF; see Figure 7					
		V_{CC} = 3.0 V to 3.6 V		7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	ns
	set or reset pulse LOW	C_L = 50 pF; see Figure 8					
		V_{CC} = 3.0 V to 3.6 V		7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	ns

Table 9: Dynamic characteristics type 74AHC74 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 9.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{rem}	removal time set or reset	C_L = 50 pF; see Figure 8				
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.0	-	-	ns
t_{su}	set-up time nD to nCP	C_L = 50 pF; see Figure 7				
		V_{CC} = 3.0 V to 3.6 V	7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
t_h	hold time nD to nCP	C_L = 50 pF; see Figure 7				
		V_{CC} = 3.0 V to 3.6 V	0.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	-	-	ns
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay					
	nCP to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 7				
		C_L = 15 pF	1.0	-	15.0	ns
		C_L = 50 pF	1.0	-	19.5	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 7				
		C_L = 15 pF	1.0	-	9.5	ns
		C_L = 50 pF	1.0	-	12.0	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	V_{CC} = 3.0 V to 3.6 V; see Figure 8				
		C_L = 15 pF	1.0	-	15.5	ns
		C_L = 50 pF	1.0	-	20.0	ns
		V_{CC} = 4.5 V to 5.5 V; see Figure 8				
		C_L = 15 pF	1.0	-	10.0	ns
		C_L = 50 pF	1.0	-	12.5	ns
f_{max}	maximum clock pulse frequency	V_{CC} = 3.0 V to 3.6 V; see Figure 7				
		C_L = 15 pF	45	-	-	MHz
		C_L = 50 pF	70	-	-	MHz
		V_{CC} = 4.5 V to 5.5 V; see Figure 7				
		C_L = 15 pF	110	-	-	MHz
		C_L = 50 pF	75	-	-	MHz
t_W	pulse width					
	clock pulse HIGH or LOW	C_L = 50 pF; see Figure 7				
		V_{CC} = 3.0 V to 3.6 V	7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
	set or reset pulse LOW	C_L = 50 pF; see Figure 8				
		V_{CC} = 3.0 V to 3.6 V	7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
t_{rem}	removal time set or reset	C_L = 50 pF; see Figure 8				
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	3.0	-	-	ns

Table 9: Dynamic characteristics type 74AHC74 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; see Figure 9.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{su}	set-up time nD to nCP	C_L = 50 pF; see Figure 7				
		V_{CC} = 3.0 V to 3.6 V	7.0	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	ns
t_h	hold time nD to nCP	C_L = 50 pF; see Figure 7				
		V_{CC} = 3.0 V to 3.6 V	0.5	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	-	-	ns

[1] Typical values are measured at nominal V_{CC}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[3] The condition is V_I = GND to V_{CC}.

Table 10: Dynamic characteristics type 74AHCT74

GND = 0 V; $t_r = t_f \leq 3.0$ ns; V_{CC} = 4.5 V to 5.5 V; see Figure 9

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C [1]							
t_{PHL}, t_{PLH}	propagation delay						
	nCP to nQ, n$\overline{Q}$	see Figure 7					
		C_L = 15 pF		-	3.3	7.8	ns
		C_L = 50 pF		-	4.8	8.8	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	see Figure 8					
		C_L = 15 pF		-	3.7	10.4	ns
		C_L = 50 pF		-	5.3	11.4	ns
f_{max}	maximum clock pulse frequency	see Figure 7					
		C_L = 15 pF		100	160	-	MHz
		C_L = 50 pF		80	140	-	MHz
t_W	pulse width						
	clock pulse HIGH or LOW	C_L = 50 pF; see Figure 7		5.0	-	-	ns
	set or reset pulse LOW	C_L = 50 pF; see Figure 7		5.0	-	-	ns
t_{rem}	removal time set or reset	C_L = 50 pF; see Figure 8		3.5	-	-	ns
t_{su}	set-up time nD to nCP	C_L = 50 pF; see Figure 7		5.0	-	-	ns
t_h	hold time nD to nCP	see Figure 7		0	-	-	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz	[2] [3]	-	16	-	pF

Table 10: Dynamic characteristics type 74AHCT74 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; $V_{CC} = 4.5$ V to 5.5 V; see Figure 9

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay					
	nCP to nQ, n$\overline{Q}$	see Figure 7				
		C_L = 15 pF	1.0	-	9.0	ns
		C_L = 50 pF	1.0	-	10.0	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	see Figure 8				
		C_L = 15 pF	1.0	-	12.0	ns
		C_L = 50 pF	1.0	-	13.0	ns
f_{max}	maximum clock pulse frequency	see Figure 7				
		C_L = 15 pF	80	-	-	MHz
		C_L = 50 pF	65	-	-	MHz
t_W	pulse width					
	clock pulse HIGH or LOW	C_L = 50 pF; see Figure 7	5.0	-	-	ns
	set or reset pulse LOW	C_L = 50 pF; see Figure 7	5.0	-	-	ns
t_{rem}	removal time set or reset	C_L = 50 pF; see Figure 8	3.5	-	-	ns
t_{su}	set-up time nD to nCP	C_L = 50 pF; see Figure 7	5.0	-	-	ns
t_h	hold time nD to nCP	see Figure 7	0	-	-	ns
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay					
	nCP to nQ, n$\overline{Q}$	see Figure 7				
		C_L = 15 pF	1.0	-	10.0	ns
		C_L = 50 pF	1.0	-	11.0	ns
	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$	see Figure 8				
		C_L = 15 pF	1.0	-	13.0	ns
		C_L = 50 pF	1.0	-	14.5	ns
f_{max}	maximum clock pulse frequency	see Figure 7				
		C_L = 15 pF	80	-	-	MHz
		C_L = 50 pF	65	-	-	MHz
t_W	pulse width					
	clock pulse HIGH or LOW	C_L = 50 pF; see Figure 7	5.0	-	-	ns
	set or reset pulse LOW	C_L = 50 pF; see Figure 7	5.0	-	-	ns

Table 10: Dynamic characteristics type 74AHCT74 *…continued*

GND = 0 V; $t_r = t_f \leq 3.0$ ns; $V_{CC} = 4.5$ V to 5.5 V; see Figure 9

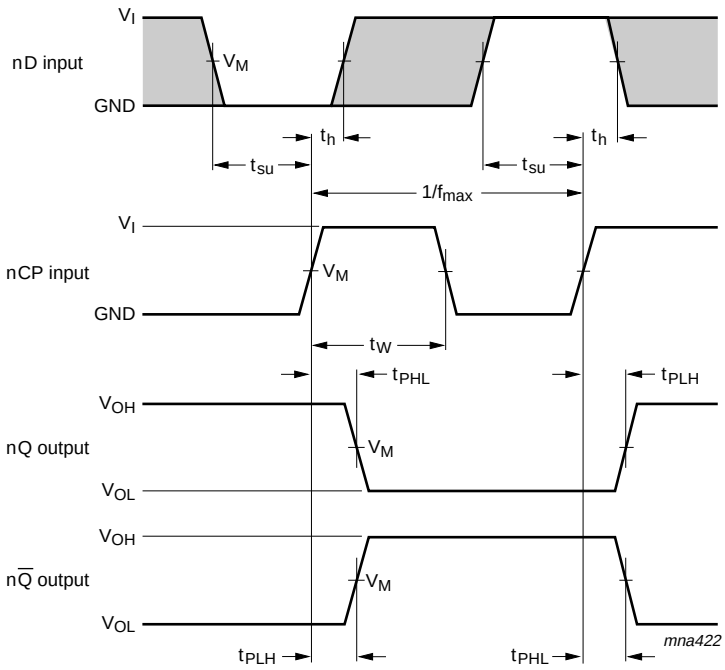
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
t_{rem}	removal time set or reset	C_L = 50 pF; see Figure 8	3.5	-	-	ns
t_{su}	set-up time nD to nCP	C_L = 50 pF; see Figure 7	5.0	-	-	ns
t_h	hold time nD to nCP	see Figure 7	0	-	-	ns

[1] Typical values are measured at V_{CC} = 5.0 V.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

[3] The condition is V_I = GND to V_{CC}.

12. Waveforms

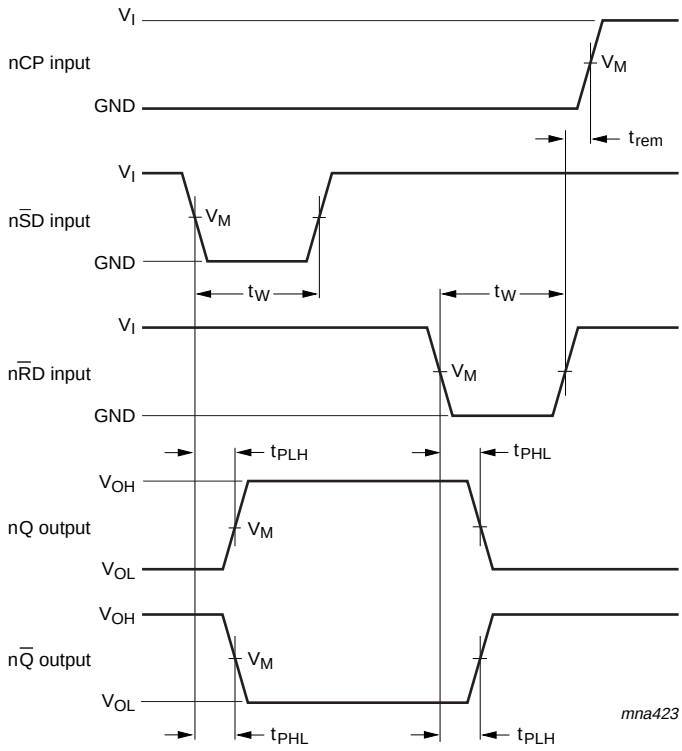


Measurement points are given in Table 11.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 7. The clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nD to nCP set-up times, the nCP to nD hold times and the maximum clock pulse frequency



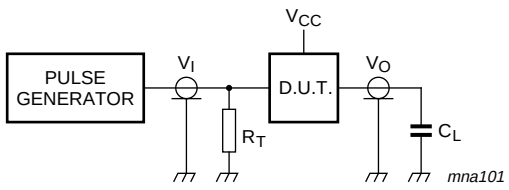
Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 8. The set (nSD) and reset (nRD) input to output (nQ, nQ) propagation delays, the set and reset pulse widths and the nRD to nCP removal time

Table 11: Measurement points

Type	Input	Output
	V_M	V_M
74AHC74	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT74	1.5 V	$0.5 \times V_{CC}$



For test data see Table 12.

Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

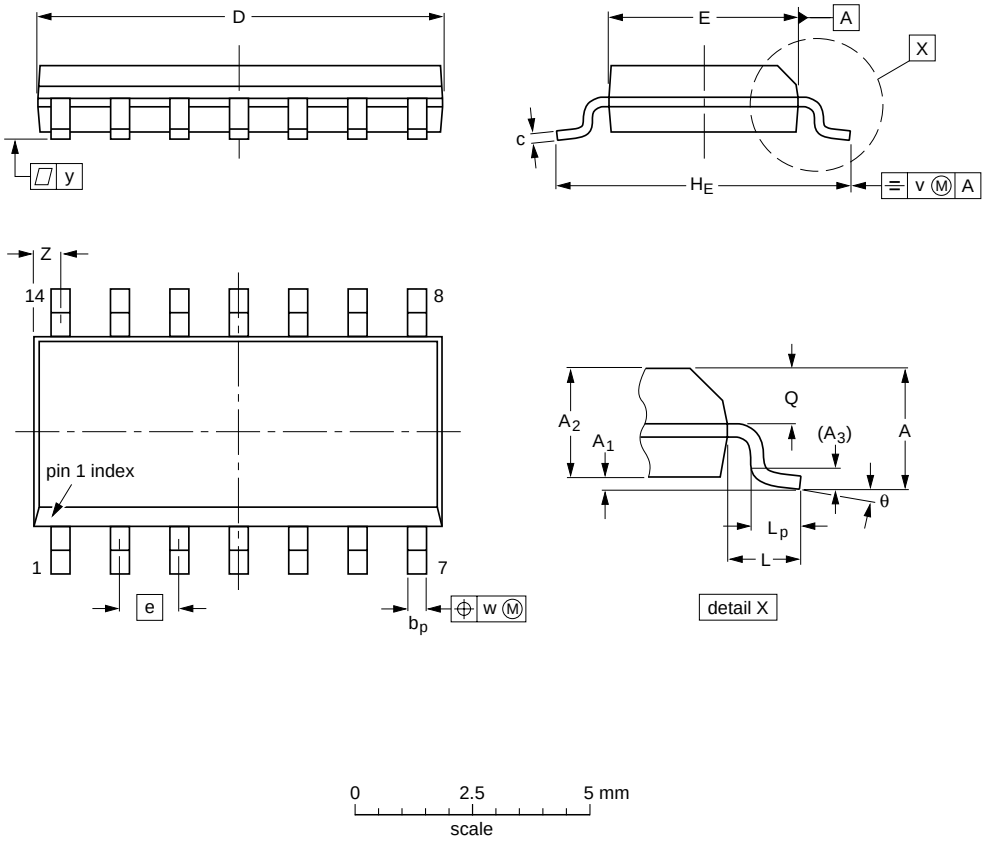
Fig 9. Load circuitry for switching times

Table 12: Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC74	V_{CC}	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}
74AHCT74	3.0 V	≤ 3.0 ns	50 pF, 15 pF	t_{PLH}, t_{PHL}

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

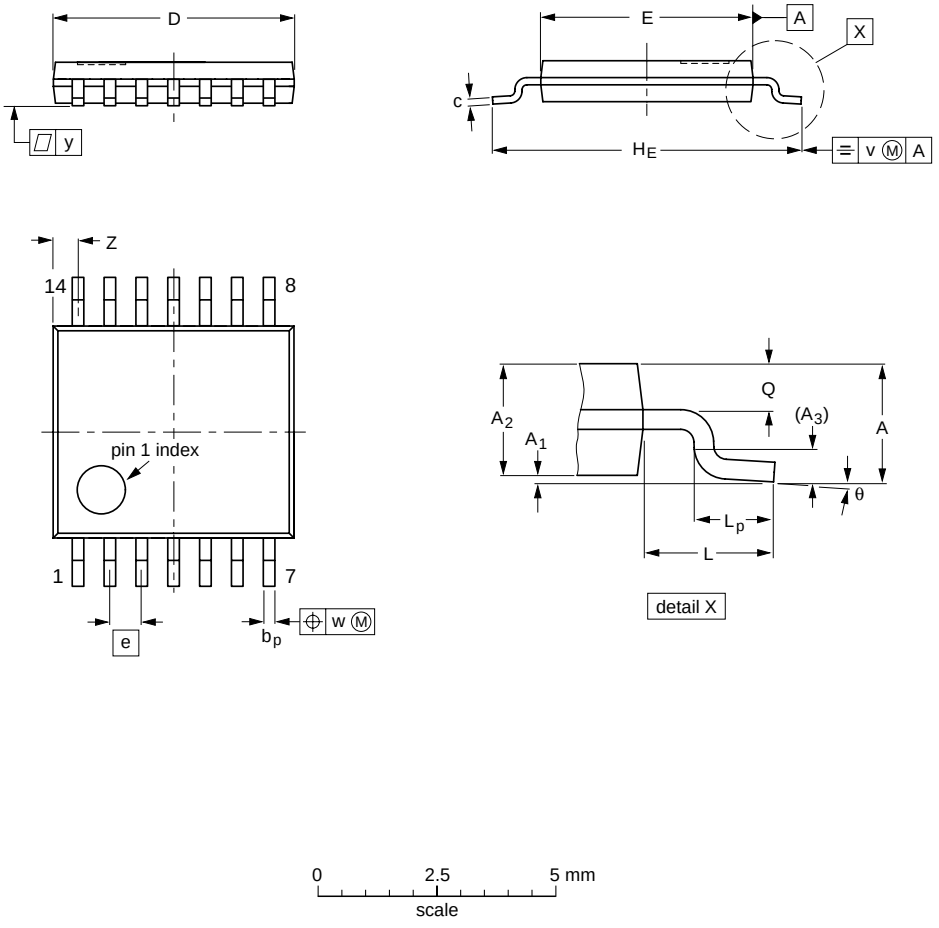
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

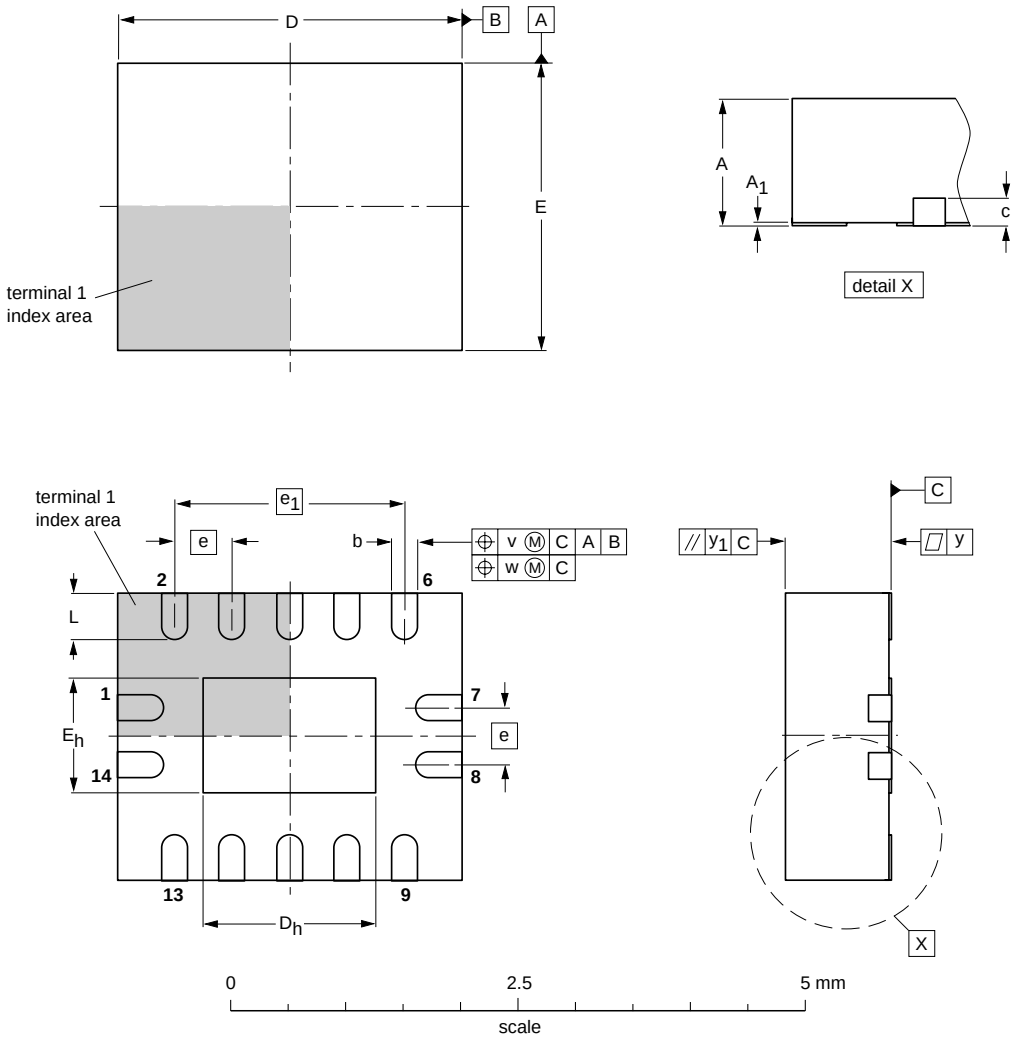
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 12. Package outline SOT762-1 (DHVQFN14)

14. Revision history

Table 13: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74AHC_AHCT74_4	20050207	Product data sheet	-	9397 750 14504	74AHC_AHCT74_3
Modifications:	• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Added: type numbers 74AHC74BQ and 74AHCT74BQ (DHVQFN14 package).				
74AHC_AHCT74_3	20040429	Product specification	-	9397 750 13118	74AHC_AHCT74_2
74AHC_AHCT74_2	19990923	Product specification	-	9397 750 06291	74AHC_AHCT74_1
74AHC_AHCT74_1	19990805	Product specification	-	9397 750 05747	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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