DATA SHEET

LinearDimensions SEMICONDUCTOR

LND-SP64HV

32MHZ, 64 CHANNEL SERIAL TO PARALLEL CONVERTER WITH PUSH-PULL OUTPUTS

Features

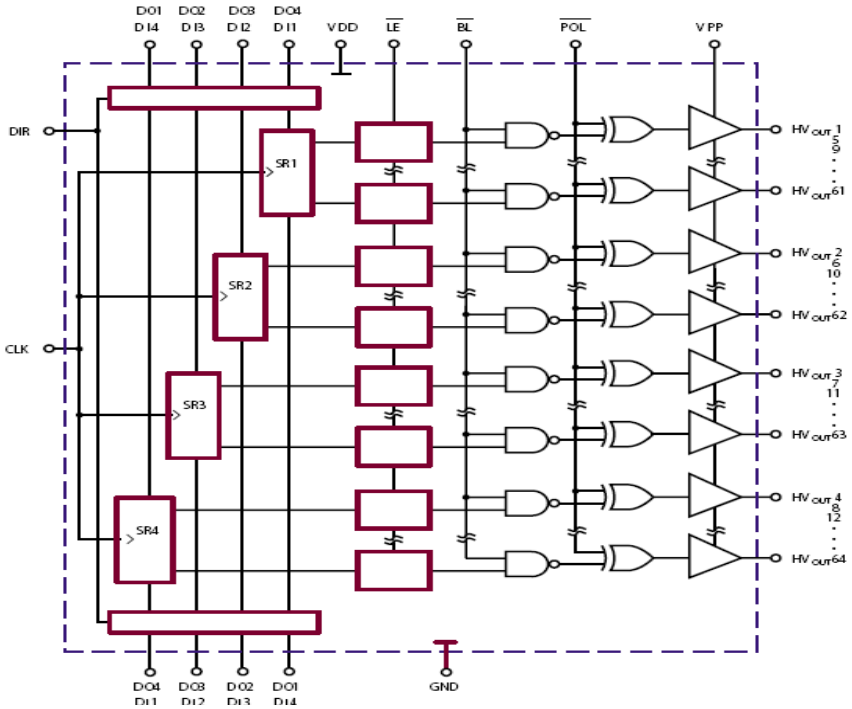
- HVCMOS® Technology
- 5.0V CMOS Logic
- Output voltage up to +90V
- Low power level shifting
- 32MHz equivalent data rate
- Latched data outputs
- Forward and reverse shifting options (DIR pin)
- Diode to V_{PP} allows efficient power recovery
- Outputs may be hot switched
- Hi-Rel processing available

General Description

The LND-SP64HV is a low voltage serial to high voltage parallel converter with push-pull outputs. The device has been designed for use as a driver for EL displays. It can also be used in any application requiring multiple output high voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 4 parallel 16-bit registers, permitting data rates 4x the speed of one (they are clocked together). There are also 64 latches and control logic to perform the polarity select and blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}64$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ input is high. The data in the latches is stored when the $\overline{LE}$ is low.

Functional Block Diagram



Ordering Information

Device	Package Options
	80-Lead PQFP *20.00x14.00mm body* *3.40mm height (max)* *0.80mm pitch*
LND-SP64HV	LND-SP64HV-PG-G

-G indicates package is ROHS compliant ('Green')

Pin Configuration

80-Lead PQFP (PG)
(top view)

Absolute Maximum Ratings

Parameter	Value
Supply voltage, V_{DD}	-0.5V to +5.5V
Output voltage, V_{PP}	-0.5V to +90V
Logic input levels	-0.3V to V_{DD}+0.3V
Ground current[1]	1.5A
Continuous total power dissipation[2]	1200mW
Operating temperature range	-40°C to +85°C
Storage temperature range	-65°C to 150°C
Lead temperature[3]	260°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

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Notes:

1. *Limited by the total power dissipated in the package*
2. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C.*
3. *1.6mm(1/16inch) from case for 10 seconds*

Recommended Operating conditions

Sym	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output voltage	8.0	90	V
V_{IH}	High-level input voltage	V_{DD}-0.5V	–	V
V_{IL}	Low-level input voltage	0	0.5	V
f_{CLK}	Clock frequency per register	–	8.0	MHz
T_A	Operating free-air temperature	-40	+85	°C

Notes:

Power-up sequence should be the following:

1. Apply ground.
2. Apply V_{DD}.
3. Set all inputs (D_{IN}, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.
5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above

DC Electrical Characteristics

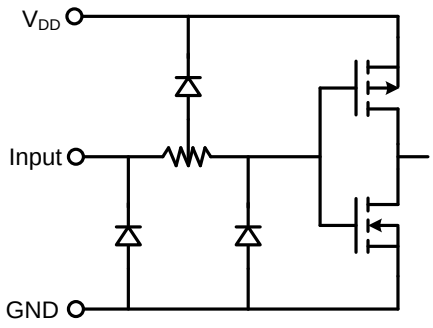
Sym	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current		–	15	mA	$V_{DD} = V_{DD}max, f_{CLK} = 8.0MHz$
I_{PP}	High voltage supply current		–	100	µA	Outputs high
			–	100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current		–	100	µA	All $V_{IN} = V_{DD}$
V_{OH}	High level output	HV_{OUT}	75	–	V	$I_O = -15mA, V_{PP} = +90V$
		Data out	V_{DD}–0.5	–	V	$I_O = -100µA$
V_{OL}	Low level output	HV_{OUT}	–	7.0	V	$I_O = 12mA, V_{PP} = +90V$
		Data out	–	0.5	V	$I_O = 100µA$
I_{IH}	High-level logic input current		–	1.0	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current		–	-1.0	µA	$V_{IL} = 0V$
V_{OC}	High voltage clamp diode		–	1.0	V	$I_{OC} = 1.0mA$

AC Electrical Characteristics *(T_A =85° C max, Logic signals and Data inputs have t_r, $t_f \leq$ 5ns[10% and 90% points]).*

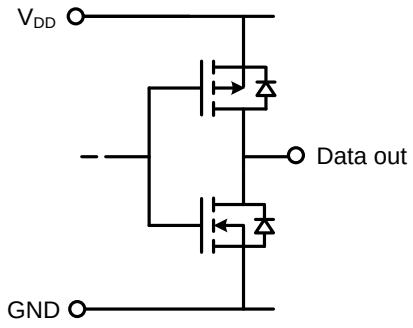
Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	–	8.0	MHz	Per register
t_{WL}, t_{WH}	Clock width high or low	62	–	ns	---
t_{SU}	Data set-up time before clock rises	10	–	ns	---
t_H	Data hold time after clock rises	15	–	ns	---
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}	–	200	ns	$C_L = 15pF$
t_{DHL}	Delay time clock to data high to low	–	70	ns	$C_L = 15pF$
t_{DLH}	Delay time clock to data low to high	–	70	ns	$C_L = 15pF$
t_{DLE}*	Delay time clock to $\overline{LE}$ low to high	25	–	ns	---
t_{WLE}	$\overline{LE}$ pulse widthOutput Turn-off Delay	25	–	ns	---
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0	–	ns	---

** t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize)*

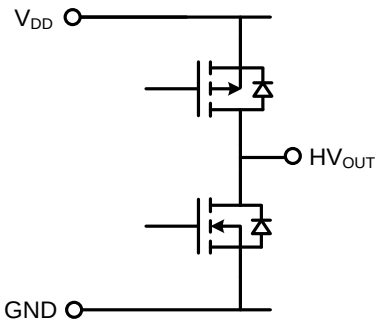
Input and Output Equivalent Circuits



Logic Inputs



Logic Data Output



High Voltage Outputs