M81722FP

HIGH VOLTAGE HALF BRIDGE DRIVER

DESCRIPTION

M81722FP is high voltage Power MOSFET and IGBT driver for half bridge applications.

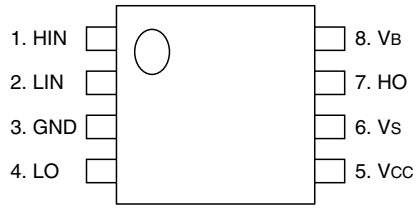
FEATURES

- FLOATING SUPPLY VOLTAGE 600V
- OUTPUT CURRENT ..... ±3A (typ)
- UNDERVOLTAGE LOCKOUT
- INPUT FILTER
- SOP-8 PACKAGE

APPLICATIONS

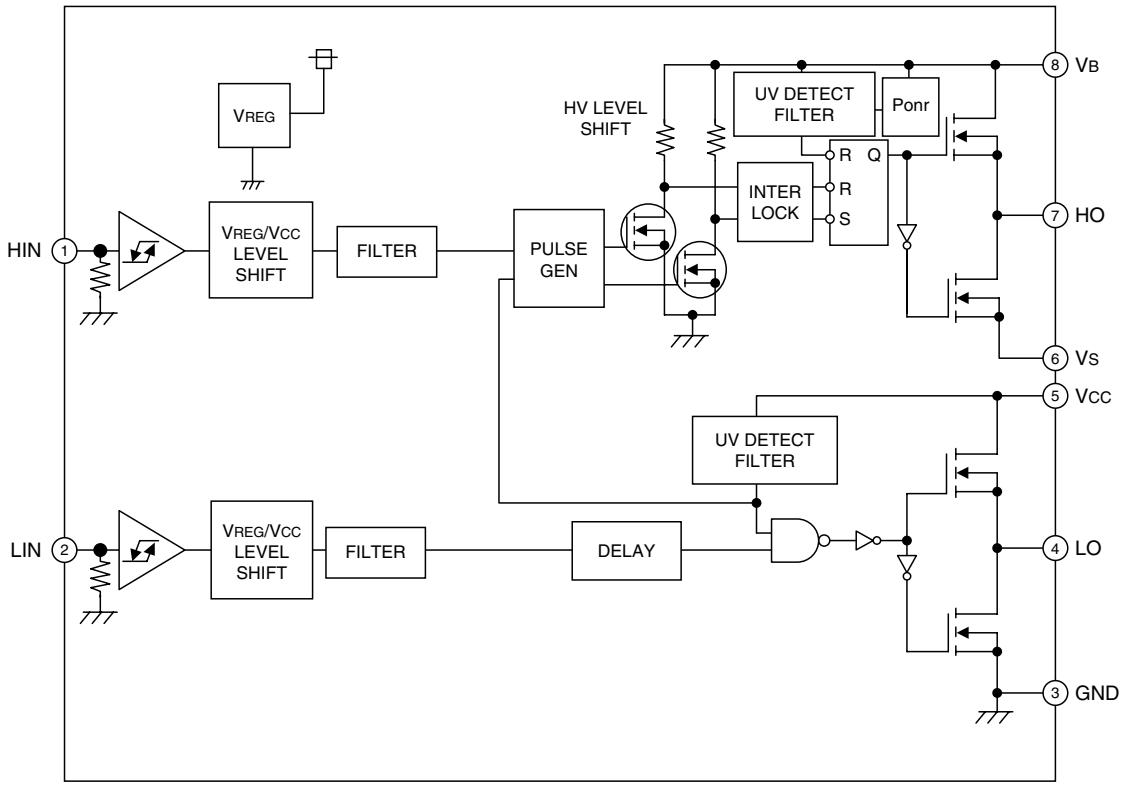
MOSFET and IGBT driver for PDP,HID lamp, refrigerator, air-conditioner, washing machine, AC-servomotor and general purpose.

PIN CONFIGURATION (TOP VIEW)



Outline:8P2S

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (Ta=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Ratings	Unit
V_B	High Side Floating Supply Absolute Voltage		–0.5 ~ 624	V
V_S	High Side Floating Supply Offset Voltage		V_B-24 ~ V_B+0.5	V
V_{BS}	High Side Floating Supply Voltage	V_{BS} = V_B-V_S	–0.5 ~ 24	V
V_{HO}	High Side Output Voltage		V_S–0.5 ~ V_B+0.5	V
V_{CC}	Low Side Fixed Supply Voltage		–0.5 ~ 24	V
V_{LO}	Low Side Output Voltage		–0.5 ~ V_{CC}+0.5	V
V_{IN}	Logic Input Voltage	HIN, LIN	–0.5 ~ V_{CC}+0.5	V
Pd	Package Power Dissipation	Ta = 25°C , On Board	0.6	W
Kθ	Linear Derating Factor	Ta > 25°C , On Board	4.8	mW/°C
Rth(j-c)	Junction - Case Thermal Resistance		50	°C/W
Tj	Junction Temperature		–20 ~ 150*	°C
Topr	Operation Temperature		–20 ~ 125	°C
Tstg	Storage Temperature		–40 ~ 150	°C
T_L	Solder heat-proof(flow)	For RoHS	260 (10s)	°C

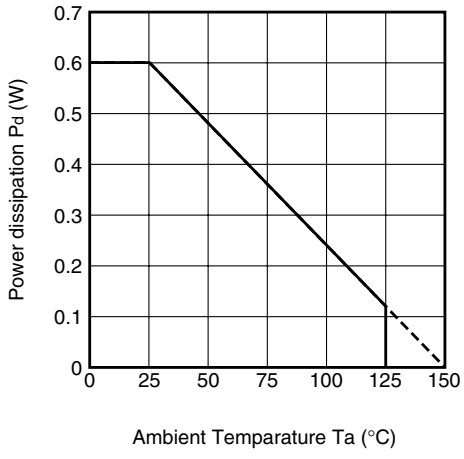
* Please adjust the V_S potential to 500V or less when the junction temperature (Tj) exceeds 125°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_B	High Side Floating Supply Absolute Voltage		V_S+10	—	V_S+20	V
V_S	High Side Floating Supply Offset Voltage	V_B > 10V	–5	—	500	V
V_{BS}	High Side Floating Supply Voltage	V_{BS} = V_B-V_S	10	—	20	V
V_{HO}	High Side Output Voltage		V_S	—	V_B	V
V_{CC}	Low Side Fixed Supply Voltage		10	—	20	V
V_{LO}	Logic Supply Voltage		0	—	V_{CC}	V
V_{IN}	Logic Input Voltage	HIN, LIN	0	—	7	V

* For proper operation, the device should be used within the recommended conditions.

THERMAL DERATING FACTOR CHARACTERISTIC (ABSOLUTE MAXIMUM RATINGS)

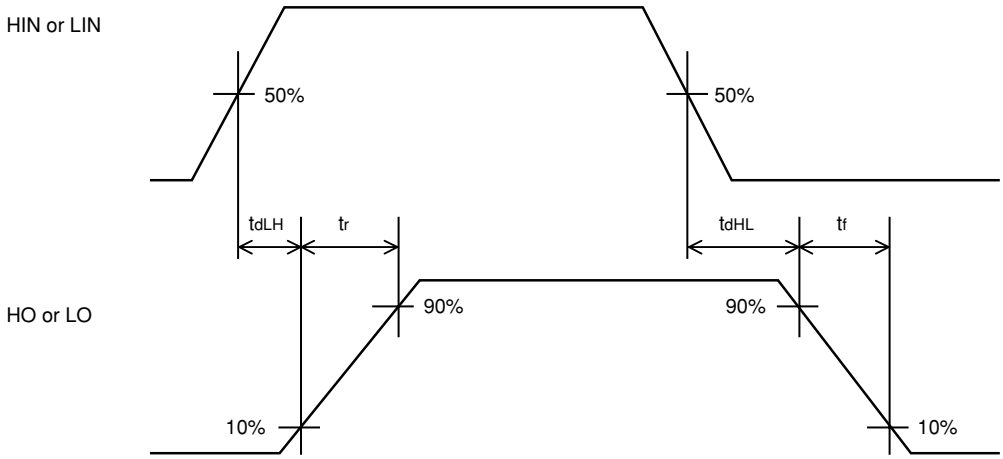


ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vcc=VBS(=VB-VS)=15V, unless otherwise specified)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.*	Max.	
I_{FS}	Floating Supply Leakage Current	V_B = V_S = 600V	—	—	1.0	μA
I_{BS}	V_{BS} standby Current	HIN = LIN = 0V	—	0.2	0.5	mA
I_{CC}	Vcc standby Current	HIN = LIN = 0V	—	0.6	1.0	mA
V_{OH}	High Level Output Voltage	I_O = 0A, LO, HO	13.8	14.4	—	V
V_{OL}	Low Level Output Voltage	I_O = 0A, LO, HO	—	—	0.1	V
V_{IH}	High Level Input Threshold Voltage	HIN, LIN	4.0	—	—	V
V_{IL}	Low Level Input Threshold Voltage	HIN, LIN	—	—	0.8	V
I_{IH}	High Level Input Bias Current	V_{IN} = 5V	—	17	40	μA
I_{IL}	Low Level Input Bias Current	V_{IN} = 0V	—	—	1	μA
V_{BSuvr}	V_{BS} Supply UV Reset Voltage		8.0	8.9	9.8	V
V_{BSuvh}	V_{BS} Supply UV Hysteresis Voltage		0.3	0.7	—	V
t_{VBSuv}	V_{BS} Supply UV Filter Time		—	7.5	—	μs
V_{CCuvr}	Vcc Supply UV Reset Voltage		8.0	8.9	9.8	V
V_{CCuvh}	Vcc Supply UV Hysteresis Voltage		0.3	0.7	—	V
t_{VCCuv}	Vcc Supply UV Filter Time		—	7.5	—	μs
V_{Ponr}	Power-On Reset Voltage		—	—	6.0**	V
tP_{onr}(FIL)	Power-On Reset Filter Time		300**	—	—	ns
I_{OH}	Output High Level Short Circuit Pulsed Current	V_O = 0V, V_{IN} = 5V, PWD < 10μ s	2.0	3.0	—	A
I_{OL}	Output Low Level Short Circuit Pulsed Current	V_O = 15V, V_{IN} = 0V, PWD < 10μs	2.0	3.0	—	A
R_{OH}	Output High Level On Resistance	I_O = -200mA, R_{OH} = (V_{OH}-V_O) /I_O	—	10	20	Ω
R_{OL}	Output Low Level On Resistance	I_O = 200mA, R_{OL} = V_O / I_O	—	2.5	3.0	Ω
$t_{dLH(HO)}$	High Side Turn-On Propagation Delay	CL = 1000pF between HO-Vs	—	200	280	ns
$t_{dHL(HO)}$	High Side Turn-Off Propagation Delay	CL = 1000pF between HO-Vs	—	180	260	ns
t_{rH}	High Side Turn-On Rise Time	CL = 1000pF between HO-Vs	—	25	45	ns
t_{fH}	High Side Turn-Off Fall Time	CL = 1000pF between HO-Vs	—	20	35	ns
$t_{dLH(LO)}$	Low Side Turn-On Propagation Delay	CL = 1000pF between LO-GND	—	200	280	ns
$t_{dHL(LO)}$	Low Side Turn-Off Propagation Delay	CL = 1000pF between LO-GND	—	180	260	ns
t_{rL}	Low Side Turn-On Rise Time	CL = 1000pF between LO-GND	—	25	45	ns
t_{fL}	Low Side Turn-Off Fall Time	CL = 1000pF between LO-GND	—	20	35	ns
Δt_{dLH}	Delay Matching,High Side and Low Side Turn-On	|tdLH (HO) -tdLH (LO)|	—	0	30	ns
Δt_{dHL}	Delay Matching,High Side and Low Side Turn-Off	|tdHL (HO) -tdHL (LO)|	—	0	30	ns
IN(FIL)	Input Filter Time	CONVEX PULSE : HIN, LIN	—	100	—	ns
		CONCAVE PULSE : HIN, LIN	—	100	—	ns

* Typ. is not specified
** High Side Circuit Only

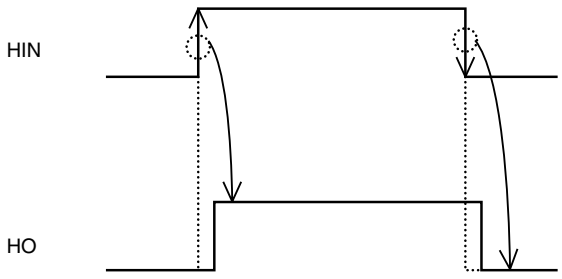
TIMING REQUIREMENT



FUNCTION TABLE

HIN	LIN	VBS UV	VCC UV	HO	LO	Behavioral state
H→L	L	H	H	L	L	LO = HO = Low
H→L	H	H	H	L	H	LO = High
L→H	L	H	H	H	L	HO = High
L→H	H	H	H	H	H	LO = HO = High
X	L	L	H	L	L	HO = Low, VBS UV tripped
X	H	L	H	L	H	LO = High, VBS UV tripped
H→L	X	H	L	L	L	LO = Low, Vcc UV tripped
L→H	X	H	L	L	L	HO = LO = Low, Vcc UV tripped

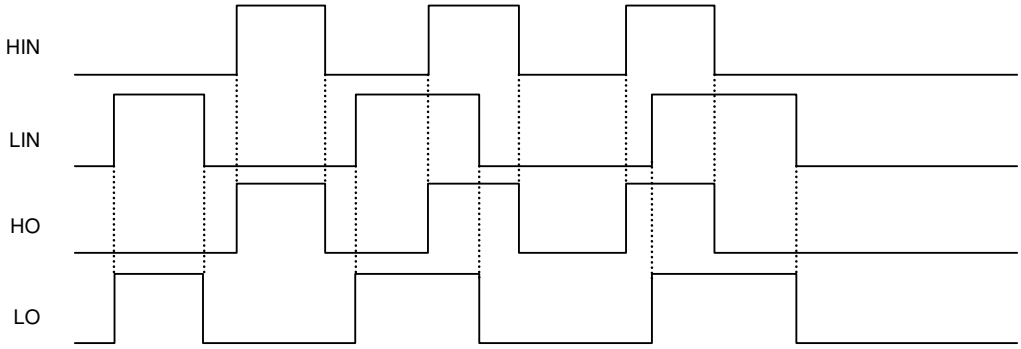
Note1 : “L” state of VBS UV, Vcc UV means that UV trip voltage.
2 : When input signal (HIN and LIN) is "H" at the same time, then output signal (Both HO and LO) is “H”.
3 : X(HIN) : L→H or H→L.X(LIN) : H or L.
4 : Output signal (HO) is triggered by the edge of input signal.



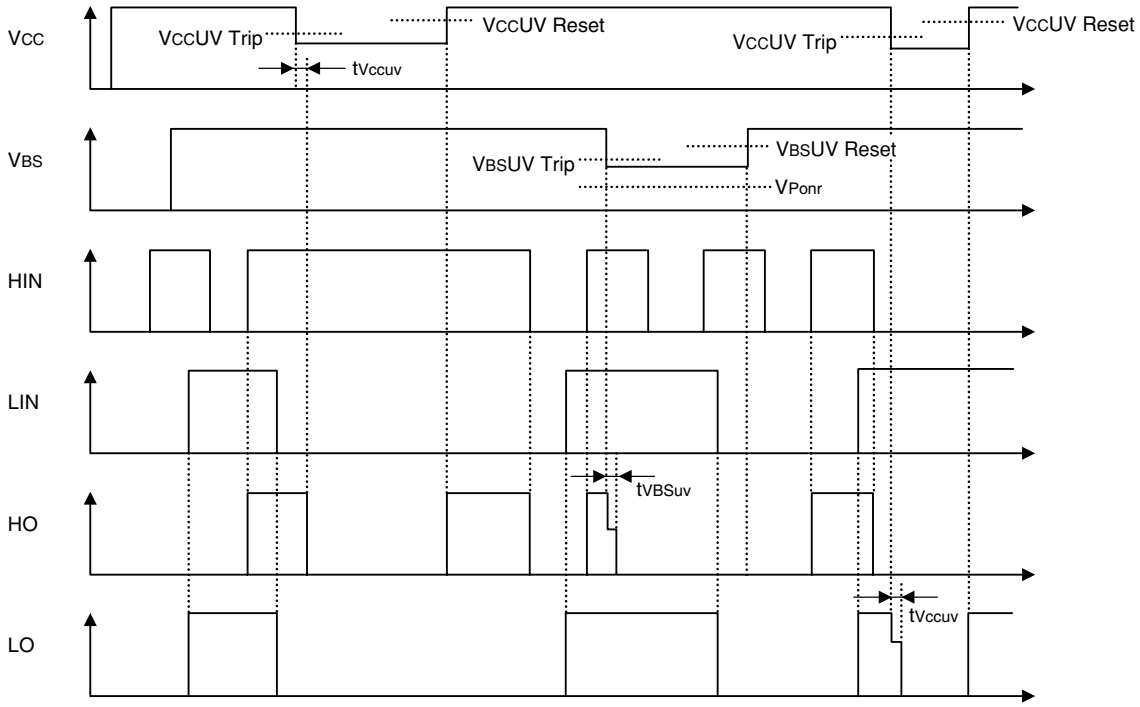
TIMING DIAGRAM

1. Input/Output Timing Diagram

HIGH ACTIVE (When input signal (HIN or LIN) is “H”, then output signal (HO or LO) is “H”.)
Because there is not interlock circuit, in the case of both input signals (HIN and LIN) are “H”, output signals (HO and LO) become “H”.



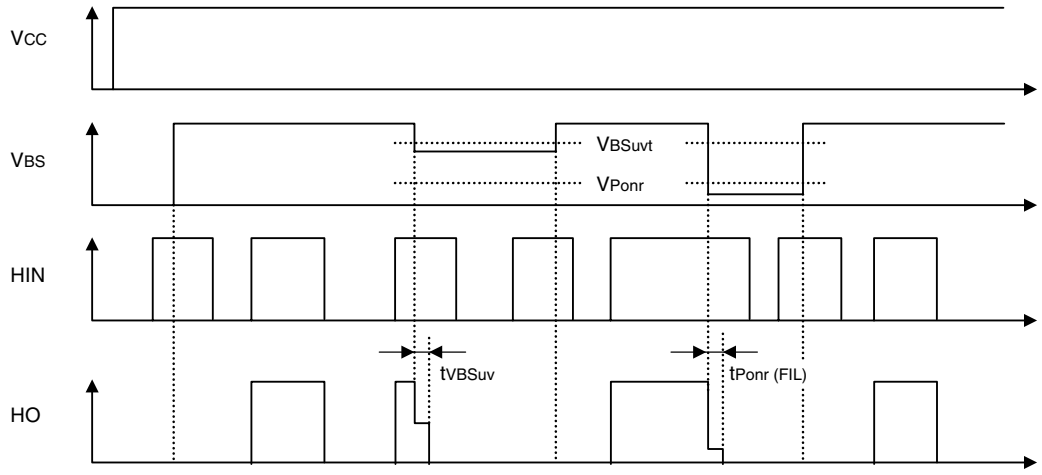
2. Operation sequence Diagram



• Logic During UV Error

Error Signal	HO	LO
UV Error (V_{CC})	HO is locked at "L" Level during V_{CC} UV error is detected. HO responds to HIN ,if V_{CC} exceeds V_{CC} UV reset level.	LO is locked at "L" Level during V_{CC} UV error is detected. LO responds to LIN ,if V_{CC} exceeds V_{CC} UV reset level.
UV Error (V_{BS})	HO is locked at "L" Level during V_{CC} UV error is detected. After V_{BS} exceeds V_{BS} UV reset level, the undervoltage lockout of HO is removed by "L"input signal of HIN,and then HO responds to the input signal.	LO responds to LIN even if V_{BS} voltage is UV error.

3. Ponr sequence Diagram



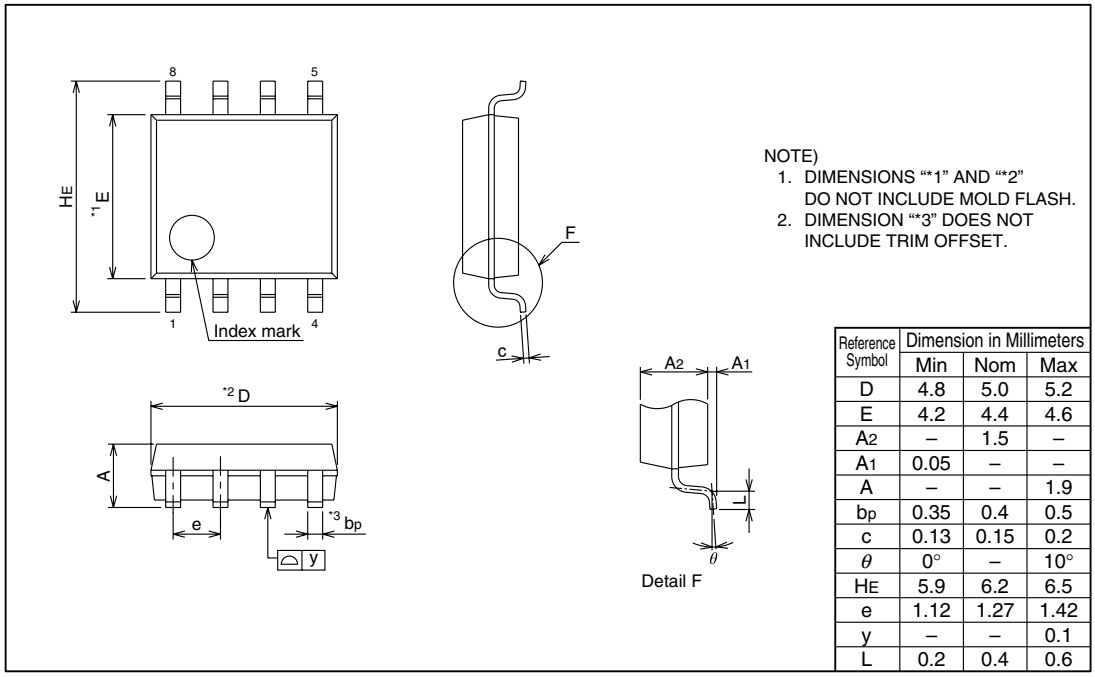
* When supply voltage is lower than V_{ponr}, then output will go low after tP_{onr}(FIL).

4. Allowable supply voltage transient
It is recommended to supply Vcc firstly and supply V_{BS} secondly. In the case of shutting off supply voltage, please shut off V_{BS} firstly and shut off Vcc secondly. When applying Vcc and V_{BS}, power supply should be applied slowly. If it rises rapidly, output signal (HO or LO) may be malfunction.

Consideration

As for this product, the terminal of low voltage part and high-voltage part is very clear (The Fifth: Vcc, The Sixth: Vs). Therefore, pin insulation space distance should be taken enough.

PACKAGE OUTLINE



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	–	1.5	–
A_1	0.05	–	–
A	–	–	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	–	10°
H_E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	–	–	0.1
L	0.2	0.4	0.6