



UR5517

LINEAR INTEGRATED CIRCUIT

3A DDR BUS TERMINATION REGULATOR

DESCRIPTION

The **UR5517** is a linear regulator which provides up to 3 Amp bi-directional sourcing and sinking capability for DDR1/2/3 SDRAM bus terminator applications. It only requires 20uF of ceramic output capacitance by a integrated operational amplifier which provides fast load transient response.

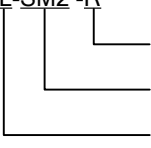
The **UR5517** also includes two control pins, S3 & S5. If S3 were set in low level, V_{TT} will be turned off and left Hi-Z(sleep-state mode).If setting S5 were set in low level, both V_{TT} and V_{TTREF} will be turned off and discharged to ground(soft-off mode).

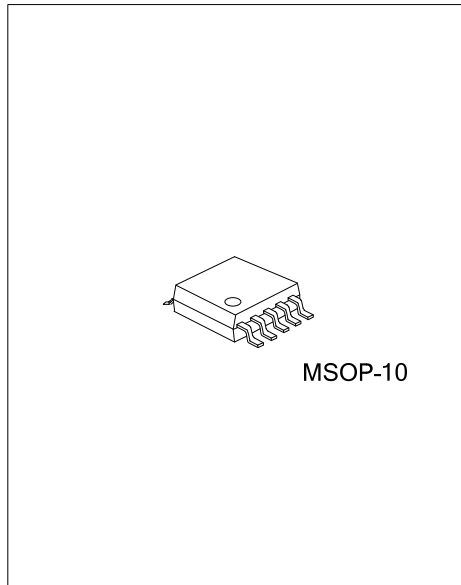
FEATURES

- * Input Voltage Range:3~5.5V
- * V_{LDOIN} Voltage Range:1.2V~3.6V
- * DDR1/2/3 Termination Voltage Applications
- * Sourcing and Sinking Current up to 3A
- * $\pm 20mV$ Accuracy for V_{TT} and V_{TTREF}
- * 10mA Buffered Reference(V_{TTREF})
- * Supports High-Z in S3(STR) and Soft-off in S5(Shutdown)
- * Integrated Divider Tracks 1/2 V_{DDQSNS} for Both V_{TT} & V_{TTREF}
- * Built-In Soft-Start
- * Current Limiting Protection
- * Thermal Shutdown Protection

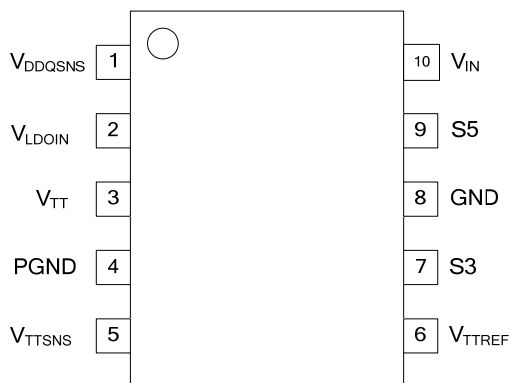
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UR5517L-SM2-R	UR5517G-SM2-R	MSOP-10	Tape Reel
UR5517L-SM2-T	UR5517G-SM2-T	MSOP-10	Tube

<p>UR5517L-SM2-R</p>  <p>(1)Packing Type (2)Package Type (3)Lead Free</p>	<p>(1) R: Tape Reel, T: Tube (2) SM2: MSOP-10 (3) G: Halogen Free, L: Lead Free</p>
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PIN CONFIGURATIONS

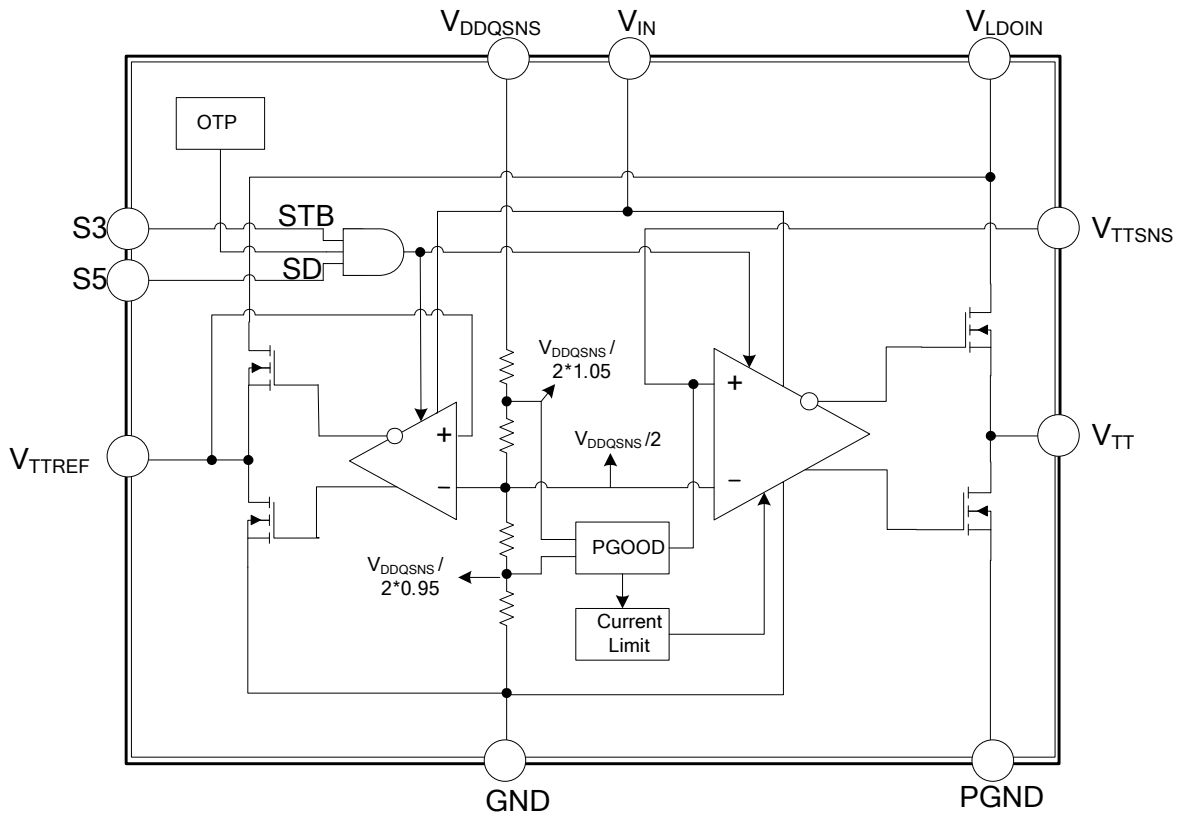


■ PIN DESCRIPTION(Note)

PIN NAME	PIN TYPE	PIN DESCRIPTION
V _{DDQSNS}	I	V _{DDQ} sense input
V _{LDOIN}	I	Power supply for the V _{TT} & V _{TTREF} output stage
V _{TT}	O	Output voltage for connection to termination resistors, equal to V _{DDQSNS} /2
PGND	O	Power ground output for the V _{TT} output
V _{TTSENS}	I	Voltage sense input for the V _{TT} . Connect to plus terminal of the output capacitor
V _{TTREF}	O	Buffered output that is a reference output, equal to V _{DDQSNS} /2
S3	I	Active low suspend to RAM mode control pin, V _{TT} is turned off and left Hi-Z
GND	I	Ground
S5	I	Active low shutdown control pin, both V _{TT} &V _{TTREF} are turned off and discharged to ground
V _{IN}	I	Analog input pin

Note: Recommend connecting the Thermal Pad to the GND for the excellent power dissipation.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage($V_{IN}, V_{LDOIN}, V_{DDQSNS}, S3, S5$)		-0.3~6	V
Power Ground Output for the V_{TT} Output	P_{GND}	-0.3~0.3	V
Output Voltage(V_{TT}, V_{TTREF})	V_{TT}, V_{TTREF}	-0.3~ $V_{LDOIN}+0.3$	V
Junction Temperature	T_J	160	°C
Storage Temperature	T_{STG}	-55 ~ +160	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Note1, 2)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	3		5.5	V
STR and Shutdown Voltage	S3, S5	-0.1		5.5	V
V_{DDQ} Sense Input	V_{DDQSNS}	1.3		3.6	V
Power Supply for the V_{TT} and V_{TTREF} Output Stage	V_{LDOIN}	1.2		3.6	V
Power Ground Output for the V_{TT} Output	P_{GND}	-0.1		0.1	V
Operating Temperature	T_A	-40		85	°C

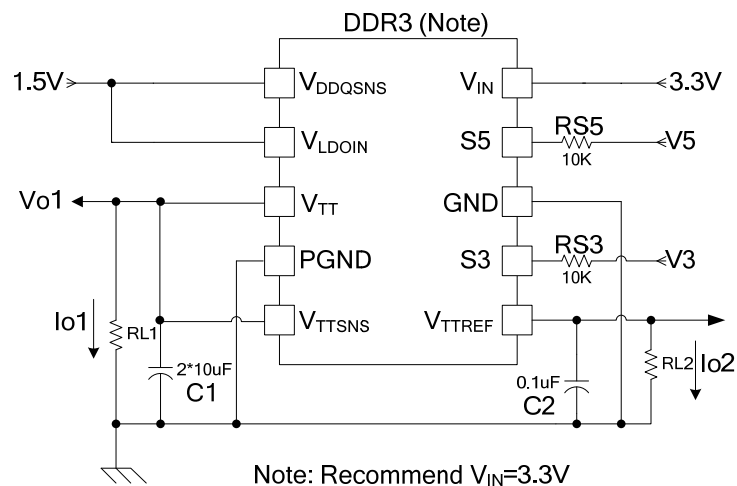
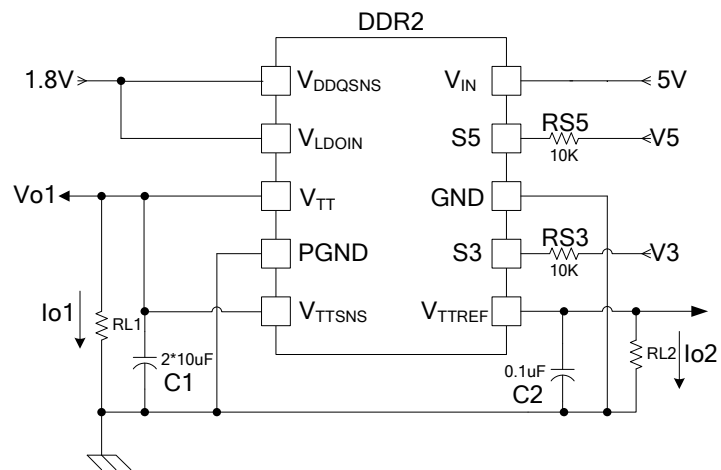
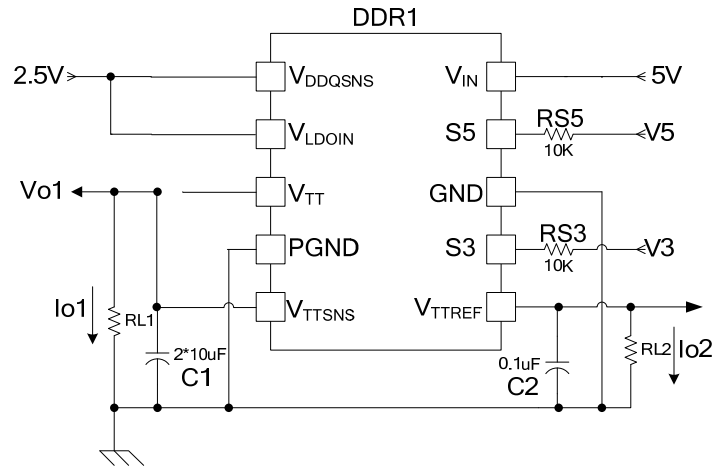
Note: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.
2. Please always keep $V_{LDOIN}, V_{TTSNS}, V_{DDQSNS}, S3, S5$ lower than V_{IN} on operation.

■ ELECTRICAL CHARACTERISTICS

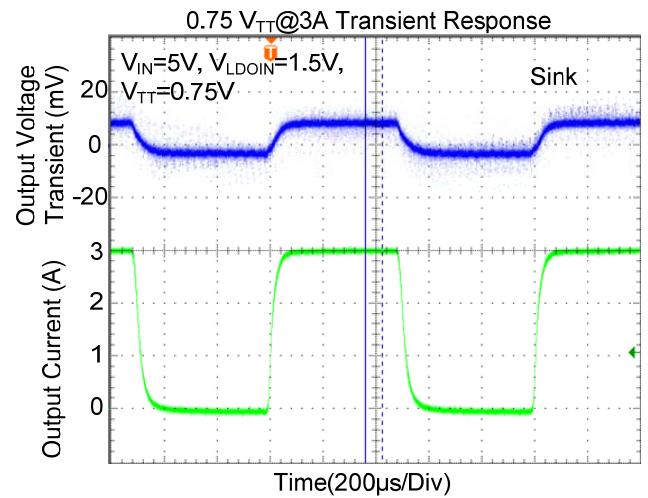
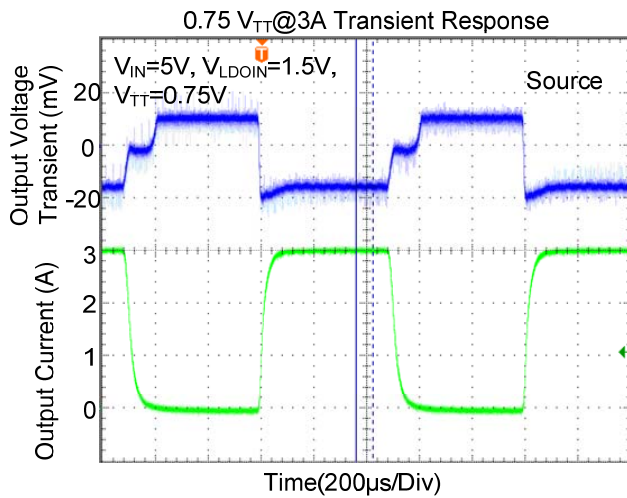
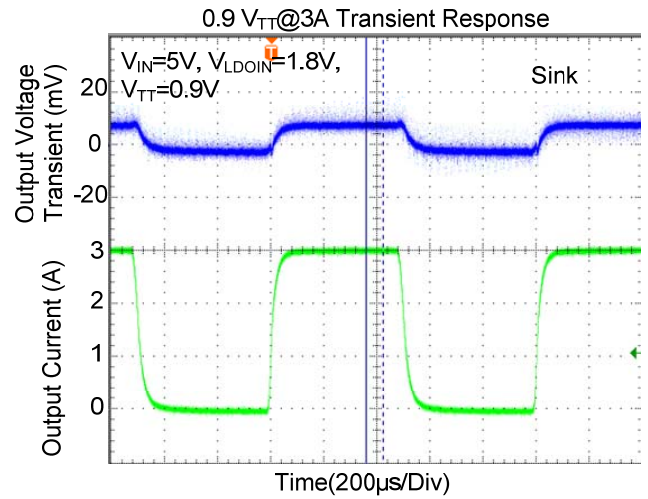
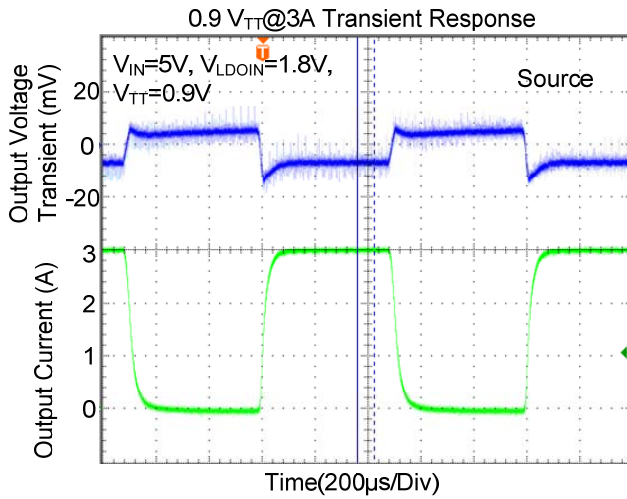
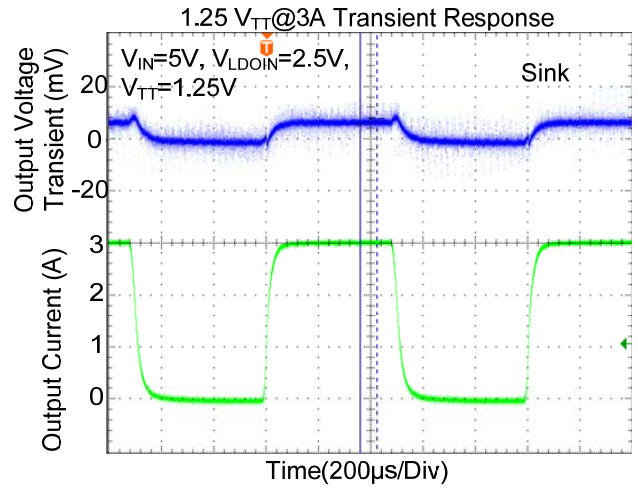
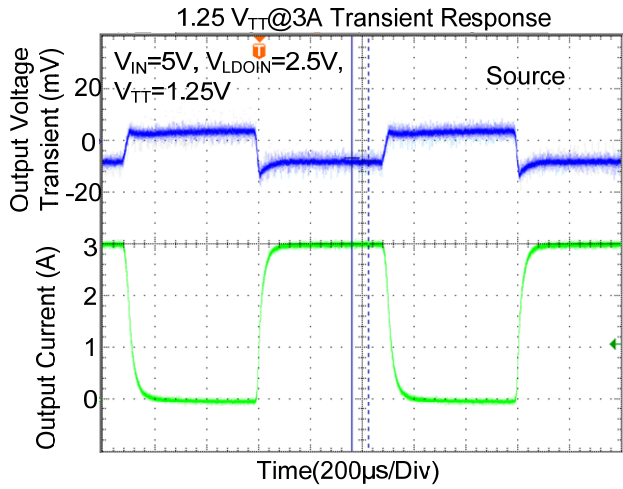
($V_{IN}=5V, V_{LDOIN}=V_{DDQSNS}=2.5V, T_A=25^\circ C$. Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current of V_{IN}	I_{VIN}	S5=Hi, S3=Hi, no load(Normal)	0.5	0.8	2	mA
	I_{VINSTB}	S5=Hi, S3=Lo, no load(Standby)		110	200	uA
	I_{VINSND}	S5=Lo, S3=Lo, no load(Shutdown)			1	uA
Current of V_{LDOIN}	I_{VLDOIN}	S5=Hi, S3=Hi, no load(Normal)		0.03	2	mA
	$I_{VLDOINSTB}$	S5=Hi, S3=Lo, no load(Standby)		0.1	10	uA
	$I_{VLDOINSDN}$	S5=Lo, S3=Lo, no load(Shutdown)		0.1	1	uA
Input Impedance of V_{DDQSNS}	$Z_{VDDQSNS}$	S5=Hi, S3=Hi		200		kΩ
Input Current of V_{TTSNS}	I_{VTTSNS}	S5=Hi, S3=Hi		0.3	1	uA
Output Voltage of V_{TT}	V_{TT}	DDR1($V_{LDOIN}=V_{DDQSNS}=2.5V$)		1.25		V
		DDR2($V_{LDOIN}=V_{DDQSNS}=1.8V$)		0.9		
		DDR3($V_{LDOIN}=V_{DDQSNS}=1.5V$)		0.75		
Load Regulation of V_{TT} ($V_{TTREF}-V_{TT}$)	$V_{OS}V_{TT}$	$I_{VTT}=0$	-20		20	mV
		$ I_{VTT} < 1.5A$	-30		30	
		$ I_{VTT} < 3A$	-40		40	
Source Current Limit of V_{TT}	$I_{VTTCLSRC}$	$V_{TT}=V_{DDQSNS}/2*0.95, PGOOD=HI$	3	4		A
		$V_{TT}=0$	1.5	2		
Sink Current Limit of V_{TT}	$I_{VTTCLSNK}$	$V_{TT}=V_{DDQSNS}/2*1.05, PGOOD=HI$	3	4		A
		$V_{TT}=V_{DDQSNS}$	1.5	2		
Leakage Current of V_{TT}	I_{VTTLK}	S5=Hi, S3=Lo		0.01		uA
Discharge Current of V_{TT}	I_{VTTDIS}	S5=Lo, $V_{DDQSNS}=0V, V_{TT}=0.5V$	10	20		mA
Output Voltage of V_{TTREF}	V_{TTREF}	DDR1($V_{LDOIN}=V_{DDQSNS}=2.5V$)		1.25		V
		DDR2($V_{LDOIN}=V_{DDQSNS}=1.8V$)		0.9		
		DDR3($V_{LDOIN}=V_{DDQSNS}=1.5V$)		0.75		
Load Regulation of V_{TTREF}	ΔV_{TTREF}	$ I_{VTTREF} < 10mA$	-20		20	mV
High Level Input Voltage	V_{IH}	S3 & S5 pin	1.6			V
Low Level Input Voltage	V_{IL}	S3 & S5 pin			1	V
Logic Input Leakage Current	I_{ILEAK}	S3 & S5 pin	-1		1	uA
Thermal Shutdown Temperature	T_{SD}	$V_{IN}=3V\sim 5.5V$		160		°C
Thermal Shutdown Hysteresis	ΔT_{SD}	$V_{IN}=3V\sim 5.5V$		20		

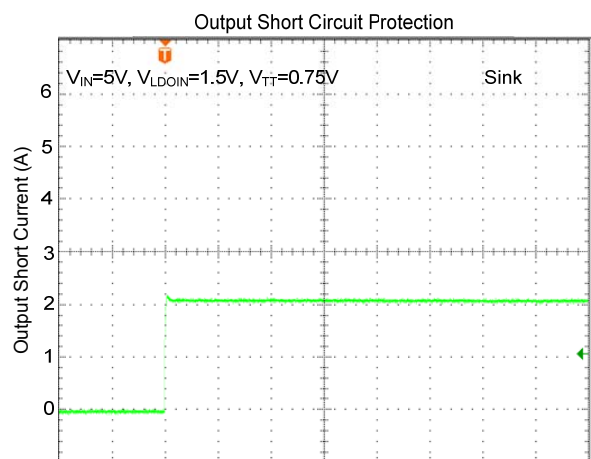
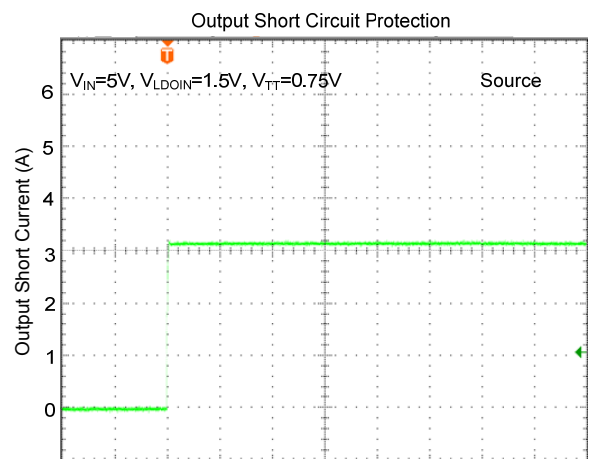
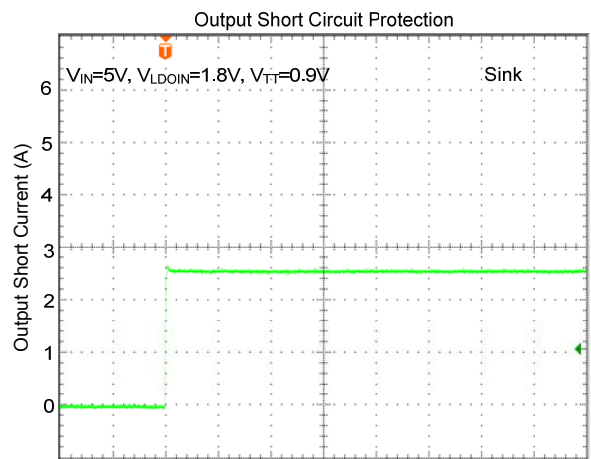
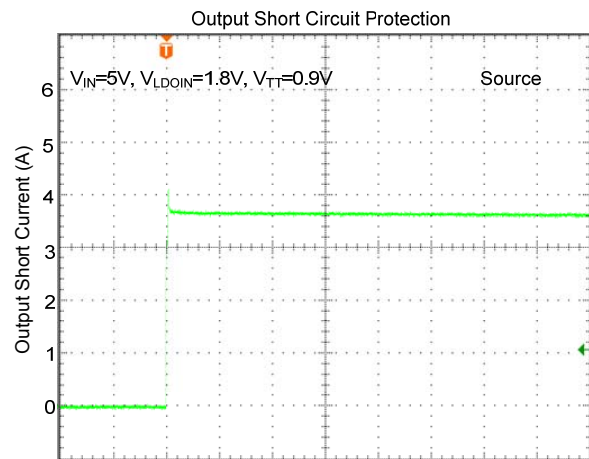
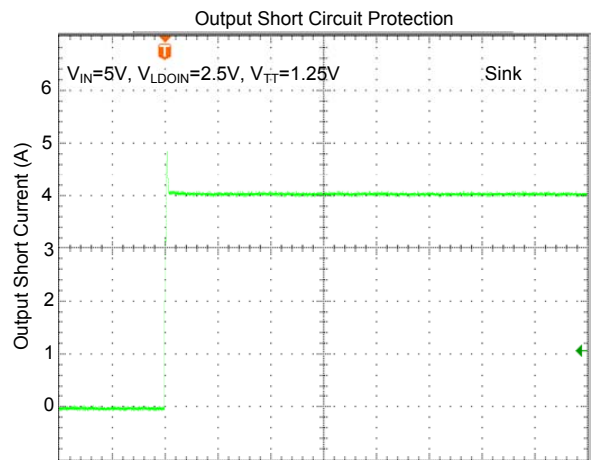
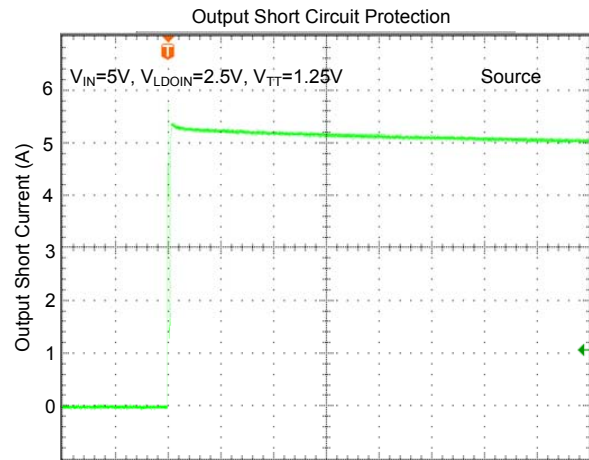
■ TYPICAL APPLICATIONS CIRCUIT



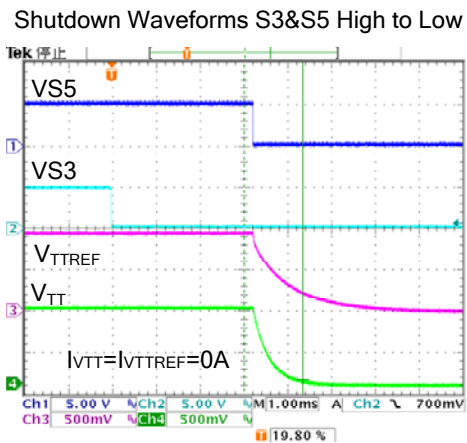
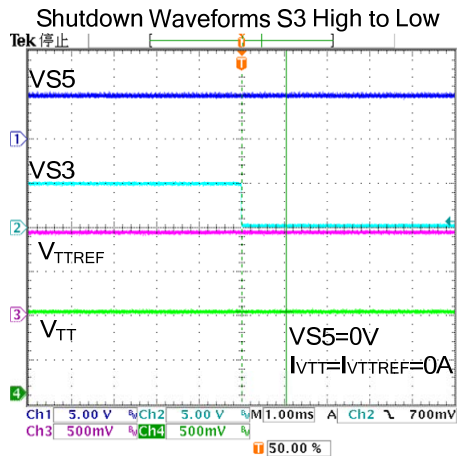
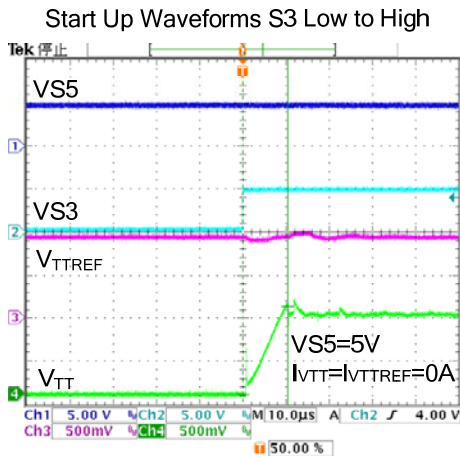
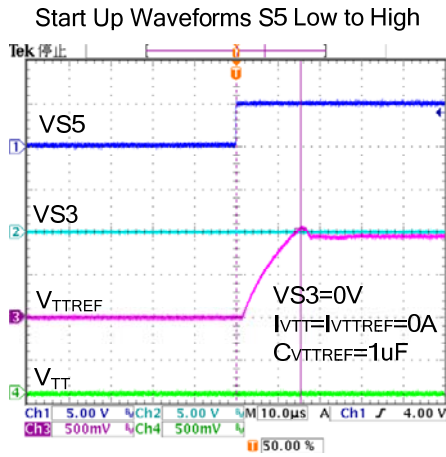
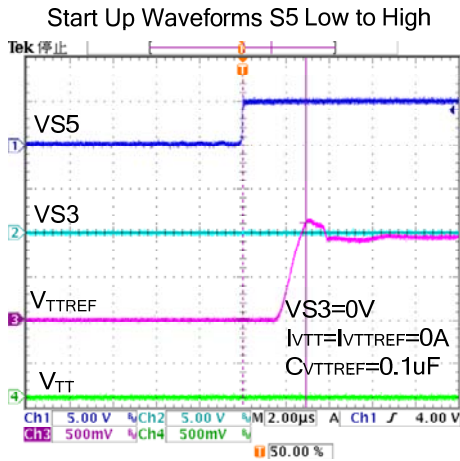
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



■ TYPICAL CHARACTERISTICS(Cont.)



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