M37902FCMHP, M37902FGMHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

These are single-chip microcomputers designed with high-performance CMOS silicon gate technology, including the internal flash memory. These microcomputers support the 7900 Series instruction set, which are enhanced and expanded instruction set and are upper-compatible with the 7700/7751 Series instruction set.

The CPU of these microcomputers is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Also, the bus interface unit of these microcomputers enhances the memory access efficiency to execute instructions fast. Therefore, these microcomputers are suitable for office, business, and industrial equipment controller that require high-speed processing of large data.

For the internal flash memory, single-power-supply programming and erasure, using a PROM programmer or the control by the central processing unit (CPU), is supported. Also, each of these microcomputers has the memory area dedicated for storing a certain software which controls programming and erasure (reprogramming control software). Therefore, on these microcomputers, the program can easily be changed even after they are mounted on the board.

APPLICATION

Control devices for personal computer peripheral equipment such as CD-ROM drives, DVD-ROM drives, hard disk drives, high density FDD, printers

DISTINCTIVE FEATURES

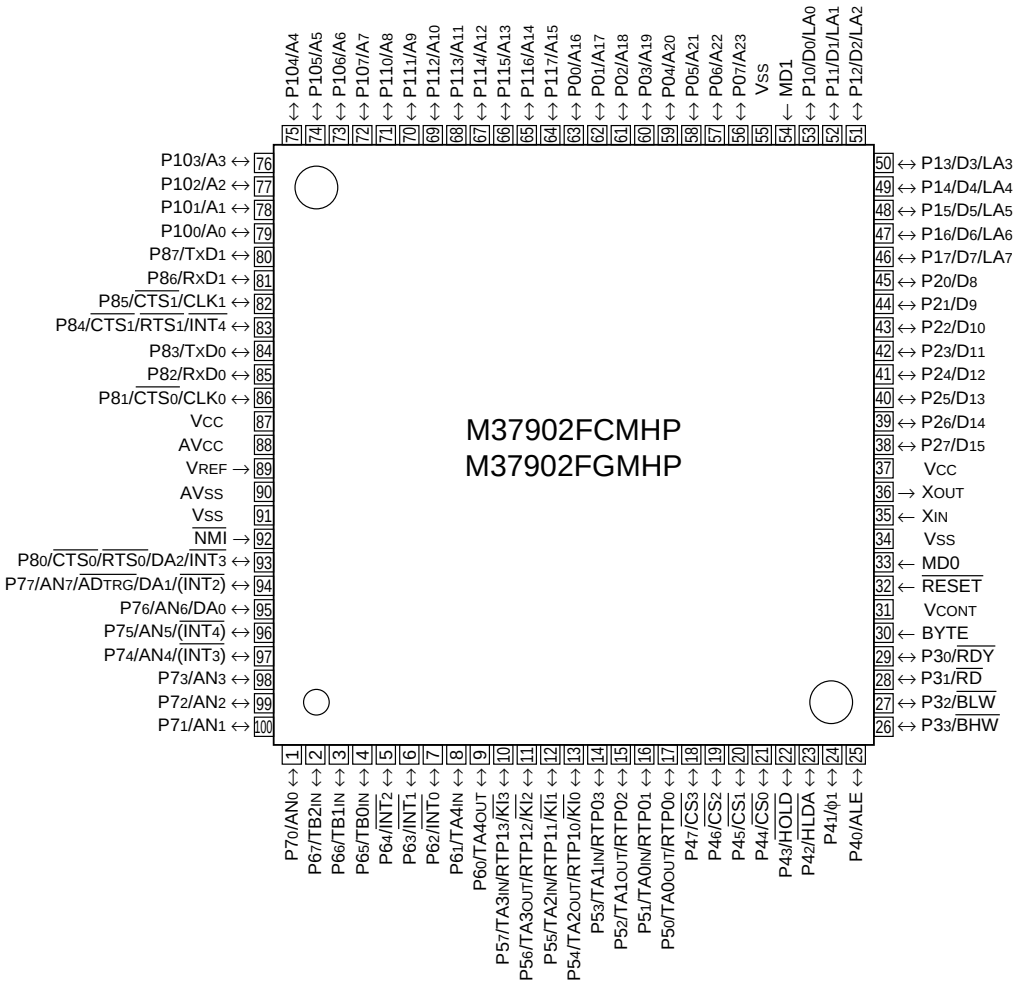
<Microcomputer mode>

- Number of basic machine instructions 203
- Memory
  [M37902FCMHP]
  Flash memory (User ROM area) ..... 120 Kbytes
  RAM ..... 4096 bytes
  [M37902FGMHP]
  Flash memory (User ROM area) ..... 248 Kbytes
  RAM ..... 6144 bytes
  [All of the above computers]
  Flash memory (Boot ROM area) ..... 16 Kbytes
- Instruction execution time
  The fastest instruction at 20 MHz frequency ..... 50 ns
- Single power supply ..... 3.3 V ± 0.3 V
- Interrupts ..... 6 external sources, 16 internal sources, 7 levels
- Multi-functional 16-bit timer ..... 5 + 3
- Serial I/O (UART or Clock synchronous) 2
- 10-bit A-D converter ..... 8-channel inputs
- 8-bit D-A converter ..... 3-channel outputs
- Real-time output
  .... 4 bits × 2 channels, or 6 bits × 1 channel + 2 bits × 1 channel
- 12-bit watchdog timer
- Programmable input/output (ports P0–P8, P10, P11) 84

<Flash memory mode>

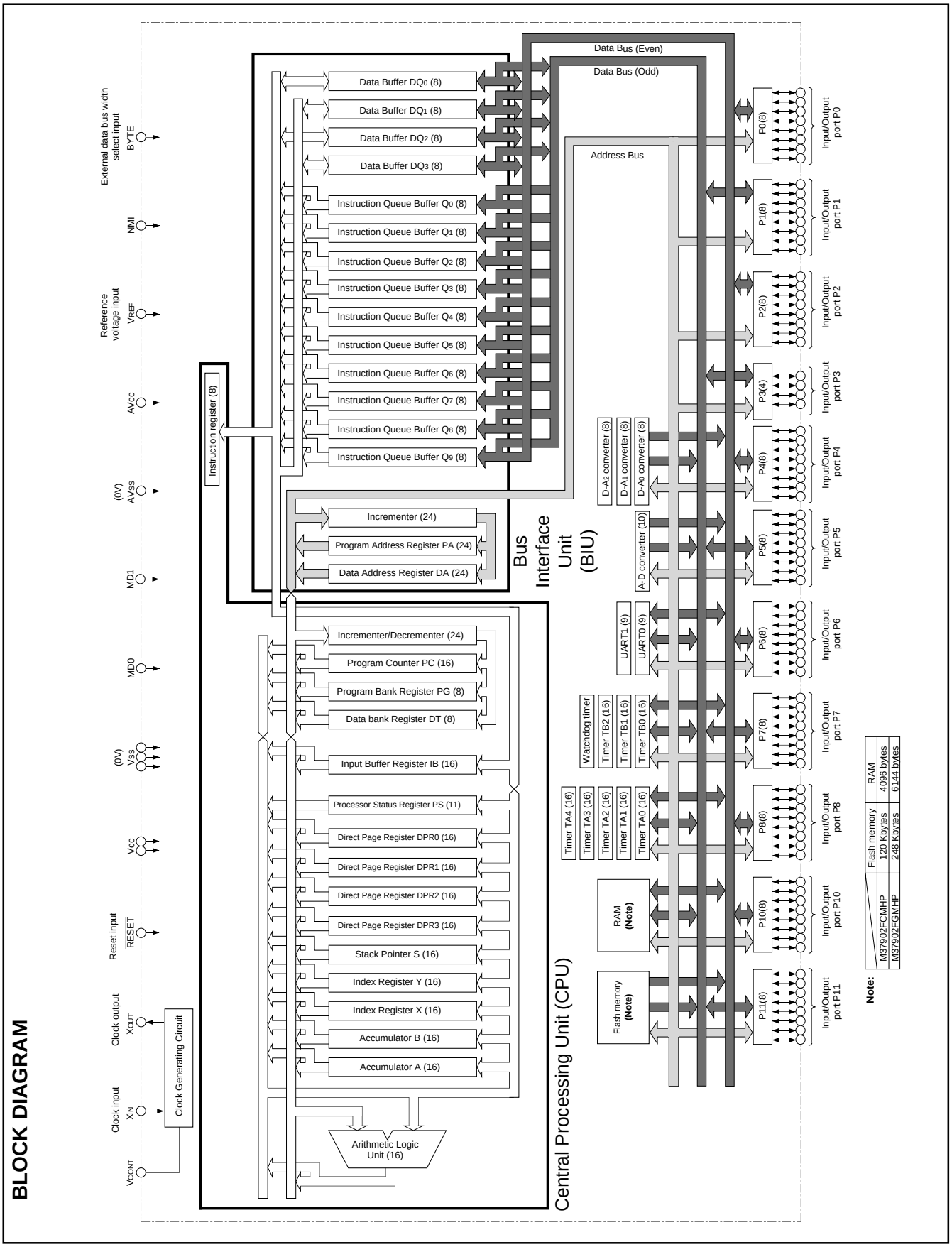
- Power supply voltage ..... 3.3 V ± 0.3 V
- Programming/Erase voltage ..... 3.3 V ± 0.3 V
- Programming method ..... Programming in a unit of 256 bytes
- Erase method ..... Block erase or Total erase
  (Data protection per block is enabled.)
- Programming/Erase control by software command
- Maximum number of reprograms 100

M37902FxMHP PIN CONFIGURATION (TOP VIEW)



Outline 100P6Q-A

BLOCK DIAGRAM



Note:

	Flash memory	RAM
M37902FCMHP	120 Kbytes	4096 bytes
M37902FGMHP	248 Kbytes	6144 bytes

FUNCTIONS (Microcomputer mode)

Parameter		Functions
Number of basic machine instructions		203
Instruction execution time		50 ns (the fastest instruction at f(f_{sys}) = 20 MHz)
External clock input frequency f(X_{IN})		20 MHz (Max.)
System clock frequency f_{sys}		20 MHz (Max.)
Memory size	Flash memory (User ROM area)	**(Note)**
	RAM	**(Note)**
	Flash memory (Boot ROM area)	16 Kbytes
Programmable input/output ports	P0–P2, P4–P8, P10, P11	8-bit × 10
	P3	4-bit × 1
Multi-functional timers	TA0–TA4	16-bit × 5
	TB0–TB2	16-bit × 3
Serial I/O	UART0 and UART1	(UART or Clock synchronous serial I/O) × 2
A-D converter		10-bit successive approximation method × 1 (8 channels)
D-A converter		8-bit × 3
Watchdog timer		12-bit × 1
Chip-select wait control		Chip select area × 4 ($\overline{CS_0}$–$\overline{CS_3}$). A bus cycle type and bus width can be set for each chip select area.
Real-time output		4 bits × 2 channels; or 6 bits × 1 channel + 2 bits × 1 channel
Interrupts	Maskable interrups	5 external types, 13 internal types. Each interrupt can be set to a priority level within the range of 0–7 by software.
	Non-maskable interrups	1 external type, 3 internal types.
Clock generating circuit		Built-in (externally connected to a ceramic resonator or quartz crystal resonator).
PLL frequency multiplier		The following multiplication methods are available: double, triple, and quadruple.
Power supply voltage		3.3 V±0.3 V
Power dissipation		39.6 mW (at f(f_{sys}) = 20 MHz, Typ., PLL frequency multiplier stopped)
Ports' input/output characteristics	Input/Output withstand voltage	3.3 V
	Output current	5 mA
Memory expansion		Up to 16 Mbytes. Note that bank FF_{16} is a reserved area.
Operating ambient temperature range		–20 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		100-pin plastic molded QFP

Note:

Flash memory (User ROM area)	M37902FCMHP	120 Kbytes
	M37902FGMHP	248 Kbytes
RAM	M37902FCMHP	4096 bytes
	M37902FGMHP	6144 bytes

FUNCTIONS (Flash memory mode)

Parameter		Functions
Power supply voltage		3.3 V±0.3 V
Programming/Erase voltage		3.3 V±0.3 V
Flash memory mode		3 modes: parallel I/O, serial I/O, and CPU reprogramming modes
Block division for erasure	User ROM area	**(Note 1)**
	Boot ROM area	1 block (16 Kbytes × 1) **(Note 2)**
Programming method		Programmed per page (in a unit of 256 Kbytes)
	Flash memory parallel I/O mode	User ROM area + Boot ROM area
	Flash memory serial I/O mode	User ROM area
	Flash memory CPU reprogramming mode	User ROM area
Erase method		Total erase/Block erase
	Flash memory parallel I/O mode	User ROM area + Boot ROM area
	Flash memory serial I/O mode	User ROM area
	Flash memory CPU reprogramming mode	User ROM area
Programming/Erase control		Programming/Erase control by software commands
Data protection method		Protected per block, by using a lock bit.
Number of commands		8 commands
Maximum number of reprograms		100

Notes 1:

User ROM area	M37902FCMHP	5 blocks (8 Kbytes × 3, 32 Kbytes × 1, 64 Kbytes × 1), total 120 Kbytes
	M37902FGMHP	7 blocks (8 Kbytes × 3, 32 Kbytes × 1, 64 Kbytes × 3), total 248 Kbytes

2: On shipment, our reprogramming control firmware for the flash memory serial I/O mode has been stored into the boot ROM area. Note that the boot ROM area can be erased/programmed only in the flash memory parallel I/O mode.

PIN DESCRIPTION (MICROCOMPUTER MODE)

Pin	Name	Input/ Output	Functions
Vcc, Vss	Power supply input	—	Apply 3.3 V±0.3 V to Vcc, and 0 V to Vss.
MD0	MD0	Input	This pin controls the processor mode. Connect this pin to VSS for the single-chip mode or memory expansion mode, and Vcc for the microprocessor mode.
MD1	MD1	Input	Connect this pin to Vss.
$\overline{\text{RESET}}$	Reset input	Input	The microcomputer is reset when “L” level is applied to this pin.
XIN	Clock input	Input	These are input and output pins of the internal clock generating circuit. Connect a ceramic or quartz- crystal resonator between the XIN and XOUT pins. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open.
XOUT	Clock output	Output	
BYTE	External data bus width select input	Input	This pin determines whether the external data bus has an 8-bit width or 16-bit width for the memory expansion mode or microprocessor mode. The width is 16 bits when “L” signal is input, and 8 bits when “H” signal is input. When BYTE = Vss level, by the register setting, the external data bus for each of areas $\overline{\text{CS1}}$ to $\overline{\text{CS3}}$ can have a width of 8 bits.
VCONT	Filter circuit connection	—	When using the PLL frequency multiplier, connect this pin to the filter circuit. When not using, this pin should be left open.
AVcc, AVss	Analog power supply input	—	Power supply input pins for the A-D converter and the D-A converter. Connect AVcc to Vcc, and AVss to Vss externally.
VREF	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter and the D-A converter.
P00–P07	I/O port P0	I/O	■ In single-chip mode Port P0 is an 8-bit I/O port. This port has an I/O direction register, and each pin can be programmed for input or output. These pins enter the input mode at reset. ■ In memory expansion and microprocessor modes Address (A16–A23) is output. These pins also function as I/O port pins according to the register setting.
P10–P17	I/O port P1	I/O	■ In single-chip mode These pins have the same functions as port P0. ■ In memory expansion and microprocessor modes The low-order 8 bits of data (D0–D7) are input/output. When the external data bus has an 8-bit width, address (LA0–LA7) output and data (D0–D7) input/output can be performed with the time-sharing method, according to the register setting.
P20–P27	I/O port P2	I/O	■ In single-chip mode or When 8-bit external data bus is used in memory expansion mode and microprocessor mode These pins have the same functions as port P0. ■ When the 16-bit external data bus is used in memory expansion or microprocessor mode The high-order 8 bits of data (D8–D15) are input or output.
P30–P33	I/O port P3	I/O	■ In single-chip mode These pins have the same functions as port P0. ■ In memory expansion mode P30 functions as an I/O port pin; and P31, P32, and P33 function as the output pins of $\overline{\text{RD}}$, $\overline{\text{BLW}}$, $\overline{\text{BHW}}$, respectively. P30 also functions as an output pin of $\overline{\text{RDY}}$ according to the register setting. When the external data bus has a width of 8 bits, the $\overline{\text{BHW}}$ pin functions as an I/O port pin (P33). ■ In microprocessor mode P30 functions as an input pin of $\overline{\text{RDY}}$; and P31,P32, P33 function as the output pins of $\overline{\text{RD}}$, $\overline{\text{BLW}}$, $\overline{\text{BHW}}$, respectively. P30 also functions as an I/O port pin according to the register setting. When the external data bus has a width of 8 bits, the $\overline{\text{BHW}}$ pin functions as an I/O port pin (P33).
P40–P47	I/O port P4	I/O	■ In single-chip mode These pins have the same functions as port P0. ■ In memory expansion mode P40–P47 function as I/O port pins. According to the register setting, these pins function as output pins or input pins of ALE, ϕ1, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$, $\overline{\text{CS0}}$–$\overline{\text{CS3}}$, respectively. ■ In microprocessor mode P40–P44 function as output or input pins of ALE, ϕ1, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$, $\overline{\text{CS0}}$, and P45–P47 as I/O port pins, respectively. According to the register setting, P40–P43 also function as I/O port pins, and P45–P47 as output pins of $\overline{\text{CS1}}$–$\overline{\text{CS3}}$.

Pin	Name	Input/ Output	Functions
$P5_0$–$P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0–A3, output pins for the real-time output, and input pins for the key-input interrupt.
$P6_0$–$P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt inputs $\overline{INT_0}$–$\overline{INT_2}$, and input pins for timers B0–B2.
$P7_0$–$P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as input pins for the A-D converter, output pins for the D-A converter, and input pins for $\overline{INT_2}$, $\overline{INT_3}$, and $\overline{INT_4}$.
$P8_0$–$P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART0, UART1, output pins for D-A converter, and input pins for $\overline{INT_3}$ and $\overline{INT_4}$.
$P10_0$–$P10_7$	I/O port P10	I/O	■ In single-chip mode These pins have the same functions as port P0. ■ In memory expansion and microprocessor modes Address (A_0–A_7) is output.
$P11_0$–$P11_7$	I/O port P11	I/O	■ In single-chip mode These pins have the same functions as port P0. ■ In memory expansion and microprocessor modes Address (A_8–A_{15}) is output. Also, these pins function as I/O port pins according to the register setting.
$\overline{NMI}$	Non-maskable interrupt	Input	This pin is for a non-maskable interrupt.

PIN DESCRIPTION (FLASH MEMORY SERIAL I/O MODE)

Pin	Name	Input /Output	Functions
VCC, VSS	Power supply input	—	Apply 3.3 V ± 0.3 V to Vcc, and 0 V to Vss.
MD0	MD0	Input	Connect this pin to Vss.
MD1	MD1	Input	Connect this pin to Vss via a resistor of 10 kΩ to 100 kΩ.
$\overline{\text{RESET}}$	Reset input	Input	The reset input pin.
XIN	Clock input	Input	Connect a ceramic resonator between the XIN and XOUT pins, or input an external clock from the XIN pin with the XOUT pin left open.
XOUT	Clock output	Output	
BYTE	BYTE	Input	Connect this pin to Vcc or Vss. (This is not used in the flash memory serial I/O mode.)
VCONT	Filter circuit connection	—	Connect this pin to the filter circuit, or leave this pin open. (This is not used in the flash memory serial I/O mode.)
AVcc, AVss	Analog supply input	—	Connect AVcc to Vcc, and AVss to Vss.
VREF	Reference voltage input	Input	Input an arbitrary level within the range of VSS–VCC.(This is not used in the flash memory serial I/O mode.)
P00–P07	Input port P0	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P10–P17	Input port P1	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P20–P27	Input port P2	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P30–P33	Input port P3	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P40, P44– P47	Input port P4	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P41	SCLK input	Input	This is an input pin for a serial clock.
P42	SDA I/O	I/O	This is an I/O pin for serial data. Connect this pin to VCC via a resistor (about 1 kΩ).
P43	BUSY output	Output	This is an output pin for the BUSY signal.
P50–P57	Input port P5	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P60–P67	Input port P6	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P70–P77	Input port P7	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P80–P87	Input port P8	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P100–P107	Input port P10	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
P110–P117	Input port P11	Input	Input “H” or “L”, or leave them open. (This is not used in the flash memory serial I/O mode.)
$\overline{\text{NMI}}$	Non-maskable interrupt	Input	Input “H”, or leave this pin open.

BASIC FUNCTION BLOCKS

These microcomputers have the same functions as the M37902FCCHP.
Therefore, refer to the datasheet of the M37902FCCHP.

MEMORY

Figures 1 and 2 show the memory maps. The address space is 16 Mbytes from address 0_{16} to FFFFFF$_{16}$. The address space is divided into 64-Kbyte units called banks. The banks are numbered from 0_{16} to FF$_{16}$. Bank FF$_{16}$ is a reserved area for the development support tool. Therefore, do not use bank FF$_{16}$.
Internal flash memory and internal RAM are assigned as shown in Figures 1 and 2.

Addresses FFC0$_{16}$ to FFFF$_{16}$ contain the RESET and the interrupt vector addresses, and the interrupt vectors are stored there.
For details, refer to the section on interrupts.
Assigned to addresses 0_{16} to FF$_{16}$ are peripheral devices such as I/O ports, A-D converter, D-A converter, UART, timers, interrupt control registers, etc. Figures 7 and 8 show the location of SFRs. For the flash memory in the boot ROM area, refer to the section on the flash memory mode.

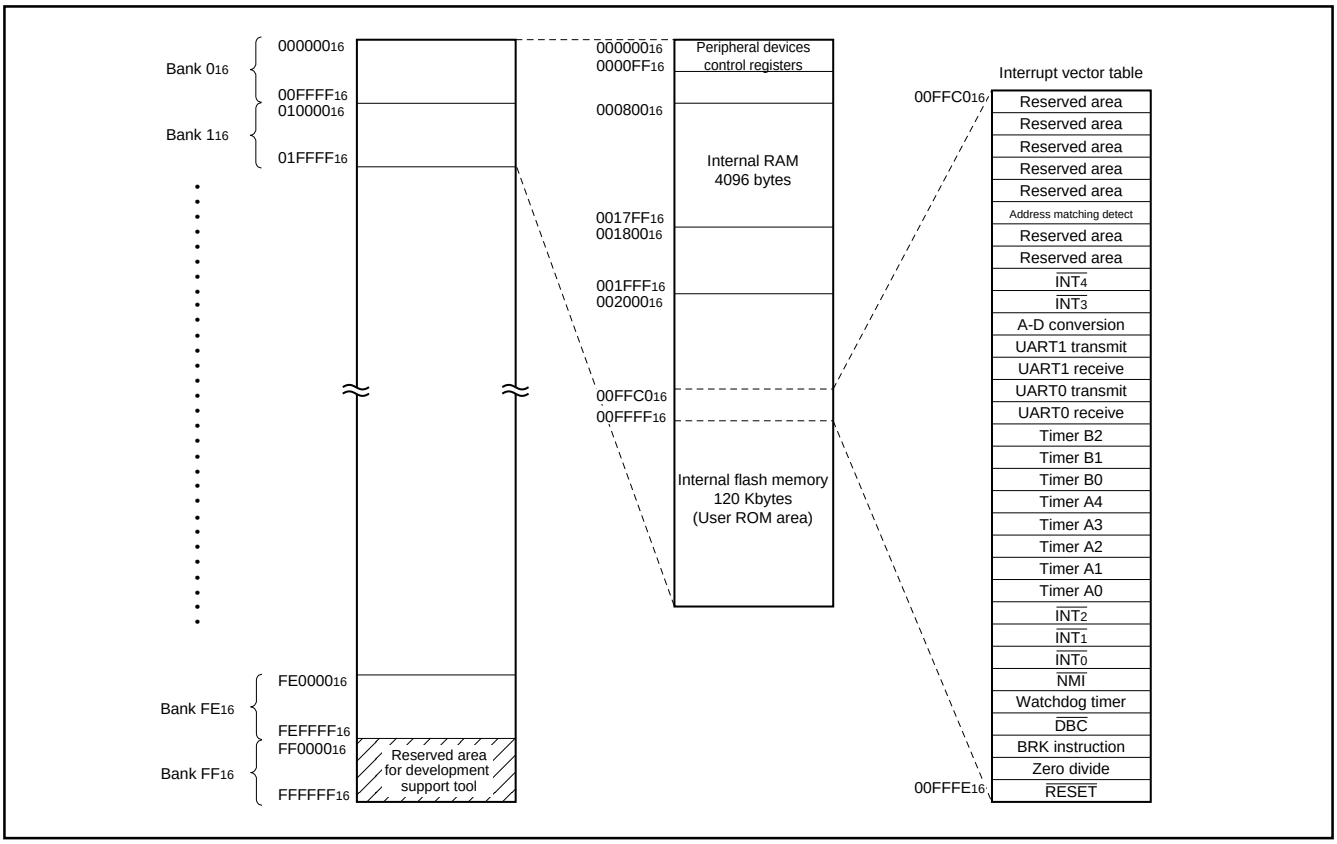


Fig. 1 Memory map of M37902FCMHP (Single-chip mode)

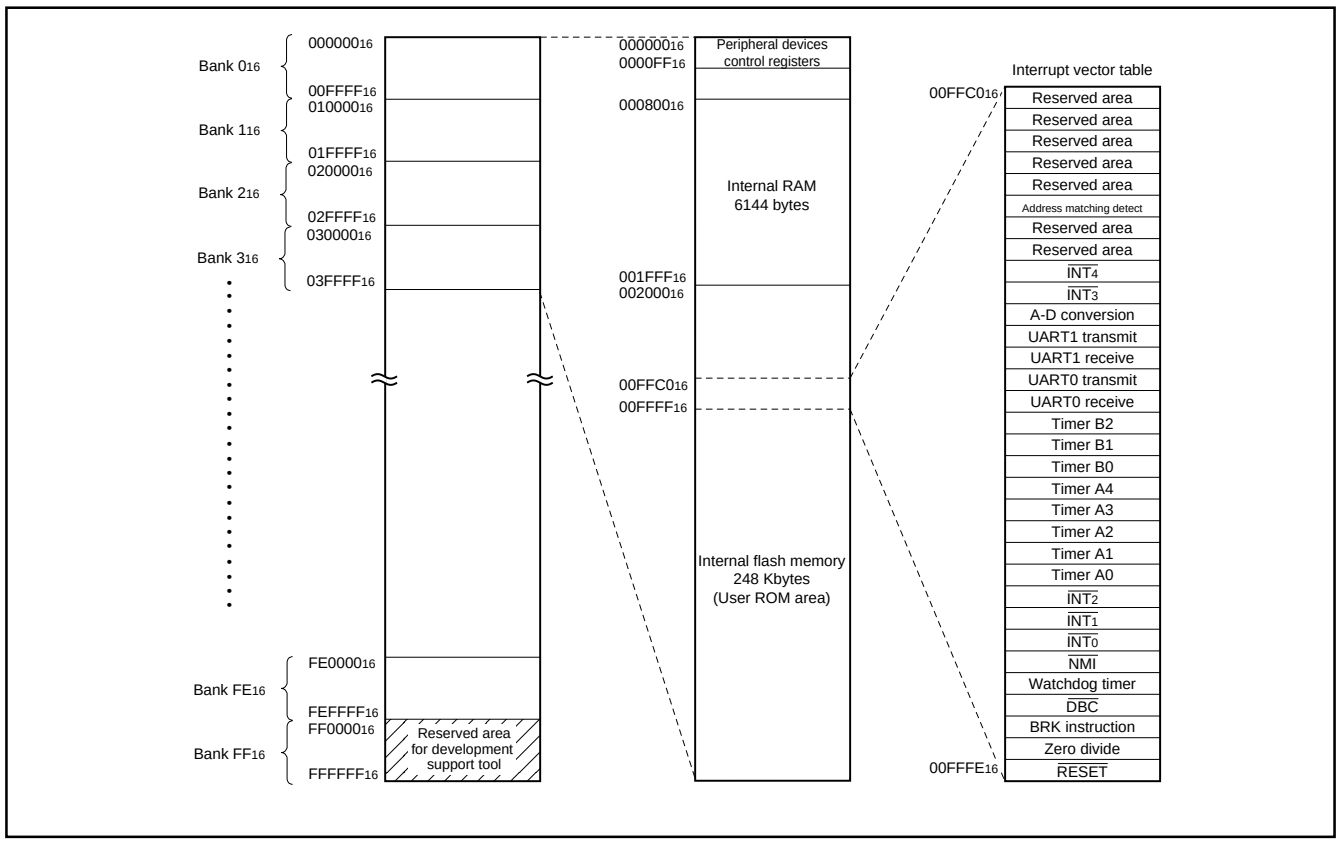


Fig. 2 Memory map of M37902FGMHP (Single-chip mode)

Address (Hexadecimal notation)	
000000₁₆	Reserved area **(Note)**
000001₁₆	Reserved area **(Note)**
000002₁₆	Port P0 register
000003₁₆	Port P1 register
000004₁₆	Port P0 direction register
000005₁₆	Port P1 direction register
000006₁₆	Port P2 register
000007₁₆	Port P3 register
000008₁₆	Port P2 direction register
000009₁₆	Port P3 direction register
00000A₁₆	Port P4 register
00000B₁₆	Port P5 register
00000C₁₆	Port P4 direction register
00000D₁₆	Port P5 direction register
00000E₁₆	Port P6 register
00000F₁₆	Port P7 register
000010₁₆	Port P6 direction register
000011₁₆	Port P7 direction register
000012₁₆	Port P8 register
000013₁₆	
000014₁₆	Port P8 direction register
000015₁₆	
000016₁₆	Port P10 register
000017₁₆	Port P11 register
000018₁₆	Port P10 direction register
000019₁₆	Port P11 direction register
00001A₁₆	
00001B₁₆	
00001C₁₆	
00001D₁₆	
00001E₁₆	A-D control register 0
00001F₁₆	A-D control register 1
000020₁₆ 000021₁₆	A-D register 0
000022₁₆ 000023₁₆	A-D register 1
000024₁₆ 000025₁₆	A-D register 2
000026₁₆ 000027₁₆	A-D register 3
000028₁₆ 000029₁₆	A-D register 4
00002A₁₆ 00002B₁₆	A-D register 5
00002C₁₆ 00002D₁₆	A-D register 6
00002E₁₆ 00002F₁₆	A-D register 7
000030₁₆	UART0 transmit/receive mode register
000031₁₆	UART0 baud rate register (BRG0)
000032₁₆ 000033₁₆	UART0 transmit buffer register
000034₁₆	UART0 transmit/receive control register 0
000035₁₆	UART0 transmit/receive control register 1
000036₁₆ 000037₁₆	UART0 receive buffer register
000038₁₆	UART1 transmit/receive mode register
000039₁₆	UART1 baud rate register (BRG1)
00003A₁₆ 00003B₁₆	UART1 transmit buffer register
00003C₁₆	UART1 transmit/receive control register 0
00003D₁₆	UART1 transmit/receive control register 1
00003E₁₆ 00003F₁₆	UART1 receive buffer register

Address (Hexadecimal notation)	
000040₁₆	Count start register
000041₁₆	
000042₁₆	One-shot start register
000043₁₆	
000044₁₆	Up-down register
000045₁₆	Timer A clock division select register
000046₁₆ 000047₁₆	Timer A0 register
000048₁₆ 000049₁₆	Timer A1 register
00004A₁₆ 00004B₁₆	Timer A2 register
00004C₁₆ 00004D₁₆	Timer A3 register
00004E₁₆ 00004F₁₆	Timer A4 register
000050₁₆ 000051₁₆	Timer B0 register
000052₁₆ 000053₁₆	Timer B1 register
000054₁₆ 000055₁₆	Timer B2 register
000056₁₆	Timer A0 mode register
000057₁₆	Timer A1 mode register
000058₁₆	Timer A2 mode register
000059₁₆	Timer A3 mode register
00005A₁₆	Timer A4 mode register
00005B₁₆	Timer B0 mode register
00005C₁₆	Timer B1 mode register
00005D₁₆	Timer B2 mode register
00005E₁₆	Processor mode register 0
00005F₁₆	Processor mode register 1
000060₁₆	Watchdog timer register
000061₁₆	Watchdog timer frequency select register
000062₁₆	Particular function select register 0
000063₁₆	Particular function select register 1
000064₁₆	Particular function select register 2
000065₁₆	Reserved area **(Note)**
000066₁₆	Debug control register 0
000067₁₆	Debug control register 1
000068₁₆ 000069₁₆ 00006A₁₆	Address comparison register 0
00006B₁₆ 00006C₁₆ 00006D₁₆	Address comparison register 1
00006E₁₆	$\overline{INT}_3$ interrupt control register
00006F₁₆	$\overline{INT}_4$ interrupt control register
000070₁₆	A-D conversion interrupt control register
000071₁₆	UART0 transmit interrupt control register
000072₁₆	UART0 receive interrupt control register
000073₁₆	UART1 transmit interrupt control register
000074₁₆	UART1 receive interrupt control register
000075₁₆	Timer A0 interrupt control register
000076₁₆	Timer A1 interrupt control register
000077₁₆	Timer A2 interrupt control register
000078₁₆	Timer A3 interrupt control register
000079₁₆	Timer A4 interrupt control register
00007A₁₆	Timer B0 interrupt control register
00007B₁₆	Timer B1 interrupt control register
00007C₁₆	Timer B2 interrupt control register
00007D₁₆	$\overline{INT}_0$ interrupt control register
00007E₁₆	$\overline{INT}_1$ interrupt control register
00007F₁₆	$\overline{INT}_2$ interrupt control register

Note: Do not write to this address.

Fig. 7 Location of SFRs (1)

Address (Hexadecimal notation)	
000080₁₆	$\overline{CS_0}$ control register L
000081₁₆	$\overline{CS_0}$ control register H
000082₁₆	$\overline{CS_1}$ control register L
000083₁₆	$\overline{CS_1}$ control register H
000084₁₆	$\overline{CS_2}$ control register L
000085₁₆	$\overline{CS_2}$ control register H
000086₁₆	$\overline{CS_3}$ control register L
000087₁₆	$\overline{CS_3}$ control register H
000088₁₆	
000089₁₆	
00008A₁₆	Area $\overline{CS_0}$ start address register
00008B₁₆	
00008C₁₆	Area $\overline{CS_1}$ start address register
00008D₁₆	
00008E₁₆	Area $\overline{CS_2}$ start address register
00008F₁₆	
000090₁₆	Area $\overline{CS_3}$ start address register
000091₁₆	
000092₁₆	Port function control register
000093₁₆	
000094₁₆	External interrupt input control register
000095₁₆	External interrupt input read-out register
000096₁₆	D-A control register
000097₁₆	
000098₁₆	D-A register 0
000099₁₆	D-A register 1
00009A₁₆	D-A register 2
00009B₁₆	
00009C₁₆	Reserved area **(Note)**
00009D₁₆	Reserved area **(Note)**
00009E₁₆	Flash memory control register
00009F₁₆	
0000A0₁₆	Real-time output control register
0000A1₁₆	
0000A2₁₆	Pulse output data register 0
0000A3₁₆	
0000A4₁₆	Pulse output data register 1
0000A5₁₆	
0000A6₁₆	
0000A7₁₆	
0000A8₁₆	
0000A9₁₆	
0000AA₁₆	
0000AB₁₆	
0000AC₁₆	Serial I/O pin control register
0000AD₁₆	
0000AE₁₆	
0000AF₁₆	
0000B0₁₆	
0000B1₁₆	
0000B2₁₆	
0000B3₁₆	
0000B4₁₆	
0000B5₁₆	
0000B6₁₆	
0000B7₁₆	
0000B8₁₆	
0000B9₁₆	
0000BA₁₆	Reserved area **(Note)**
0000BB₁₆	Reserved area **(Note)**
0000BC₁₆	Clock control register
0000BD₁₆	Reserved area **(Note)**
0000BE₁₆	Reserved area **(Note)**
0000BF₁₆	Reserved area **(Note)**

Address (Hexadecimal notation)	
0000C0₁₆	
0000C1₁₆	
0000C2₁₆	
0000C3₁₆	
0000C4₁₆	
0000C5₁₆	
0000C6₁₆	
0000C7₁₆	
0000C8₁₆	
0000C9₁₆	
0000CA₁₆	
0000CB₁₆	
0000CC₁₆	
0000CD₁₆	
0000CE₁₆	
0000CF₁₆	
0000D0₁₆	
0000D1₁₆	
0000D2₁₆	
0000D3₁₆	
0000D4₁₆	
0000D5₁₆	
0000D6₁₆	
0000D7₁₆	
0000D8₁₆	
0000D9₁₆	
0000DA₁₆	
0000DB₁₆	
0000DC₁₆	
0000DD₁₆	
0000DE₁₆	
0000DF₁₆	
0000E0₁₆	
0000E1₁₆	
0000E2₁₆	
0000E3₁₆	
0000E4₁₆	
0000E5₁₆	
0000E6₁₆	
0000E7₁₆	
0000E8₁₆	
0000E9₁₆	
0000EA₁₆	
0000EB₁₆	
0000EC₁₆	
0000ED₁₆	
0000EE₁₆	
0000EF₁₆	
0000F0₁₆	
0000F1₁₆	
0000F2₁₆	
0000F3₁₆	
0000F4₁₆	
0000F5₁₆	
0000F6₁₆	
0000F7₁₆	
0000F8₁₆	
0000F9₁₆	
0000FA₁₆	
0000FB₁₆	
0000FC₁₆	
0000FD₁₆	
0000FE₁₆	
0000FF₁₆	

Note: Do not write to this address.

Fig. 8 Location of SFRs (2)

FLASH MEMORY MODE

These microcomputers contain the DINOR (DIvided bit line NOR)-type flash memory; and single-power-supply reprogramming is available to this. These microcomputers have the following three modes, enabling reading/programming/erasure for the flash memory:

- Flash memory parallel I/O mode and Flash memory serial I/O mode, where the flash memory is handled by using an external programmer.
- CPU reprogramming mode, where the flash memory is handled by the central processing unit (CPU).

For each modes, refer to the datasheet M37902FCCHP.

Figures 9 and 10 shows the block configuration of the internal flash memory of each microcomputer.

These microcomputers have the same functions as the M37902FCCHP except for the following:

(1) Power supply voltage (3.3 V ± 0.3 V)

(2) Electrical characteristics

Therefore, for the flash memory mode except for the above, refer to the datasheet M37902FCCHP.

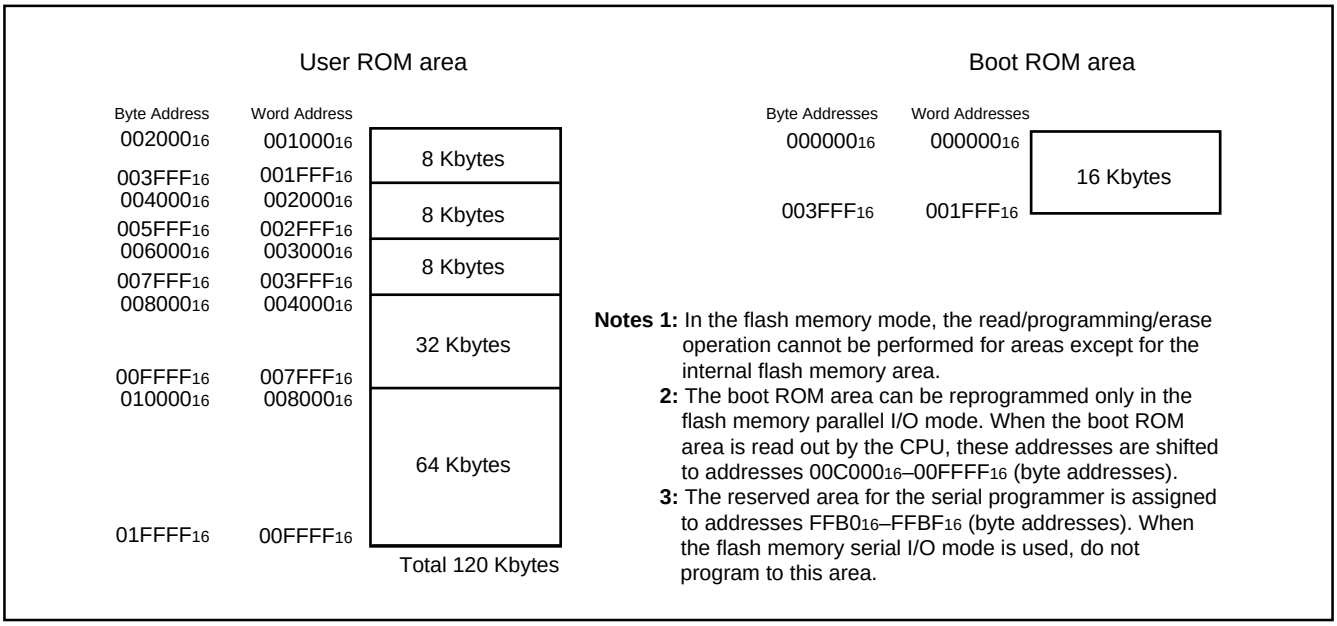


Fig 9. M37902FCMHP: block configuration of internal flash memory

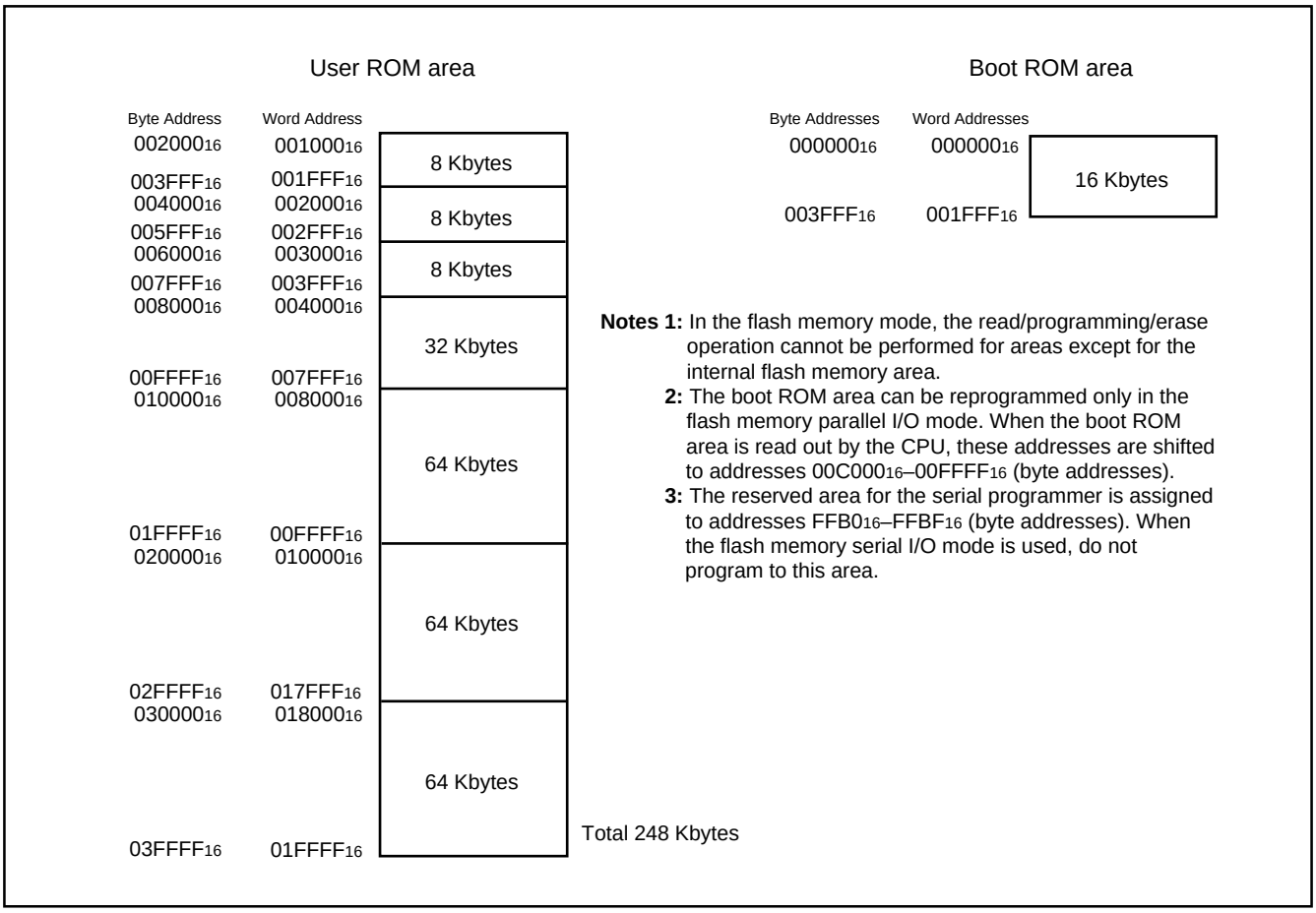


Fig 10. M37902FGMHP: block configuration of internal flash memory

DC Electrical Characteristics (V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 60 °C, f(f_{sys}) = 20 MHz (Note))

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
I_{CC1}	V_{CC} power source current (at read)		19	40	mA
I_{CC2}	V_{CC} power source current (at write)			40	mA
I_{CC3}	V_{CC} power source current (at programming)			48	mA
I_{CC4}	V_{CC} power source current (at erasing)			48	mA

Limits of V_{IH}, V_{IL}, V_{OH}, V_{OL}, I_{IH}, and I_{IL} for each pin are the same as those in the microcomputer mode.
Note: f(f_{sys}) indicates the system clock (fsys) frequency.

AC Electrical Characteristics (V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to 60 °C, f(f_{sys}) = 20 MHz (Note))

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Page programming time		8	120	ms
Block erase time		50	600	ms
Erase all unlocked block time		50 × n	600 × n	ms
Lock bit programming time		8	120	ms

n = Number of blocks to be erased

The limits of parameters other than the above are same as those in the microcomputer mode.
Note: f(f_{sys}) indicates the system clock (fsys) frequency.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Power source voltage	–0.3 to 4.6	V
AV_{CC}	Analog power source voltage	–0.3 to 4.6	V
V_I	Input voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$, V_{REF}, X_{IN}, $\overline{RESET}$, BYTE, MD0, MD1, NMI, V_{CONT}	–0.3 to V_{CC}+0.3	V
V_O	Output voltage P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$, X_{OUT}	–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	400	mW
T_{opr}	Operating ambient temperature	–20 to 85	°C
T_{stg}	Storage temerature	–40 to 150	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 3.3 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage	3.0	3.3	3.6	V
AV_{CC}	Analog power source voltage		V_{CC}		V
V_{SS}	Power source voltage		0		V
AV_{SS}	Analog power source voltage		0		V
V_{IH}	High-level input voltage X_{IN}, $\overline{RESET}$, BYTE, MD0, MD1	0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$	0.7 V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage P0$_0$–P0$_7$ (When the port P0 input level select bit = “0”)	0.7 Vcc		Vcc	V
V_{IH}	High-level input voltage P0$_0$–P0$_7$ (When the port P0 input level select bit = “1”)	0.5 Vcc		Vcc	V
V_{IH}	High-level input voltage D$_0$–D$_7$, D$_8$–D$_{15}$	0.5 Vcc		Vcc	V
V_{IH}	High-level input voltage $\overline{RDY}$, $\overline{HOLD}$, TA0$_{IN}$–TA4$_{IN}$, TA0$_{OUT}$–TA4$_{OUT}$, TB0$_{IN}$–TB2$_{IN}$, $\overline{KI_0}$–$\overline{KI_3}$, $\overline{INT_0}$–$\overline{INT_4}$, $\overline{NMI}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK$_0$, CLK$_1$, RxD$_0$, RxD$_1$	0.5 Vcc		Vcc	V
V_{IH}	High-level input voltage SCLK, SDA **(Note 1)**	0.5 Vcc		Vcc	V
V_{IH}	Low-level input voltage X_{IN}, $\overline{RESET}$, BYTE, MD0, MD1	0		0.2 V_{CC}	V
V_{IL}	Low-level input voltage P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$	0		0.2 V_{CC}	V
V_{IL}	Low-level input voltage P0$_0$–P0$_7$ (When the port P0 input level select bit = “0”)	0		0.2 V_{CC}	V
V_{IL}	Low-level input voltage P0$_0$–P0$_7$ (When the port P0 input level select bit = “1”)	0		0.16 V_{CC}	V
V_{IL}	Low-level input voltage D$_0$–D$_7$, D$_8$–D$_{15}$	0		0.22 V_{CC}	V
V_{IL}	Low-level input voltage $\overline{RDY}$, $\overline{HOLD}$, TA0$_{IN}$–TA4$_{IN}$, TA0$_{OUT}$–TA4$_{OUT}$, TB0$_{IN}$–TB2$_{IN}$, $\overline{KI_0}$–$\overline{KI_3}$, $\overline{INT_0}$–$\overline{INT_4}$, $\overline{NMI}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK$_0$, CLK$_1$, RxD$_0$, RxD$_1$	0		0.16 V_{CC}	V
V_{IL}	Low-level input voltage SCLK, SDA **(Note 1)**	0		0.16 V_{CC}	V
$I_{OH(peak)}$	High-level peak output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$			–10	mA
$I_{OH(avg)}$	High-level average output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$			–5	mA
$I_{OL(peak)}$	Low-level peak output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$			10	mA
$I_{OL(avg)}$	Low-level average output current P0$_0$–P0$_7$, P1$_0$–P1$_7$, P2$_0$–P2$_7$, P3$_0$–P3$_3$, P4$_0$–P4$_7$, P5$_0$–P5$_7$, P6$_0$–P6$_7$, P7$_0$–P7$_7$, P8$_0$–P8$_7$, P10$_0$–P10$_7$, P11$_0$–P11$_7$			5	mA
f(X_{IN})	External clock input frequency **(Note 2)**			20	MHz
f(f_{sys})	System clock frequency			20	MHz

Notes 1: Pins SCLK and SDA are used only in the flash memory serial I/O mode.
2: When using the PLL frequency multiplier, be sure that f(f_{sys}) = 20 MHz or less.
3: Average output current is the average value of an interval of 100 ms.
4: The sum of $I_{OL(peak)}$ for ports P0–P2, P8, P10, and P11 must be 80 mA or less, the sum of $I_{OH(peak)}$ for ports P0–P2, P8, P10, and P11 must be 80 mA or less, the sum of $I_{OL(peak)}$ for ports P3–P7 must be 80 mA or less, the sum of $I_{OH(peak)}$ for ports P3–P7 must be 80 mA or less.

DC ELECTRICAL CHARACTERISTICS (Vcc = 3.3 V, Vss = 0 V, Ta = –20 to 85 °C, f(f_{sys}) = 20 MHz **(Note)**)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High-level output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, $P11_0$–$P11_7$	I_{OH} = –1 mA		2.5			V
V_{OH}	High-level output voltage $P3_1$–$P3_3$	I_{OH} = –1 mA		2.6			V
V_{OL}	Low-level output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, $P11_0$–$P11_7$	I_{OL} = 1 mA				0.5	V
V_{OL}	Low-level output voltage $P3_1$–$P3_3$	I_{OL} = 1 mA				0.4	V
V_{T+} —V_{T-}	Hysteresis $\overline{RDY}$, $\overline{HOLD}$, $TA0_{IN}$–$TA4_{IN}$, $TA0_{OUT}$–$TA4_{OUT}$, $TB0_{IN}$–$TB2_{IN}$, $\overline{KI_0}$–$\overline{KI_3}$, $\overline{INT_0}$–$\overline{INT_4}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK_0, CLK_1, RxD_0, RxD_1			0.08		0.5	V
V_{T+} —V_{T-}	Hysteresis $\overline{RESET}$			0.3		1	V
V_{T+} —V_{T-}	Hysteresis X_{IN}			0.05		0.26	V
I_{IH}	High-level input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, $P11_0$–$P11_7$, X_{IN}, $\overline{RESET}$, BYTE, MD0, MD1, $\overline{NMI}$	V_I = 3.3 V				4	V
I_{IL}	Low-level input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_3$, $P5_0$–$P5_3$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $P10_0$–$P10_7$, $P11_0$–$P11_7$, X_{IN}, $\overline{RESET}$, BYTE, MD0, MD1	V_I = 0 V				–4	μA
I_{IL}	Low-level input current $P4_4$–$P4_7$, $P5_4$–$P5_7$, $\overline{NMI}$	V_I = 0 V, No pullup transistor				–4	μA
		V_I = 0 V, Pullup transistor used		–0.20	–0.36	–0.54	mA
V_{RAM}	RAM hold voltage	When clock is stoped.		2			V
I_{CC}	Power source current	Output-only pins are open, and the other pins are connected to Vss or Vcc. An external square-waveform clock is input. (Pin X_{OUT} is open.) The PLL frequency multiplier stops its operation.	$f(f_{sys})$ = 20 MHz. CPU operates.		12	24	mA
			Ta = 25 °C when clock is stopped.			1	μA
			Ta = 85 °C when clock is stopped.			20	

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits		Unit
				Min.	Max.	
————	Resolution	V_{REF} = V_{CC}			10	Bits
————	Absolute accuracy	V_{REF} = V_{CC}	10-bit resolution mode		± 3	LSB
			8-bit resolution mode		± 2	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}		5		kΩ
t_{CONV}	Conversion time	f(f_{sys}) ≤ 20 MHz	10-bit resolution mode	5.90		μs
			8-bit resolution mode	2.45 **(Note)**		
V_{REF}	Reference voltage			2.7	V_{CC}	V
V_{IA}	Analog input voltage			0	V_{REF}	V

Note: This is applied when A-D conversion freguency (ϕ_{AD}) = f_1.

D-A CONVERTER CHARACTERISTICS

(V_{CC} = 3.3 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 3.3 V, T_a = –20 to 85 °C, unless otherwise noted)

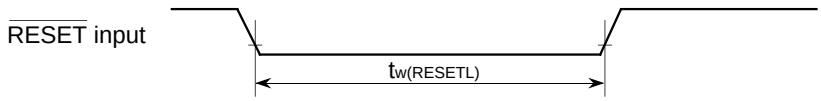
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
——	Resolution				8	Bits
——	Absolute accuracy				± 1.0	%
t_{su}	Set time				3	μs
R_O	Output resistance		1	2.5	4	kΩ
I_{VREF}	Reference power source input current	**(Note)**			3.2	mA

Note: The test conditions are as follows:
- One D-A converter is used.
- The D-A register value of the unused D-A converter is "00_{16}."
- The reference power source input current for the ladder resistance of the A-D converter is excluded.

RESET INPUT

Reset input timing requirements (V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(RESETL)}$	$\overline{RESET}$ input low-level pulse width	2			μs



PERIPHERAL DEVICE INPUT/OUTPUT TIMING

(V_{CC} = 3.3 V±0.3 V, V_{SS} = 0 V, T_a = –20 to 85 °C, f(f_{sys}) = 20 MHz unless otherwise noted)

✻ For limits depending on f(f_{sys}), their calculation formulas are shown below. Also, the values at f(f_{sys}) = 20 MHz are shown in ( ).

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	80		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	f(f_{sys}) ≤ 20 MHz	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width	f(f_{sys}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	f(f_{sys}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

Note : The TAiIN input cycle time requires 4 or more cycles of a count source. The TAiIN input high-level pulse width and the TAiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at f(f_{sys}) ≤ 20 MHz.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	f(f_{sys}) ≤ 20 MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TAH)}$	TAiIN input high-level pulse width		80		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width		80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high-level pulse width	80		ns
$t_{w(TAL)}$	TAiIN input low-level pulse width	80		ns

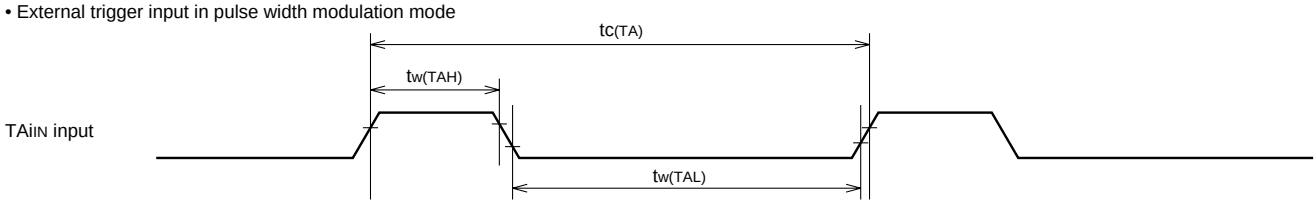
Timer A input (Up-down input and Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input high-level pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input low-level pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

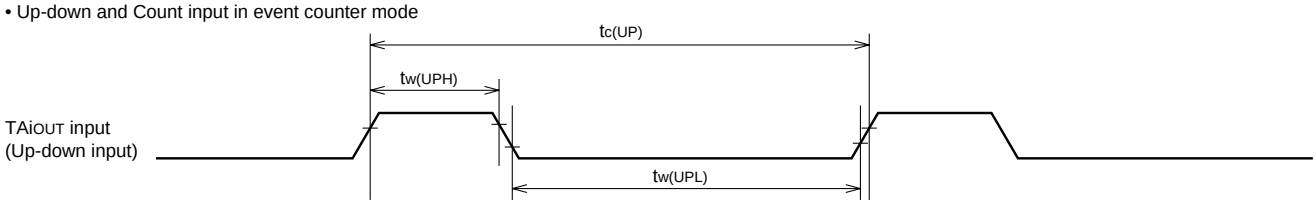
Timer A input (Two-phase pulse input in event counter mode)

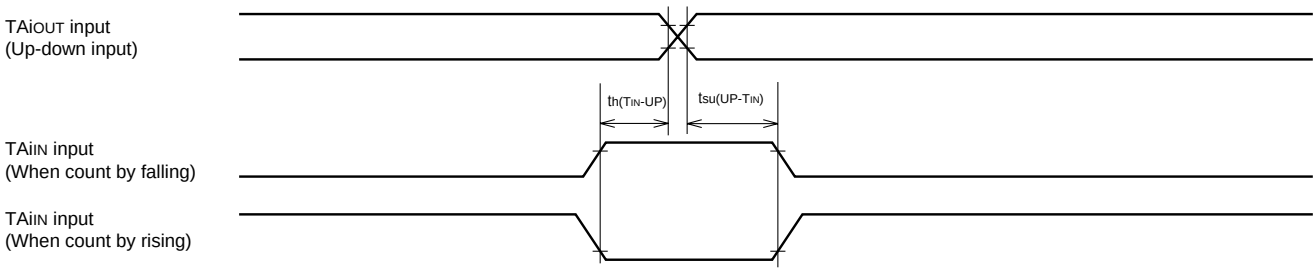
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TA_{iIN} input cycle time	800		ns
$t_{su(TA_{jIN}\text{-}TA_{jOUT})}$	TA_{jIN} input setup time	200		ns
$t_{su(TA_{jOUT}\text{-}TA_{jIN})}$	TA_{jOUT} input setup time	200		ns

• Gating input in timer mode
• Count input in event counter mode
• External trigger input in one-shot pulse mode
• External trigger input in pulse width modulation mode

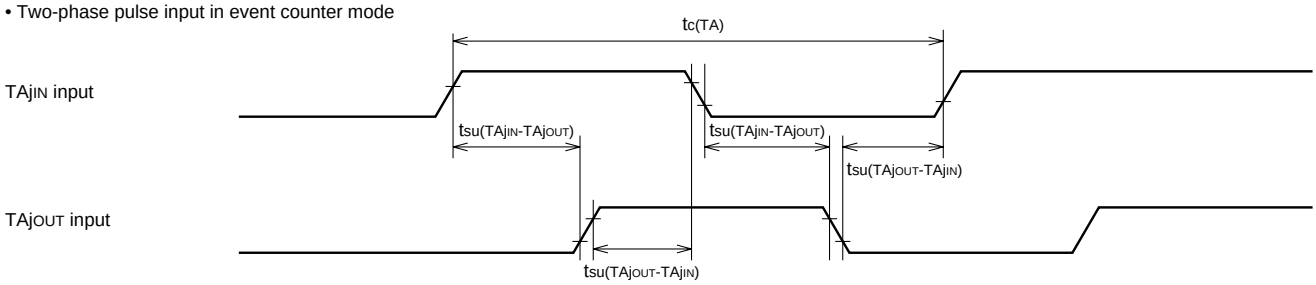


• Up-down and Count input in event counter mode





• Two-phase pulse input in event counter mode



Test conditions
• V_{CC} = 3.3 V±0.3 V, Ta = –20 to 85 °C
• Input timing voltage : V_{IL} = 0.53 V, V_{IH} = 1.65 V

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (one edge count)	80		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (one edge count)	40		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (one edge count)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (both edge count)	160		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width (both edge count)	80		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width (both edge count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$f(f_{sys}) \leq 20$ MHz	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at $f(f_{sys}) \leq 20$ MHz.

Timer B input (Pulse width measurement mode)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	$f(f_{sys}) \leq 20$ MHz	$\frac{16 \times 10^9}{f(f_{sys})}$ (800)		ns
$t_{w(TBH)}$	TBiIN input high-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns
$t_{w(TBL)}$	TBiIN input low-level pulse width	$f(f_{sys}) \leq 20$ MHz	$\frac{8 \times 10^9}{f(f_{sys})}$ (400)		ns

Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f_2 at $f(f_{sys}) \leq 20$ MHz.

A-D trigger input

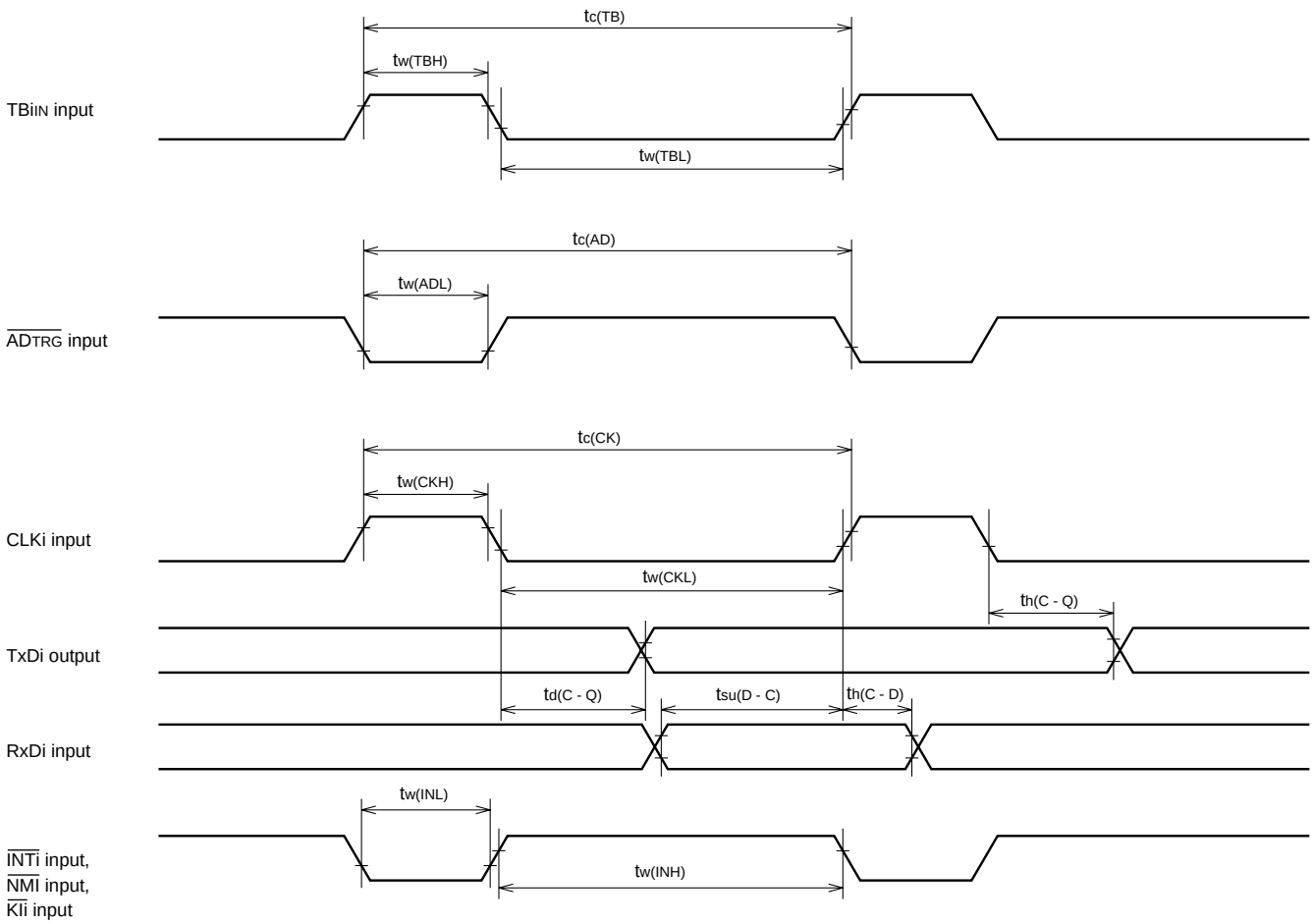
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (minimum allowable trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high-level pulse width	100		ns
$t_{w(CKL)}$	CLKi input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	20		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

External interrupt ($\overline{INT}_i$) input, $\overline{NMI}$ input, Key input interrupt ($\overline{KI}_i$) input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT}_i$ input/$\overline{NMI}$ input/$\overline{KI}_i$ input high-level pulse width	250		ns
$t_{w(INL)}$	$\overline{INT}_i$ input/$\overline{NMI}$ input/$\overline{KI}_i$ input low-level pulse width	250		ns



Test conditions
- Vcc = 3.3 V±0.3 V, Ta = –20 to 85°C
- Input timing voltage : V_{IL} = 0.53 V, V_{IH} = 1.65 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V, C_L = 50 pF

READY, HOLD TIMING

Timing requirements

(V_{CC} = 3.3 V±0.3 V, V_{SS} = 0 V, T_a = –20 to 85 °C, f(f_{sys}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(RDY-\phi1)}$	$\overline{RDY}$ input setup time	40		ns
$t_{su(HOLD-\phi1)}$	$\overline{HOLD}$ input setup time	40		ns
$t_{h(\phi1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

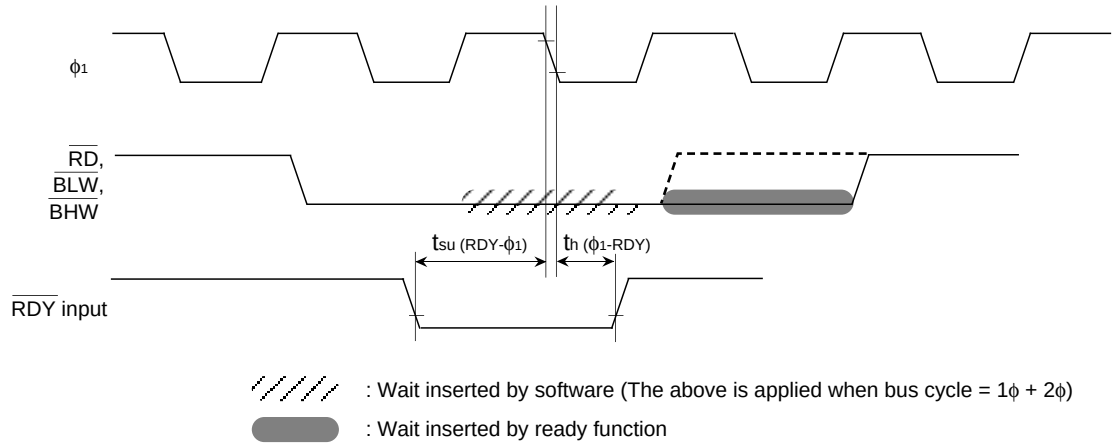
Switching characteristics

(V_{CC} = 3.3 V±0.3 V, V_{SS} = 0 V, T_a = –20 to 85 °C, f(f_{sys}) = 20 MHz, unless otherwise noted)

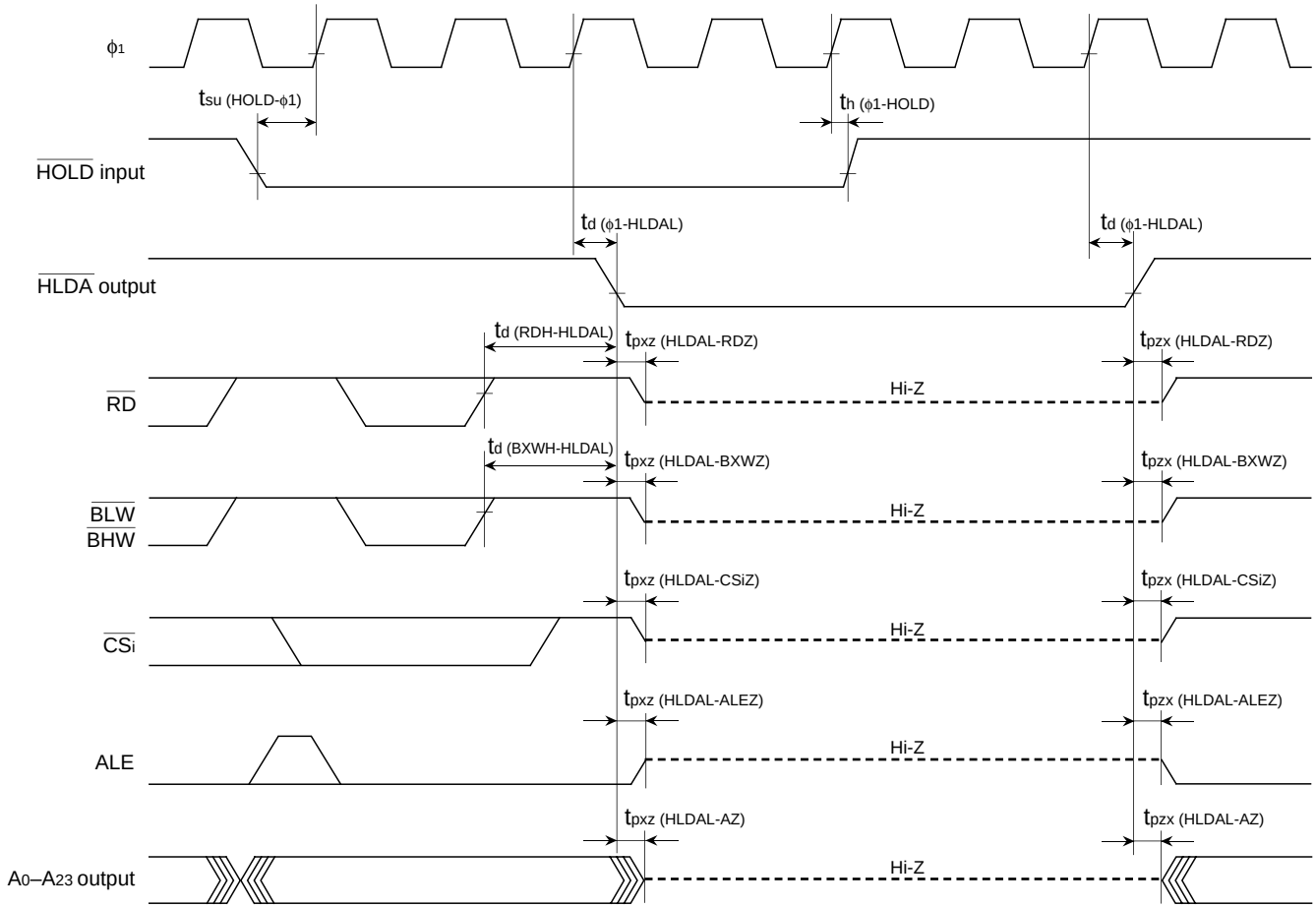
Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{d(\phi1-HLDAL)}$	$\overline{HLDA}$ output delay time		20	ns
$t_{d(RDH-HLDAL)}$	$\overline{HLDA}$ low-level output delay time after read	t_c –15 **(Note)**		ns
$t_{d(BXWH-HLDAL)}$	$\overline{HLDA}$ low-level output delay time after write	t_c –15 **(Note)**		ns
$t_{pxz(HLDAL-RDZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-BXWZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-CSiZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-ALEZ)}$	Floating start delay time	–15	10	ns
$t_{pxz(HLDAL-AZ)}$	Floating start delay time	–15	10	ns
$t_{pzx(HLDAL-RDZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-BXWZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-CSiZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-ALEZ)}$	Floating release delay time	0		ns
$t_{pzx(HLDAL-AZ)}$	Floating release delay time	0		ns

Note: $t_c = 1/f(f_{sys})$.

$\overline{\text{RDY}}$ input



$\overline{\text{HOLD}}$ input



Test conditions

- V_{CC} = 3.3 V ± 0.3 V, Ta= –20 to 85 °C
- $\overline{\text{RDY}}$ input, $\overline{\text{HOLD}}$ input:V_{IL} = 0.53 V, V_{IH} = 1.65 V
- $\overline{\text{HLDA}}$ output : V_{OL} = 0.8V, V_{OH} = 2.0 V, C_L = 50 pF

External bus timing

For limits depending on f(f_{sys}), their calculation formulas are shown below.

Bus cycle	W_H	W_L	Bus cycle	W_H	W_L
1ϕ +1ϕ	1	1	2ϕ +3ϕ	2	3
1ϕ +2ϕ	1	2	2ϕ +4ϕ	2	4
1ϕ +3ϕ	1	3	3ϕ +3ϕ	3	3
2ϕ +2ϕ	2	2	3ϕ +4ϕ	3	4

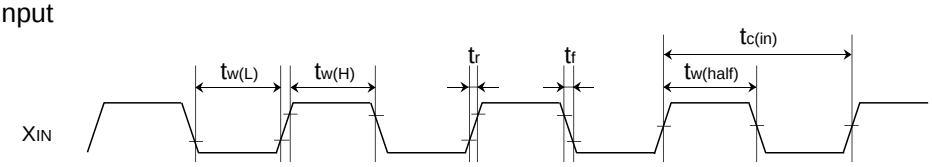
tc = 1/f(f_{sys}).

Timing Requirements (V_{CC} = 3.3 V±0.3 V, V_{SS} = 0 V, Ta = –20 to 85 °C, f(X_{IN}) = 20 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(in)}$	External clock input cycle time	50		ns
$t_{w(half)}$	External clock input pulse width with half input-volage	0.45 tc	0.55 tc	ns
$t_{w(H)}$	External clock input high-level pulse width	0.5 tc – 6		ns
$t_{w(L)}$	External clock input low-level pulse width	0.5 tc – 6		ns
t_r	External clock input rise time	6		ns
t_f	External clock input fall time	6		ns
$t_{a(A-D)}$	Address access time (the address output select bit = 0)		(W_H + W_L) tc-45	ns
$t_{a(A-D)}$	Address access time (the address output select bit = 1)		(W_H + W_L-0.5) tc-35	ns
$t_{a(CSiL-D)}$	Chip select access time		(W_H + W_L-0.5) tc-35	ns
$t_{a(RDL-D)}$	Read access time		W_L × tc-30	ns
$t_{su(D-RDL)}$	Read data setup time	15		ns
$t_{h(RDH-D)}$	Data input hold time after read	0		ns
$t_{a(BA-D)}$	Address access time at burst ROM access		W_L × tc-35	ns
$t_{h(BA-D)}$	Data hold time after address at burst ROM access	8		ns
$t_{a(LA-D)}$	Address access time (the multiplexed bus select bit = 1)	(W_H + W_L-0.5)tc-35 **(Note)**		ns

Note: This is independent of the value of the address output select bit's contents.

External clock input



Test conditions
- Vcc = 3.3 V ± 0.3 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL} = 0.66 V, V_{IH} = 2.64 V (tw(H), tw(L), tr, tf)
- Output timing voltage : 1.65 V (tc(in), tw(half))

Switching characteristics (V_{CC} = 3.3 V±0.3 V, V_{SS} = 0 V, T_a = –20 to 85 °C, f(f_{sys}) = 20 MHz, unless otherwise noted)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
td(φ1-RDL)	Read low-level output delay time		–18	0	ns
td(φ1-RDH)	Read high-level output delay time		–18	0	ns
td(φ1-BXWL)	Write low-level output delay time		–18	0	ns
td(φ1-BXWH)	Write high-level output delay time		–18	0	ns
td(φ1L-CSiL)	Chip select low-level output delay time		–20	0	ns
td(φ1L-CSiH)	Chip select high-level output delay time		–22	10	ns
td(φ1H-A)	Address output delay time (the address output select bit = 0)		–5	25	ns
td(φ1L-A)	Address output delay time (the address output select bit = 1)		–20	16	ns
tw(ALEH)	ALE pulse width	Bus cycle = 1φ + 1φ, 1φ + 2φ, 1φ + 3φ	0.5tc-19		ns
		Bus cycle = 2φ + 2φ	tc-20		ns
		Bus cycle = 2φ + 3φ, 2φ + 4φ, 3φ + 3φ, 3φ + 4φ	1.5tc-20		ns
td(A-ALEL)	ALE completion delay time after address stabilization (when the address output select bit = 0)	Bus cycle = 1φ + 1φ, 1φ + 2φ, 1φ + 3φ	tc-30		ns
		Bus cycle = 2φ + 2φ	1.5tc-30		ns
		Bus cycle = 2φ + 3φ, 2φ + 4φ, 3φ + 3φ, 3φ + 4φ	2tc-30		ns
	ALE completion delay time after address stabilization (when the address output select bit = 1)	Bus cycle = 1φ + 1φ, 1φ + 2φ, 1φ + 3φ	0.5tc-19		ns
		Bus cycle = 2φ + 2φ	tc-20		ns
		Bus cycle = 2φ + 3φ, 2φ + 4φ, 3φ + 3φ, 3φ + 4φ	1.5tc-20		ns
tw(RDL)	Read output pulse width		W_L × tc-15		ns
tw(RDH)	Read output high-level width **(Note 1)**		W_H × tc-15		ns
td(RDH-BXWH)	Write disable valid time after read **(Note 2)**		tc-15		ns
td(A-RDH)	Address valid time before read (when the address output select bit = 0)		W_H × tc-30		ns
td(A-RDH)	Address valid time before read (when the address output select bit = 1)		(W_H-0.5)tc-19		ns
th(RDH-A)	Address hold time after read (when the address output select bit = 0) **(Note 2)**		8		ns
th(RDH-A)	Address hold time after read (when the address output select bit = 1) **(Note 2)**		0.5tc-10		ns
td(RDH-ALEL)	ALE completion delay time after read start			20	ns
td(ALEL-RDH)	Read disable valid time after ALE completion	Bus cycle = 2φ + 2φ	0.5tc-19		ns
		Bus cycle = 3φ + 3φ, 3φ + 4φ	tc-15		ns
td(CSiL-RDH)	Chip select valid time before read		(W_H-0.5)tc-19		ns
td(CSiL-RDL)	Chip select output valid time before read completion		(W_H + W_L-0.5)tc-20		ns
th(RDH-CSiL)	Chip select hold time after read		0.5tc-14		ns
td(RDH-D)	Next write cycle data output delay time after read **(Note 2)**		tc-15		ns
tw(BXWL)	Write output pulse width		W_L × tc-15		ns
tw(BXWH)	Write output high-level width **(Note 1)**		W_H × tc-15		ns
td(BXWH-RDH)	Read disable valid time after write **(Note 2)**		tc-15		ns
td(A-BXWH)	Address valid time before write (when the address output select bit = 0)		W_H × tc-30		ns
td(A-BXWH)	Address valid time before write (when the address output select bit = 1)		(W_H-0.5)tc-19		ns
th(BXWH-A)	Address hold time after write (when the address output select bit = 0) **(Note 2)**		8		ns
th(BXWH-A)	Address hold time after write (when the address output select bit = 1) **(Note 2)**		0.5tc-10		ns
td(BXWH-ALEL)	ALE completion delay time after write start			20	ns
td(ALEL-BXWH)	Write disable valid time after ALE completion	Bus cycle = 2φ + 2φ	0.5tc-19		ns
		Bus cycle = 2φ + 3φ, 2φ + 4φ, 3φ + 3φ, 3φ + 4φ	tc-15		ns
td(CSiL-BXWH)	Chip select valid time before write		(W_H-0.5)tc-19		ns
td(CSiL-BXWL)	Chip select output valid time before write completion		(W_H + W_L-0.5)tc-20		ns
th(BXWH-CSiL)	Chip select hold time after write		0.5tc-14		ns
td(D-BXWL)	Data output valid time before write completion		W_L × tc-20		ns
th(BXWH-D)	Data hold time after write **(Note 3)**		0.5tc-10		ns
tpxz(BXWH-DZ)	Floating start delay time after write **(Note 3)**			0.5tc + 10	ns

Notes 1: When the bus cycle just before this parameter is for the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns: one recovery cycle is inserted.) or by 2tc (ns: two recovery cycles are inserted.).

2: When accessing the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns: one recovery cycle is inserted.) or by 2tc (ns: two recovery cycles are inserted.).

3: This parameter is extended by tc (ns) when both of the following conditions are satisfied:

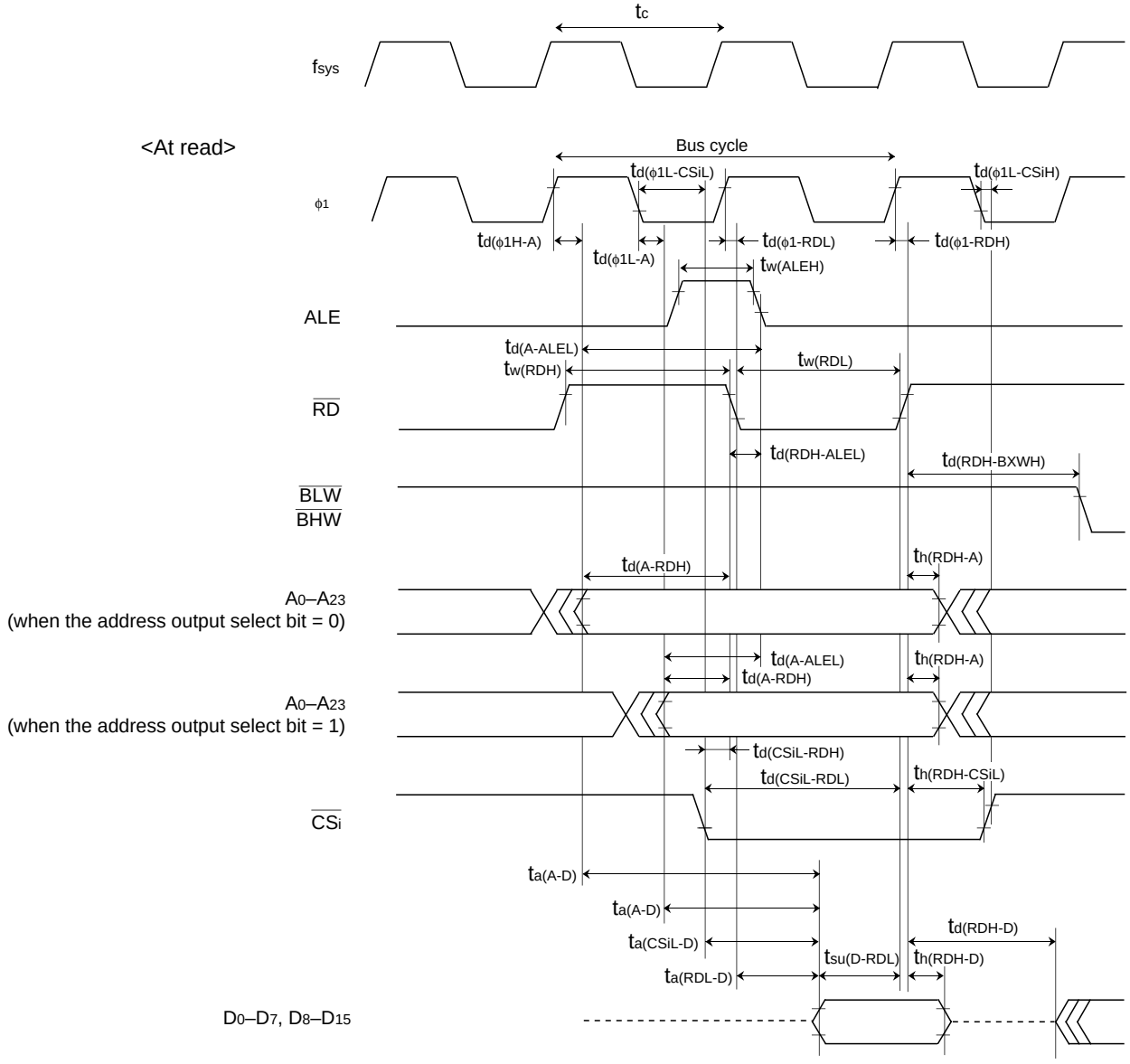
- When accessing the area where the recovery cycle insertion is selected.
- When two recovery cycles are inserted.

Switching characteristics (V_{CC} = 3.3 V±0.3 V, V_{SS} = 0 V, T_a = –20 to 85 °C, f(f_{sys}) = 20 MHz, unless otherwise noted)

Symbol	Parameter		Limits		Unit
			Min.	Max.	
$t_{d(LA-RDH)}$	Address valid time before read		(W_H-0.5)tc-19 **(Note)**		ns
$t_{d(LA-ALEL)}$	ALE completion delay time after address stabilization	Bus cycle = 2ϕ + 2ϕ	tc-20 **(Note)**		ns
		Bus cycle = 3ϕ + 3ϕ, 3ϕ + 4ϕ	1.5tc-20 **(Note)**		ns
$t_{h(ALEL-LA)}$	Address hold time after ALE completion	Bus cycle = 2ϕ + 2ϕ	0.5tc-19		ns
		Bus cycle = 3ϕ + 3ϕ, 3ϕ + 4ϕ	tc-15		ns
$t_{pxz(RDH-LAZ)}$	Floating start delay time			5	ns
$t_{d(LA-BXWH)}$	Address valid time before write		(W_H-0.5)tc-19 **(Note)**		ns
$t_{pzx(RDH-DZ)}$	Floating release delay time		0.5tc-19 **(Note)**		ns

Note: This is independent of the address output select bit's contents.

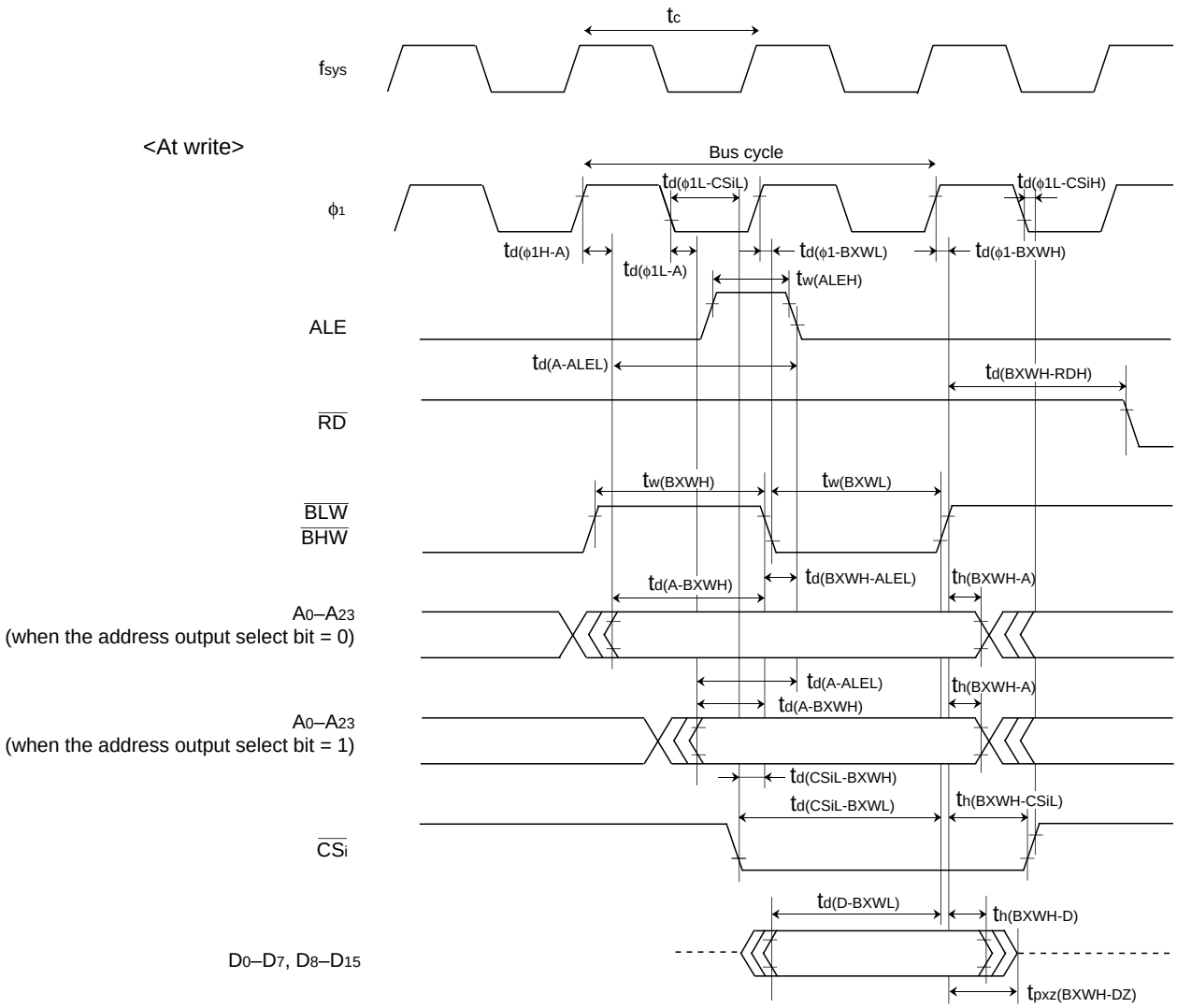
Normal access: bus cycle = 1ϕ + 1ϕ, 1ϕ + 2ϕ, 1ϕ+ 3ϕ,
2ϕ + 3ϕ, or 2ϕ + 4ϕ



Test conditions

- V_{CC} = 3.3 V ±0.3 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL}=0.53 V, V_{IH}=1.65 V
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=15 pF ($\overline{CS_i}$)
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=50 pF (except for $\overline{CS_i}$)

Normal access: bus cycle = 1ϕ + 1ϕ, 1ϕ + 2ϕ, 1ϕ + 3ϕ,
2ϕ + 3ϕ, or 2ϕ + 4ϕ

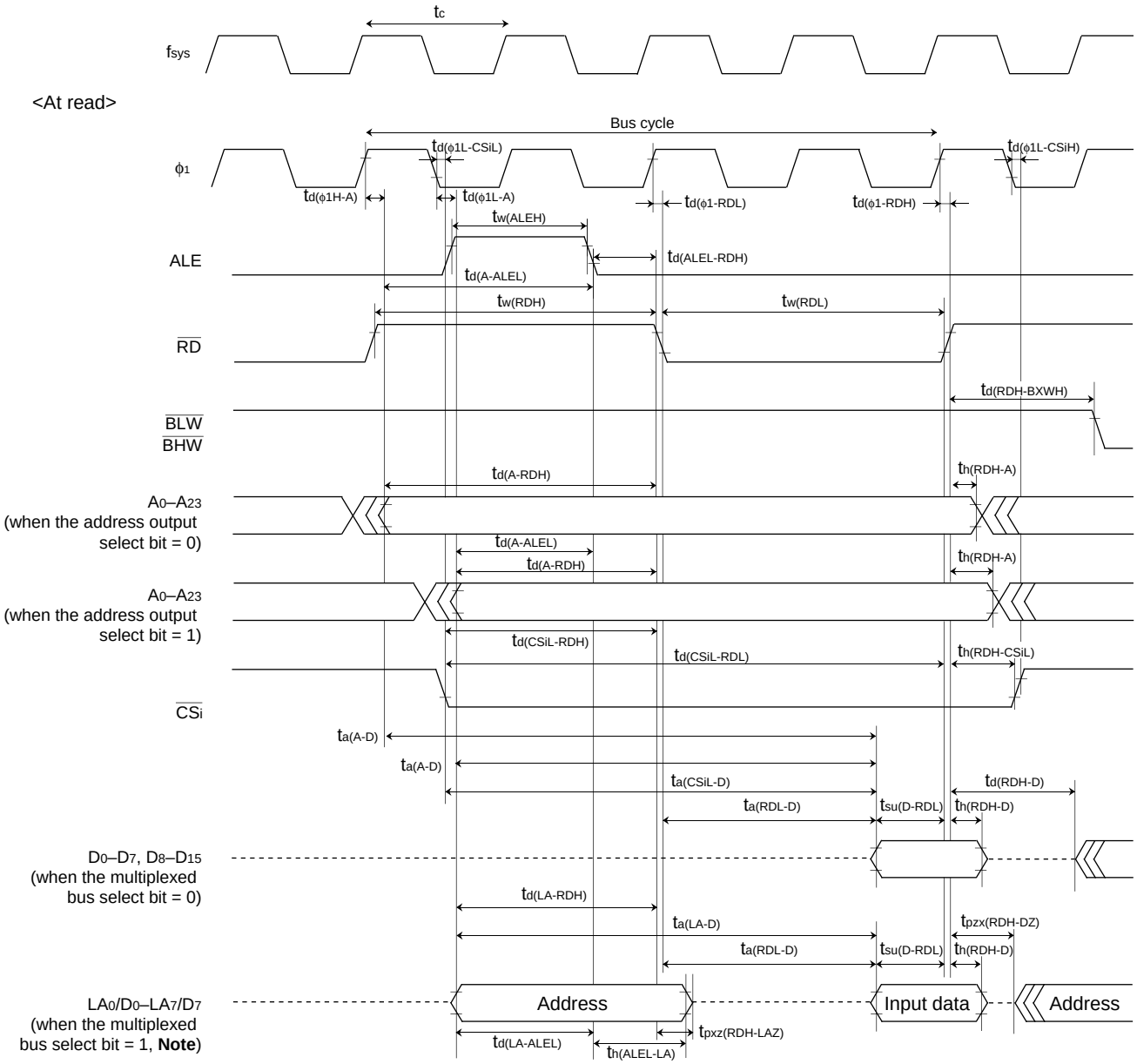


Test conditions

- V_{CC} = 3.3 V ±0.3 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL}=0.53 V, V_{IH}=1.65 V
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=15 pF ($\overline{CS_i}$)
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=50 pF (except for $\overline{CS_i}$)

Normal access: bus cycle = 2ϕ + 2ϕ, 3ϕ + 3ϕ, 3ϕ + 4ϕ

<At read>



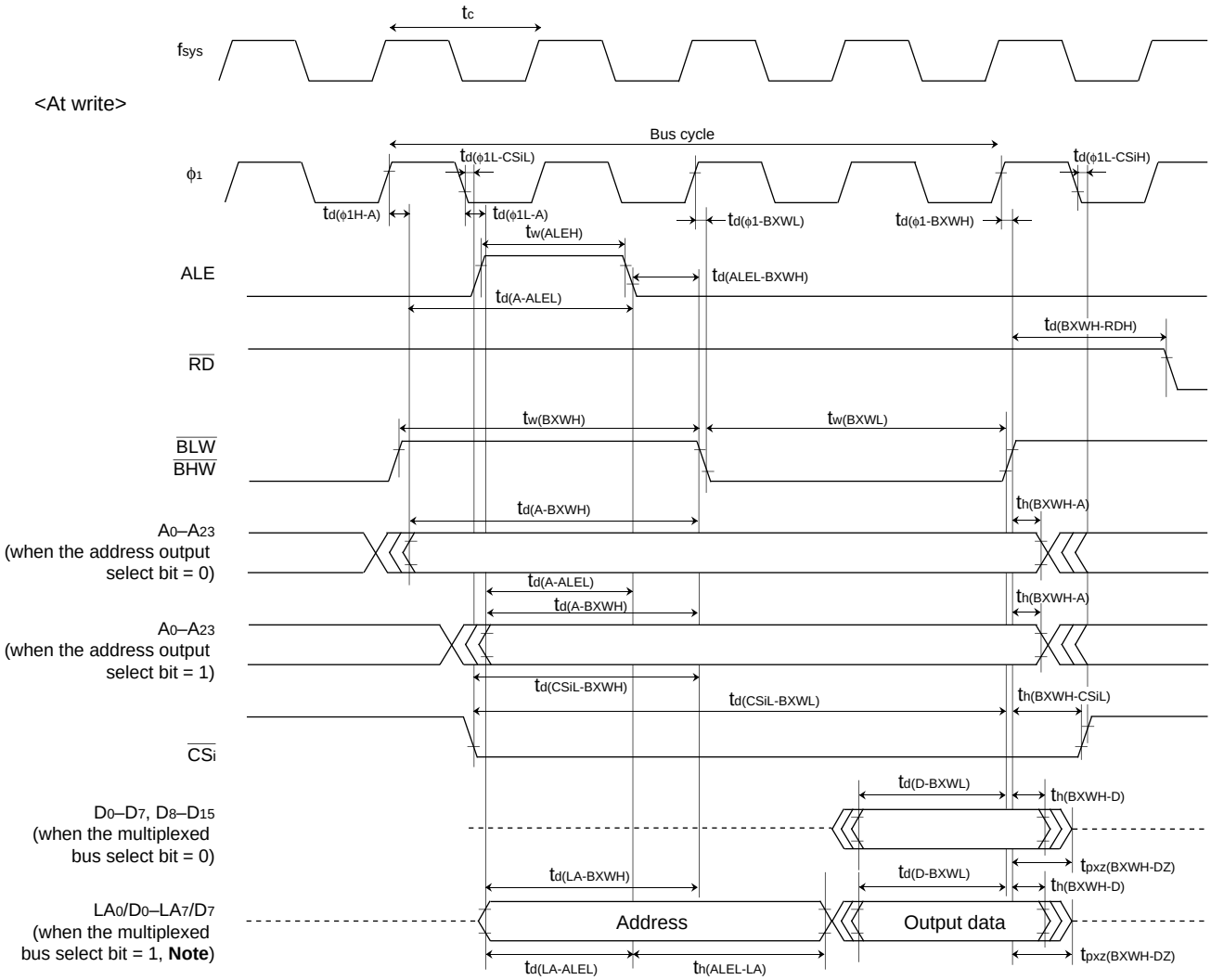
Note: Valid only when area $\overline{CS_2}$ is accessed with the external data bus width = 8 bits.

Test conditions

- V_{CC} = 3.3 V ±0.3 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL}=0.53 V, V_{IH}=1.65 V
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=15 pF ($\overline{CS_i}$)
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=50 pF (except for $\overline{CS_i}$)

Normal access: bus cycle = 2ϕ + 2ϕ, 3ϕ + 3ϕ, 3ϕ + 4ϕ

<At write>

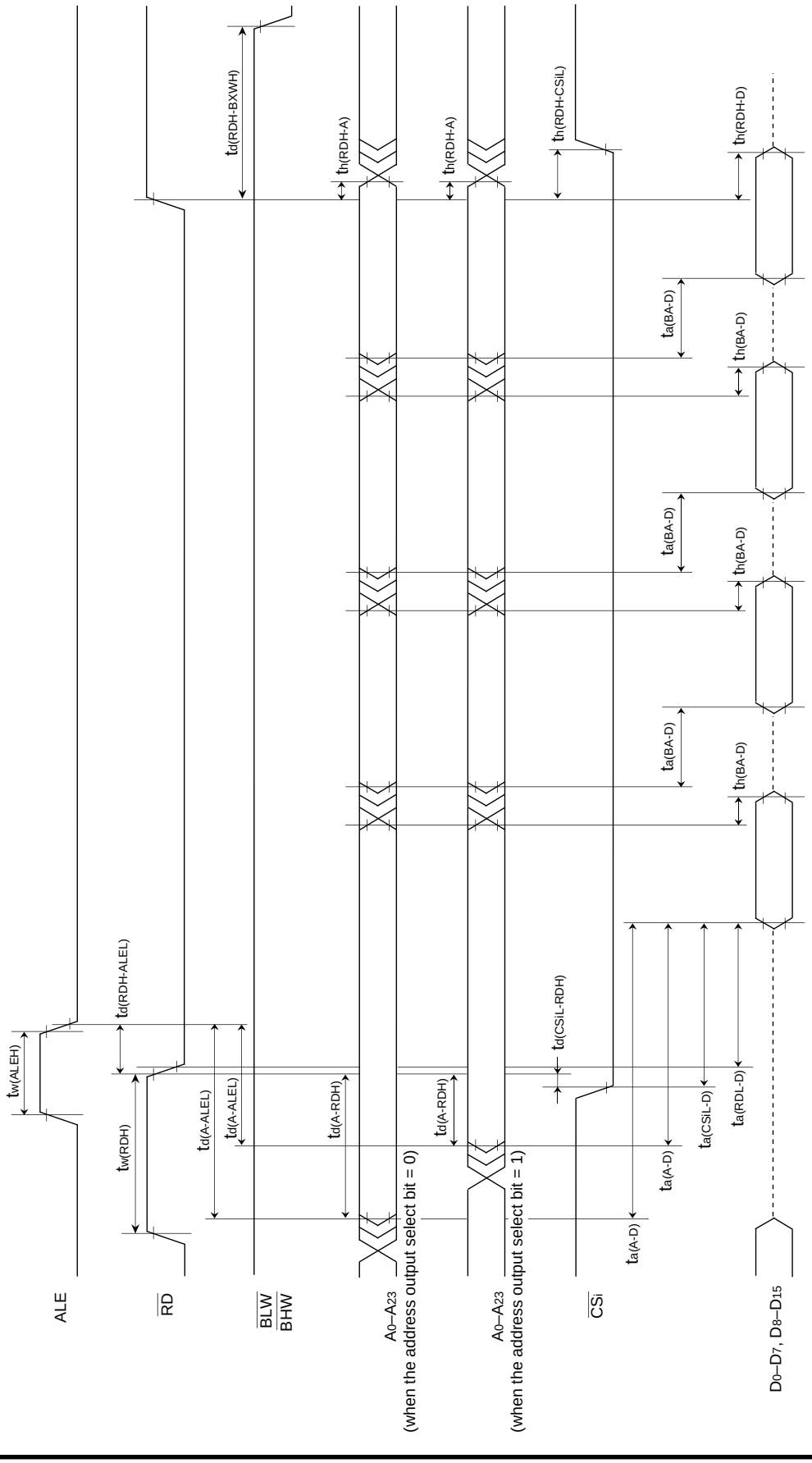


Note: Valid only when area $\overline{CS_2}$ is accessed with the external data bus width = 8 bits.

Test conditions

- V_{CC} = 3.3 V ±0.3 V, Ta = –20 to 85 °C
- Input timing voltage : V_{IL}=0.53 V, V_{IH}=1.65 V
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=15 pF ($\overline{CS_i}$)
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=50 pF (except for $\overline{CS_i}$)

Burst ROM access: bus cycle = 1φ + 1φ, 1φ + 2φ, 1φ + 3φ, 2φ + 3φ, 2φ + 4φ



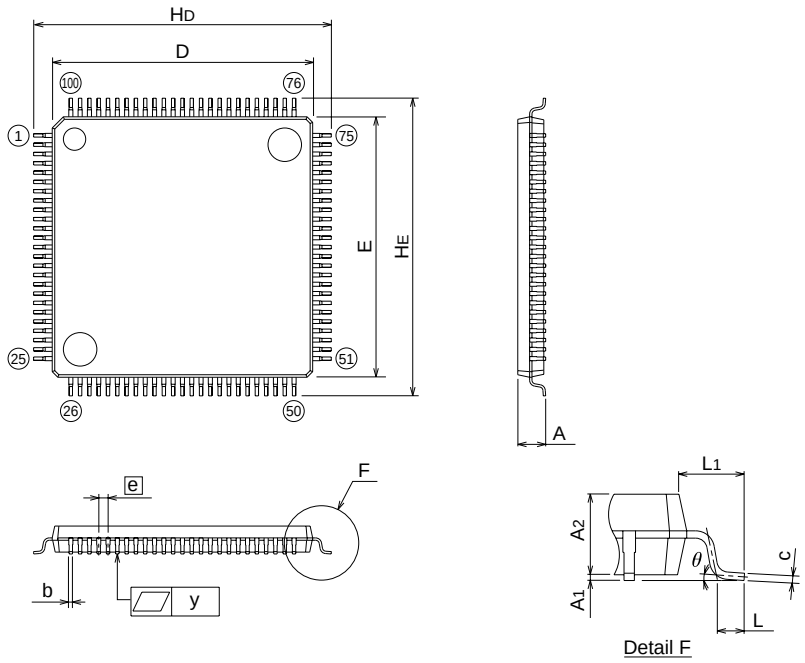
Test conditions
- V_{CC} = 3.3 V±0.3 V, Ta = –20 to 85°C
- Input timing voltage : V_{IL}=0.53 V, V_{IH}=1.65 V
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=15 pF ($\overline{CS_i}$)
- Output timing voltage: V_{OL}=0.8 V, V_{OH}=2.0 V, C_L=50 pF (except for $\overline{CS_i}$)

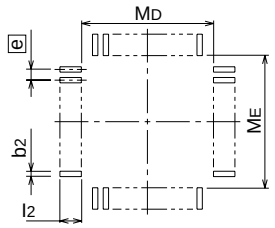
PACKAGE OUTLINE

100P6Q-A

Plastic 100pin 14×14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	–		Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	–	0.5	–
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	–	1.0	–
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	1.0	–	–
MD	–	14.4	–
ME	–	14.4	–

Keep safety first in your circuit designs!

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

- These materials are intended as a reference to assist our customers in the selection of the Mitsubishi semiconductor product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Mitsubishi Electric Corporation or a third party.
- Mitsubishi Electric Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
- All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Mitsubishi Electric Corporation without notice due to product improvements or other reasons. It is therefore recommended that customers contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for the latest product information before purchasing a product listed herein.
  The information described here may contain technical inaccuracies or typographical errors. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
  Please also pay attention to information published by Mitsubishi Electric Corporation by various means, including the Mitsubishi Semiconductor home page (http://www.mitsubishichips.com).
- When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Mitsubishi Electric Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
- Mitsubishi Electric Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
- The prior written approval of Mitsubishi Electric Corporation is necessary to reprint or reproduce in whole or in part these materials.
- If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
  Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
- Please contact Mitsubishi Electric Corporation or an authorized Mitsubishi Semiconductor product distributor for further details on these materials or the products contained therein.

© 2000 MITSUBISHI ELECTRIC CORP.
New publication, effective Jun., 2000.
Specifications subject to change without notice.

MITSUBISHI ELECTRIC

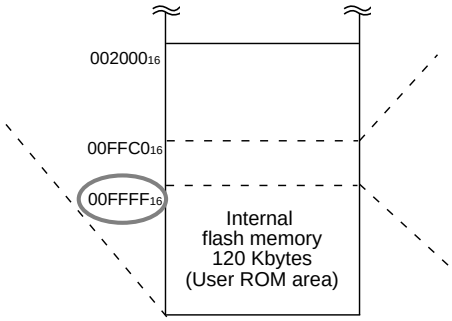
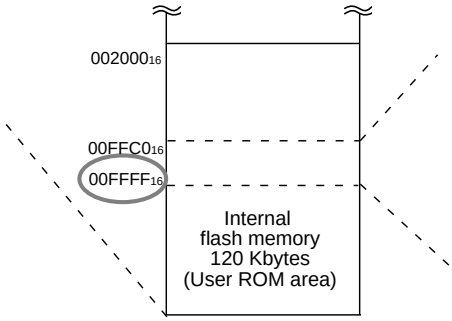
Revision History	M37902FxMHP Datasheet

Rev. No.	Revision Description	Rev. date
1.0	First Edition	990305
2.0	Refer to **Corrections and Supplementary Explanation for "M37902FxM Datasheet (REV.A)".**	990625
3.0	The following are revised/added points in this edition: • Page 20; **RECOMMENDED OPERATING CONDITIONS** <Error> f(f_{SYS}) | External clock input frequency **(Note 2)** | •••••••••• <Correction> f(X_{IN}) | External clock input frequency **(Note 2)** | •••••••••• • Page 21; the maximum value of I_{CC} is revised. <Error> Ta = 25 °C when clock is stopped : — Ta = 85 °C when clock is stopped : — <Correction> Ta = 25 °C when clock is stopped : 1 Ta = 85 °C when clock is stopped : 20	990917
4.0	Refer to **Corrections and Supplementary Explanation for "M37902FxM Datasheet (REV.B)".** **Notes 1:** ★ represents the new information added in Rev.4.0. **2:** The revised/added points informed in Rev.3.0 are included in **Corrections and Supplementary Explanation for "M37902FxM Datasheet (REV.B)".**	000609

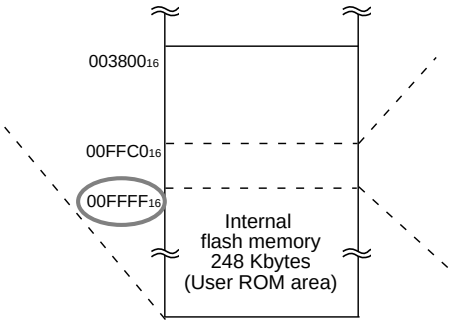
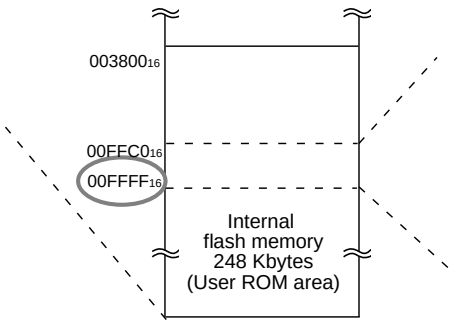
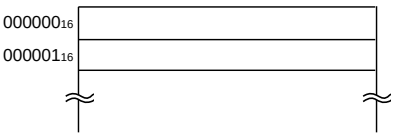
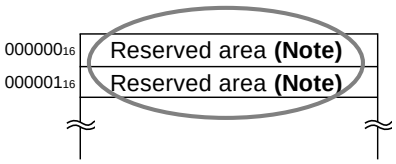
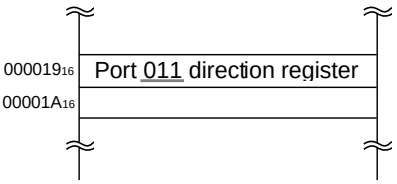
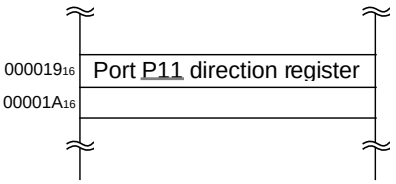
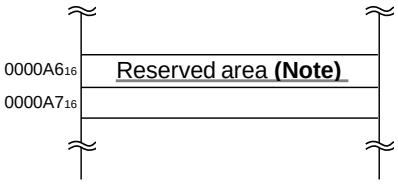
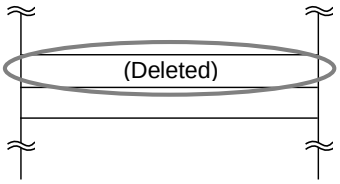
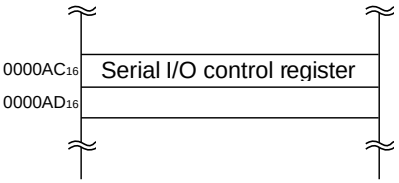
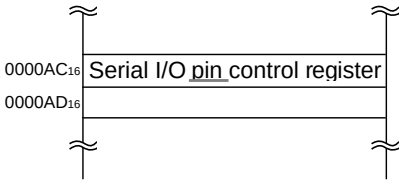
Corrections and Supplementary Explanation for M37902FxM Datasheet (REV.B) NO.1

	Page	Error	Correction
★	All pages, Header	PRELIMINARY Notice: This is not a final specification. Some parametric limits are subject to change.	(Deleted)
		M37902F8MHP, M37902FCMHP, M37902FEMHP, M37902FGMHP, M37902FHMHP, M37902FJMHP	M37902FCMHP, M37902FGMHP
★	Page 1, DISTINCTIVE FEATURES ; Memory	[M37902F8MHP] Flash memory (User ROM area) .....60 Kbytes RAM.....2048 bytes	(Deleted)
		[M37902FEMHP] Flash memory (User ROM area) .....184 Kbytes RAM.....6144 bytes	(Deleted)
		[M37902FHMHP] Flash memory (User ROM area) .....370 Kbytes RAM.....12288 bytes	(Deleted)
		[M37902FJMHP] Flash memory (User ROM area) .....498 Kbytes RAM.....12288 bytes	(Deleted)
★	Page 1, DISTINCTIVE FEATURES ; Instruction execution time	The fastest instruction at 26 MHz frequency .....38 ns	The fastest instruction at 20 MHz frequency .....50 ns
★	Page 1, APPLICATION	Control devices for personal computer peripheral equipment such as CD-ROM drives, DVD-ROM drives, hard disk drives, high density FDD, printers Control devices for office equipment such as copiers and facsimiles Control devices for industrial equipment such as communication and measuring instruments	Control devices for personal computer peripheral equipment such as CD-ROM drives, DVD-ROM drives, hard disk drives, high density FDD, printers
★	Page 2, PIN CONFIGURATION	$P6_3/\overline{INT_2}$	$P6_4/\overline{INT_2}$
		(Type) M37902F8MHP M37902FCMHP M37902FEMHP M37902FGMHP M37902FHMHP M37902FJMHP	(Type) M37902FCMHP M37902FGMHP
★	Page 3, BLOCK DIAGRAM, **Note:**	**Note:** |	Flash memory	RAM | |---|---|---| | M37902F8MHP	60 Kbytes	2048 bytes | | M37902FCMHP	120 Kbytes	4096 bytes | | M37902FEMHP	184 Kbytes	6144 bytes | | M37902FGMHP	248 Kbytes	6144 bytes | | M37902FHMHP	370 Kbytes	12288 bytes | | M37902FJMHP	498 Kbytes	12288 bytes		**Note:** |	Flash memory	RAM | |---|---|---| | M37902FCMHP	120 Kbytes	4096 bytes | | M37902FGMHP	248 Kbytes	6144 bytes	
★	Page 4, Instruction execution time	38 ns (the fastest instruction at $f(f_{sys})$ = 26 MHz)	50 ns (the fastest instruction at $f(f_{sys})$ = 20 MHz)
★	Page 4, External clock input frequency $f(X_{IN})$, System clock frequency f_{sys}	26 MHz (Max.)	20 MHz (Max.)
	Page 4, Chip-select wait control	Chip select area × 4 ($\overline{CS_0}$–$\overline{CS_3}$). A wait number and bus width can be set for each chip select area.	Chip select area × 4 ($\overline{CS_0}$–$\overline{CS_3}$). A bus cycle type and bus width can be set for each chip select area.

Corrections and Supplementary Explanation for M37902FxM Datasheet (REV.B) NO.2

<table>
<tr><th></th><th>Page</th><th>Error</th><th>Correction</th></tr>
<tr><td>★</td><td>Page 4,
Power dissipation</td><td>51.5 mW (at f(fsys) = 26 MHz, Typ., •••••</td><td>39.6 mW (at f(fsys) = 20 MHz, Typ., •••••</td></tr>
<tr><td>★</td><td>Page 4,
Operating temperature range</td><td>Operating temperature range</td><td>Operating ambient temperature range</td></tr>
<tr><td>★</td><td>Page 4,
Note:</td><td>Note:
<table><tr><td>Flash memory (User ROM area)</td><td>M37902F8MHP</td><td>60 Kbytes</td></tr><tr><td></td><td>M37902FCMHP</td><td>120 Kbytes</td></tr><tr><td></td><td>M37902FEMHP</td><td>184 Kbytes</td></tr><tr><td></td><td>M37902FGMHP</td><td>248 Kbytes</td></tr><tr><td></td><td>M37902FHMHP</td><td>370 Kbytes</td></tr><tr><td></td><td>M37902FJMHP</td><td>498 Kbytes</td></tr><tr><td>RAM</td><td>M37902F8MHP</td><td>2048 bytes</td></tr><tr><td></td><td>M37902FCMHP</td><td>4096 bytes</td></tr><tr><td></td><td>M37902FEMHP</td><td>6144 bytes</td></tr><tr><td></td><td>M37902FGMHP</td><td>6144 bytes</td></tr><tr><td></td><td>M37902FHMHP</td><td>12288 bytes</td></tr><tr><td></td><td>M37902FJMHP</td><td>12288 bytes</td></tr></table></td><td>Note:
<table><tr><td>Flash memory (User ROM area)</td><td>M37902FCMHP</td><td>120 Kbytes</td></tr><tr><td></td><td>M37902FGMHP</td><td>248 Kbytes</td></tr><tr><td>RAM</td><td>M37902FCMHP</td><td>4096 bytes</td></tr><tr><td></td><td>M37902FGMHP</td><td>6144 bytes</td></tr></table></td></tr>
<tr><td>★</td><td>Page 5,
Notes 1:</td><td><table><tr><td>User ROM area</td><td>M37902F8MHP</td><td>4 blocks ••••••</td></tr><tr><td></td><td>M37902FCMHP</td><td>5 blocks ••••••</td></tr><tr><td></td><td>M37902FEMHP</td><td>6 blocks ••••••</td></tr><tr><td></td><td>M37902FGMHP</td><td>7 blocks ••••••</td></tr><tr><td></td><td>M37902FHMHP</td><td>9 blocks ••••••</td></tr><tr><td></td><td>M37902FJMHP</td><td>11 blocks •••••</td></tr></table></td><td><table><tr><td>User ROM area</td><td>M37902FCMHP</td><td>5 blocks ••••••</td></tr><tr><td></td><td>M37902FGMHP</td><td>7 blocks••••••</td></tr></table></td></tr>
<tr><td>★</td><td>Page 6,
P40–P47</td><td>•••••••••••••••
■ In microprocessor mode
•••••••• According to the register setting, P40–P44 also ••••••••••</td><td>•••••••••••••••
■ In microprocessor mode
•••••••• According to the register setting, P40–P43 also ••••••••••</td></tr>
<tr><td>★</td><td>———</td><td>Memory map of M37902F8MHP (Single-chip mode)</td><td>(Deleted)</td></tr>
<tr><td rowspan="2">★</td><td rowspan="2">Page 9,
Fig. 1</td><td>Fig. 2 Memory map of M37902FCMHP (Single-chip mode)</td><td>Fig. 1 Memory map of M37902FCMHP (Single-chip mode)</td></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td rowspan="3">★</td><td rowspan="3">———</td><td>Memory map of M37902FEMHP (Single-chip mode)</td><td>(Deleted)</td></tr>
<tr><td>Memory map of M37902FHMHP (Single-chip mode)</td><td>(Deleted)</td></tr>
<tr><td>Memory map of M37902FJMHP (Single-chip mode)</td><td>(Deleted)</td></tr>
</table>

Corrections and Supplementary Explanation for M37902FxM Datasheet (REV.B) NO.3

Page	Error	Correction
★ Page 10, Fig. 2	Fig. 4. Memory map of M37902FGMHP (Single-chip mode)	Fig. 2. Memory map of M37902FGMHP (Single-chip mode)
		
Page 11, Fig. 7 ★ address 00₁₆, 01₁₆		
address 19₁₆		
Page 12, Fig. 8 ★ address A6₁₆		
address AC₁₆, AD₁₆		
★ ———	M37902F8MHP : block configuration of internal flash memory	(Deleted)
	M37902FEMHP : block configuration of internal flash memory	(Deleted)
★ Page 13, Fig. 9	Fig. 10. M37902FCMHP : block configuration of internal flash memory	Fig. 9. M37902FCMHP : block configuration of internal flash memory
★ Page 14, Fig. 10	Fig. 12. M37902FGMHP : block configuration of internal flash memory	Fig. 10. M37902FGMHP : block configuration of internal flash memory
★ ———	M37902FHMHP : block configuration of internal flash memory	(Deleted)
	M37902FJMHP : block configuration of internal flash memory	(Deleted)

Corrections and Supplementary Explanation for M37902FxM Datasheet (REV.B) NO.4

<table>
<tr><th>Page</th><th>Error</th><th>Correction</th></tr>
<tr><td>★ Page 15
DC Electrical Characteristics; AC Electrical Characteristics</td><td>(Vcc = 3.3 V ± 0.3 V, Ta = 0 to 60 °C, f(fsys) = 26 MHz (Note))</td><td>(Vcc = 3.3 V ± 0.3 V, Ta = 0 to 60 °C, f(fsys) = 20 MHz (Note))</td></tr>
<tr><td>★ Page 16,
ABSOLUTE MAXIMUM RATINGS</td><td>
<table>
<tr><th>Symbol</th><th>Parameter</th><th>Ratings</th><th>Unit</th></tr>
<tr><td>Pd</td><td>Power disspation</td><td>300</td><td>mW</td></tr>
<tr><td>Topr</td><td>Operating temperature</td><td></td><td></td></tr>
</table>
</td><td>
<table>
<tr><th>Symbol</th><th>Parameter</th><th>Ratings</th><th>Unit</th></tr>
<tr><td>Pd</td><td>Power disspation</td><td>400</td><td>mW</td></tr>
<tr><td>Topr</td><td>Operating ambient temperature</td><td></td><td></td></tr>
</table>
</td></tr>
<tr><td>★ Page 16,
RECOMMENDED OPERATING CONDITIONS</td><td>
<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="3">Limits</th></tr>
<tr><th></th><th></th><th>Max.</th><th>Typ.</th><th>Min.</th></tr>
<tr><td>f(XIN)</td><td>External clcok input frequency (Note 2)</td><td></td><td></td><td>26</td></tr>
<tr><td>f(sys)</td><td>System clcok frequency</td><td></td><td></td><td>26</td></tr>
</table>
2: ••••••••, be sure that f(fsys) = 26 MHz or less.
</td><td>
<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="3">Limits</th></tr>
<tr><th></th><th></th><th>Max.</th><th>Typ.</th><th>Min.</th></tr>
<tr><td>f(XIN)</td><td>External clcok input frequency (Note 2)</td><td></td><td></td><td>20</td></tr>
<tr><td>f(fsys)</td><td>System clcok frequency</td><td></td><td></td><td>20</td></tr>
</table>
2: ••••••••, be sure that f(fsys) = 20 MHz or less.
</td></tr>
<tr><td>★ Page 17,
DC ELECTRICAL CHARACTERISTICS</td><td>★ (Vcc = 3.3 V, Vss = 0 V, •••••• f(fsys) = 26 MHz (Note))
★
<table>
<tr><th>Symbol</th><th>Test conditions</th><th colspan="3">Limits</th></tr>
<tr><th></th><th></th><th>Min.</th><th>Typ.</th><th>Max.</th></tr>
<tr><td>ICC</td><td>f(fsys) = 26MHz, CPU operates.</td><td></td><td>15.6</td><td>31.2</td></tr>
</table>
<table>
<tr><td>Icc</td><td>••••••••</td><td>••••••••</td><td></td><td></td><td>—</td><td>µA</td></tr>
<tr><td></td><td></td><td>Ta = 25 °C ••••••••</td><td></td><td></td><td>—</td><td></td></tr>
<tr><td></td><td></td><td>Ta = 85 °C ••••••••</td><td></td><td></td><td>—</td><td></td></tr>
</table>
</td><td>(Vcc = 3.3 V, Vss = 0 V, •••••• f(fsys) = 20 MHz (Note))
<table>
<tr><th>Symbol</th><th>Test conditions</th><th colspan="3">Limits</th></tr>
<tr><th></th><th></th><th>Min.</th><th>Typ.</th><th>Max.</th></tr>
<tr><td>ICC</td><td>f(fsys) = 20MHz, CPU operates.</td><td></td><td>12</td><td>24</td></tr>
</table>
<table>
<tr><td>Icc</td><td>••••••••</td><td>••••••••</td><td></td><td></td><td>1</td><td>µA</td></tr>
<tr><td></td><td></td><td>Ta = 25 °C ••••••••</td><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td>Ta = 85 °C ••••••••</td><td></td><td></td><td>20</td><td></td></tr>
</table>
</td></tr>
<tr><td>★ Page 18,
A-D CONVERTER CHARACTERISTICS; the minium value of tCONV</td><td>
<table>
<tr><th>Symbol</th><th>Test conditions</th><th colspan="2">Limits</th></tr>
<tr><th></th><th></th><th>Min.</th><th>Max.</th></tr>
<tr><td>tCONV</td><td>f(fsys) ≤ 26MHz</td><td>••••••••</td><td>4.54</td><td></td></tr>
<tr><td></td><td></td><td>••••••••</td><td>1.89 (Note)</td><td></td></tr>
</table>
</td><td>
<table>
<tr><th>Symbol</th><th>Test conditions</th><th colspan="2">Limits</th></tr>
<tr><th></th><th></th><th>Min.</th><th>Max.</th></tr>
<tr><td>tCONV</td><td>f(fsys) ≤ 20MHz</td><td>••••••••</td><td>5.90</td><td></td></tr>
<tr><td></td><td></td><td>••••••••</td><td>2.45 (Note)</td><td></td></tr>
</table>
</td></tr>
<tr><td>Page 19
PERIPHERAL DEVICE INPUT/OUTPUT TIMING</td><td>(Vcc = 3.3 V ± 0.3 V, •••••• f(fsys) = 26 MHz, unless othre-wise noted)
✻ •••••• at f(fsys) = 26 MHz are shown in ( ).</td><td>(Vcc = 3.3 V ± 0.3 V, •••••• f(fsys) = 20 MHz, unless othre-wise noted)
✻ •••••• at f(fsys) = 20 MHz are shown in ( ).</td></tr>
</table>

Corrections and Supplementary Explanation for M37902FxM Datasheet (REV.B) NO.5

Page	Error	Correction
★ Page 19, Timer A input; (Gating input in timer mode)	Symbol / Parameter / Limits (Min., Max.) $t_{c(TA)}$ •••••••• f(f_{sys}) ≤ 26MHz Min. $\frac{16\times10^9}{f(f_{sys})}$ (615) $t_{w(TAH)}$ •••••••• f(f_{sys}) ≤ 26MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (307) $t_{w(TAL)}$ •••••••• f(f_{sys}) ≤ 26MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (307) **Note:** •••••• the count source = f_2 at f(f_{sys}) ≤ 26 MHz.	Symbol / Parameter / Limits (Min., Max.) $t_{c(TA)}$ •••••••• f(f_{sys}) ≤ 20MHz Min. $\frac{16\times10^9}{f(f_{sys})}$ (800) $t_{w(TAH)}$ •••••••• f(f_{sys}) ≤ 20MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (400) $t_{w(TAL)}$ •••••••• f(f_{sys}) ≤ 20MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (400) **Note:** •••••• the count source = f_2 at f(f_{sys}) ≤ 20 MHz.
★ Page 19, Timer A input; (External trigger input in one-shot pulse mode)	Symbol / Parameter / Limits (Min., Max.) $t_{c(TA)}$ •••••••• f(f_{sys}) ≤ 26MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (307)	Symbol / Parameter / Limits (Min., Max.) $t_{c(TA)}$ •••••••• f(f_{sys}) ≤ 20MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (400)
★ Page 21, Timer B input; (Pulse period measurement mode), (Pulse width measurement mode)	Symbol / Parameter / Limits (Min., Max.) $t_{c(TB)}$ •••••••• f(f_{sys}) ≤ 26MHz Min. $\frac{16\times10^9}{f(f_{sys})}$ (615) $t_{w(TBH)}$ •••••••• f(f_{sys}) ≤ 26MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (307) $t_{w(TBL)}$ •••••••• f(f_{sys}) ≤ 26MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (307) **Note:** •••••• the count source = f_2 at f(f_{sys}) ≤ 26 MHz.	Symbol / Parameter / Limits (Min., Max.) $t_{c(TB)}$ •••••••• f(f_{sys}) ≤ 20MHz Min. $\frac{16\times10^9}{f(f_{sys})}$ (800) $t_{w(TBH)}$ •••••••• f(f_{sys}) ≤ 20MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (400) $t_{w(TBL)}$ •••••••• f(f_{sys}) ≤ 20MHz Min. $\frac{8\times10^9}{f(f_{sys})}$ (400) **Note:** •••••• the count source = f_2 at f(f_{sys}) ≤ 20 MHz.
★ Page 23, READY, HOLD TIMING; Timing requirements, Switching characteristics ★ Pages 25,26,27, External bus timing; (Timing requirements), (Switching characteristics)	(Vcc = 3.3 V ± 0.3 V, •••••• f(f_{sys}) = 26 MHz, unless otherwise noted)	(Vcc = 3.3 V ± 0.3 V, •••••• f(f_{sys}) = 20 MHz, unless otherwise noted)
★ Page 26, External bus timing; (Timing requirements)	Symbol / Parameter / Limits (Min., Max.) $t_{c(in)}$ External clock •••••••• Min. 38	Symbol / Parameter / Limits (Min., Max.) $t_{c(in)}$ External clock •••••••• Min. 50