SONY

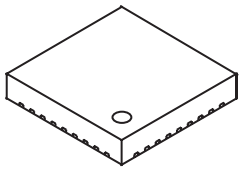
CXM3502ER

High Power 6 × 5 Antenna Switch MMIC for PDC Full Packet

Description

The CXM3502ER is a high power antenna switch MMIC for PDC full packet handsets. There are two modes which are TDMA mode and Packet mode. The CXM3502ER is suited to connect Tx/Rx/Duplexer to one of 4 antennas. The CXM3502ER has a CMOS decoder for RF switch control. The Sony Junction-gate PHEMT (JPHEMT) process is used for low insertion loss and low voltage operation.

36 pin VQFN (Plastic)



Features

- Low insertion loss
- Low loss bypass mode in TDMA
- High linearity: Harmonic < –60dBc
- CMOS compatible input control
- Small package: 36-pin VQFN (4.3mm × 4.3mm)

Applications

6 × 5 antenna switch for digital cellular such as PDC full packet handsets

Structure

GaAs junction-gate PHEMT

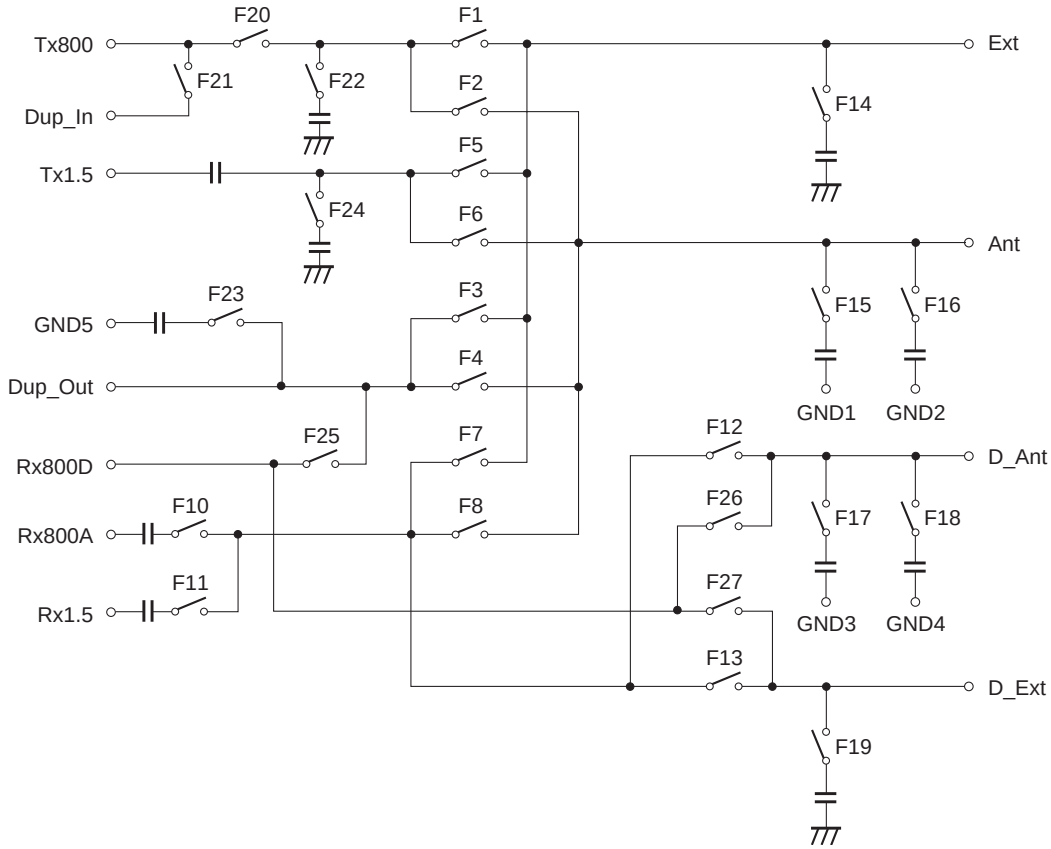
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operating temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

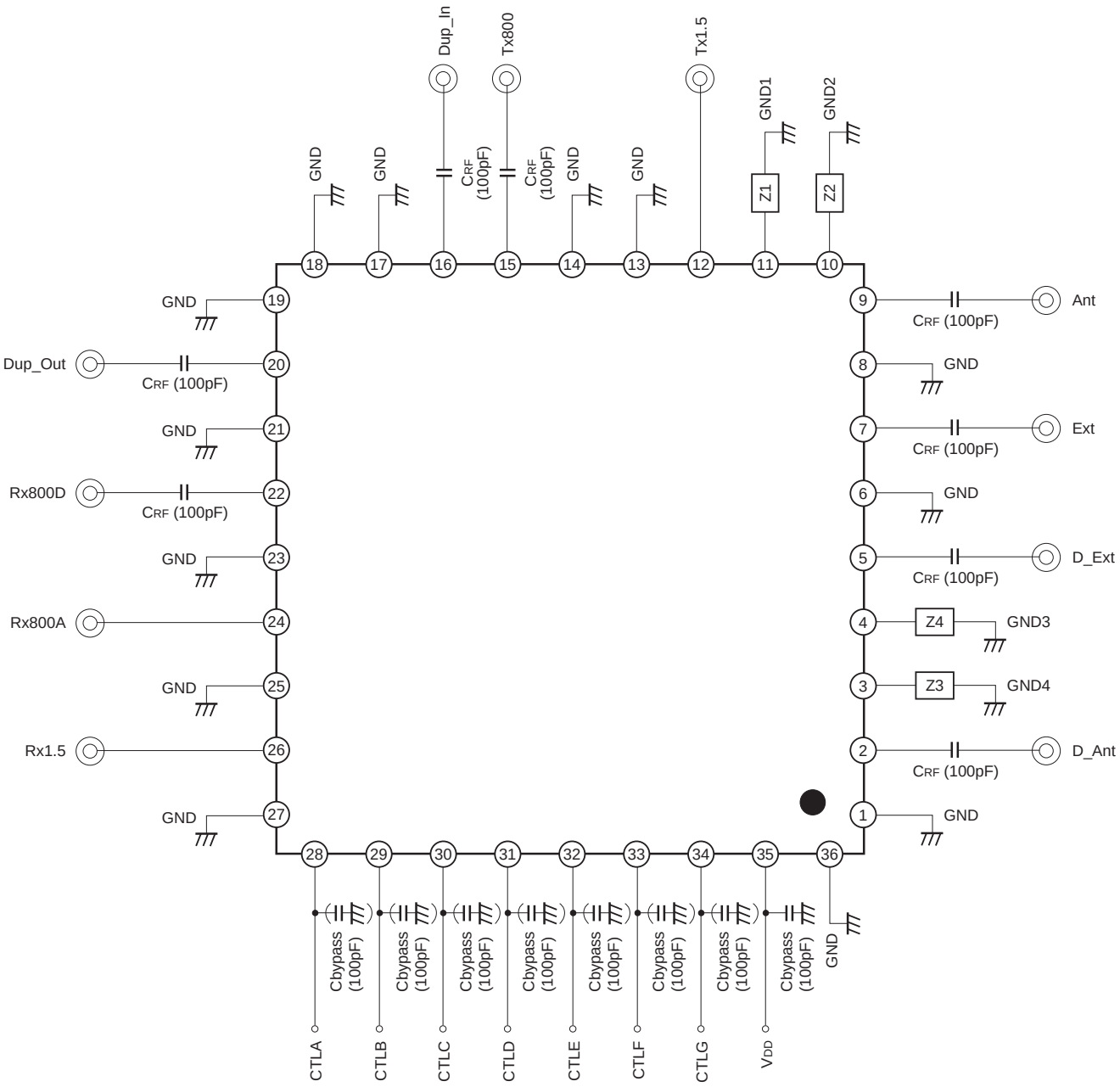
GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.
The actual ESD test data will be available later.

E03205-PS

Block Diagram



Pin Configuration and Recommended Circuit



When using this IC, the following external components should be used:

CRF: This capacitor is used for RF de-coupling and must be used for all applications. 100pF is recommended.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

A: Rx/Tx
B: Main/diversity
C: External/antenna
D: 800MHz digital/800MHz analog
E: 800MHz/1.5GHz
F: TDMA/duplex

State	On Pass	A	B	C	D	E	F	G	F1	F2	F3	F4	F5	F6	F7	F8	F10	F11	F12	F13	F14	F15	F16	F17	F18	F19	F20	F21	F22	F23	F24	F25	F26	F27
1	Tx800 – Ext	H	–	L	–	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	H	L	L	H	H	L	L	L
2	Tx800 – Ant	H	–	H	–	L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H	H	L	L	H	H	L	L	L
3	Tx1.5 – Ext	H	–	L	–	H	–	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	H	H	L	L	L	L
4	Tx1.5 – Ant	H	–	H	–	H	–	H	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	H	H	L	L	H	H	L	L	L	L
5	Rx800D – Ext	L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	L	L	H	L	H	H	L	L
6	Rx800A – Ext	L	L	L	H	L	L	H	L	L	L	L	L	L	H	L	H	L	L	L	L	H	L	H	L	H	L	L	H	H	H	L	L	L
7	Rx1.5 – Ext	L	L	L	–	H	–	H	L	L	L	L	L	L	H	L	L	H	L	L	L	L	H	L	H	H	L	L	H	H	H	L	L	L
8	Rx800D – Ant	L	L	H	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	H	L	H	L	L	H	L	H	H	L	L
9	Rx800A – Ant	L	L	H	H	L	L	H	L	L	L	L	L	L	L	H	H	L	L	L	H	L	L	H	L	H	L	L	H	H	H	L	L	L
10	Rx1.5 – Ant	L	L	H	–	H	–	H	L	L	L	L	L	L	L	H	L	H	L	L	H	L	L	L	H	H	L	L	H	H	H	L	L	L
11	Rx800D – D_Ext	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	L	L	L	H	H	H	L	L	H
12	Rx800A – D_Ext	L	H	L	H	L	L	H	L	L	L	L	L	L	L	L	H	L	L	H	H	H	L	H	L	L	L	L	H	H	H	L	L	L
13	Rx1.5 – D_Ext	L	H	L	–	H	–	H	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H	L	H	L	L	L	H	H	H	L	L	L
14	Rx800D – D_Ant	L	H	H	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	L	L	H	L	L	H	H	H	L	H	L
15	Rx800A – D_Ant	L	H	H	H	L	L	H	L	L	L	L	L	L	L	L	H	L	H	L	H	H	L	L	L	H	L	L	H	H	H	L	L	L
16	Rx1.5 – D_Ant	L	H	H	–	H	–	H	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H	L	L	H	L	L	H	H	H	L	L	L
17	Tx800 – Dup_In Dup_Out – Ext Rx800D – Ext	–	L	L	L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H	L	H	H	L	H	H	L	L
18	Tx800 – Dup_In Dup_Out – Ant Rx800D – Ant	–	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	L
19	Tx800 – Dup_In Dup_Out – Ext Rx800D – D_Ext	–	H	L	L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	H	H	L	H	L	L	H
20	Tx800 – Dup_In Dup_Out – Ant Rx800D – D_Ant	–	H	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	H	L

DC Bias Condition

(Ta = 25°C)

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	+2.7	+3.0	+3.3	V
Vctl (H)	V_{DD} – 0.2		V_{DD} + 0.2	V
Vctl (L)	0		0.5	V

Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	State	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	1	Tx800 – Ext	940MHz		0.55	0.85	dB
		2	Tx800 – Ant	940MHz		0.55	0.85	dB
		3	Tx1.5 – Ext	1.44GHz		0.50	0.80	dB
		4	Tx1.5 – Ant	1.44GHz		0.50	0.80	dB
		5	Rx800D – Ext	850MHz		0.65	0.95	dB
		6	Rx800A – Ext	850MHz		0.80	1.10	dB
		7	Rx1.5 – Ext	1.49GHz		1.00	1.30	dB
		8	Rx800D – Ant	850MHz		0.65	0.95	dB
		9	Rx800A – Ant	850MHz		0.80	1.10	dB
		10	Rx1.5 – Ant	1.49GHz		0.95	1.25	dB
		11	Rx800D – D_Ext	850MHz		0.55	0.85	dB
		12	Rx800A – D_Ext	850MHz		0.80	1.10	dB
		13	Rx1.5 – D_Ext	1.49GHz		0.95	1.25	dB
		14	Rx800D – D_Ant	850MHz		0.60	0.90	dB
		15	Rx800A – D_Ant	850MHz		0.80	1.10	dB
		16	Rx1.5 – D_Ant	1.49GHz		0.95	1.25	dB
		17, 18, 19, 20	Tx800 – Dup_In	940MHz		0.20	0.50	dB
		17	Dup_Out – Ext/ Rx800D – Ext	940MHz 850MHz		0.50 0.65	0.80 0.95	dB
		18	Dup_Out – Ant/ Rx800D – Ant	940MHz 850MHz		0.50 0.65	0.80 0.95	dB
		19	Dup_Out – Ext/ Rx800D – D_Ext	940MHz 850MHz		0.50 0.60	0.80 0.90	dB
		20	Dup_Out – Ant/ Rx800D – D_Ant	940MHz 850MHz		0.50 0.60	0.80 0.90	dB

Item	Symbol	State	Port	Condition	Min.	Typ.	Max.	Unit
Isolation	ISO.	2	Tx800 – Ext	940MHz	25	39		dB
		1	Tx800 – Ant	940MHz	20	28		dB
		4	Tx1.5 – Ext	1.44GHz	25	37		dB
		3	Tx1.5 – Ant	1.44GHz	20	26		dB
		8	Rx800D – Ext	850MHz	25	36		dB
		9	Rx800A – Ext	850MHz	25	36		dB
		10	Rx1.5 – Ext	1.49GHz	25	35		dB
		5	Rx800D – Ant	850MHz	20	28		dB
		6	Rx800A – Ant	850MHz	20	29		dB
		7	Rx1.5 – Ant	1.49GHz	20	29		dB
		14	Rx800D – D_Ext	850MHz	25	32		dB
		15	Rx800A – D_Ext	850MHz	25	32		dB
		16	Rx1.5 – D_Ext	1.49GHz	20	28		dB
		11	Rx800D – D_Ant	850MHz	25	41		dB
		12	Rx800A – D_Ant	850MHz	25	37		dB
		13	Rx1.5 – D_Ant	1.49GHz	25	33		dB
		1 to 16	Tx800 – Dup_In	940MHz	15	21		dB
		18	Dup_In – Dup_Out Dup_Out – Ext/ Rx800D – Ext	940MHz 940MHz 850MHz	25 25 25	41 38 36		dB
		17	Dup_In – Dup_Out Dup_Out – Ant/ Rx800D – Ant	940MHz 940MHz 850MHz	25 20 20	41 28 28		dB
		20	Dup_In – Dup_Out Dup_Out – Ext/ Rx800D – D_Ext	940MHz 940MHz 850MHz	25 25 25	41 38 32		dB
		19	Dup_In – Dup_Out Dup_Out – Ant/ Rx800D – D_Ant	940MHz 940MHz 850MHz	25 20 25	41 28 41		dB

Item	Symbol	State	Port	Condition	Min.	Typ.	Max.	Unit
Harmonics	2fo	1	Tx800 – Ext	*5		–75	–60	dBc
		2	Tx800 – Ant	*5		–75	–60	dBc
		3	Tx1.5 – Ext	*6		–75	–60	dBc
		4	Tx1.5 – Ant	*6		–75	–60	dBc
		17, 18, 19, 20	Tx800 – Dup_In	*5		–80	–60	dBc
		17	Dup_Out – Ext	*5		–75	–60	dBc
		18	Dup_Out – Ant	*5		–75	–60	dBc
		19	Dup_Out – Ext	*5		–75	–60	dBc
		20	Dup_Out – Ant	*5		–75	–60	dBc
	3fo	1	Tx800 – Ext	*5		–70	–60	dBc
		2	Tx800 – Ant	*5		–70	–60	dBc
		3	Tx1.5 – Ext	*6		–70	–60	dBc
		4	Tx1.5 – Ant	*6		–70	–60	dBc
		17, 18, 19, 20	Tx800 – Dup_In	*5		–80	–60	dBc
		17	Dup_Out – Ext	*5		–70	–60	dBc
		18	Dup_Out – Ant	*5		–70	–60	dBc
		19	Dup_Out – Ext	*5		–70	–60	dBc
		20	Dup_Out – Ant	*5		–70	–60	dBc
ACP	±50kHz	1	Tx800 – Ext	*5		–68	–57	dBc
		2	Tx800 – Ant	*5		–68	–57	dBc
		3	Tx1.5 – Ext	*6		–68	–57	dBc
		4	Tx1.5 – Ant	*6		–68	–57	dBc
		17, 18, 19, 20	Tx800 – Dup_In	*5		–68	–57	dBc
		17	Dup_Out – Ext	*5		–68	–57	dBc
		18	Dup_Out – Ant	*5		–68	–57	dBc
		19	Dup_Out – Ext	*5		–68	–57	dBc
		20	Dup_Out – Ant	*5		–68	–57	dBc
	±100kHz	1	Tx800 – Ext	*5		–74	–65	dBc
		2	Tx800 – Ant	*5		–74	–65	dBc
		3	Tx1.5 – Ext	*6		–74	–65	dBc
		4	Tx1.5 – Ant	*6		–74	–65	dBc
		17, 18, 19, 20	Tx800 – Dup_In	*5		–74	–65	dBc
		17	Dup_Out – Ext	*5		–74	–65	dBc
		18	Dup_Out – Ant	*5		–74	–65	dBc
		19	Dup_Out – Ext	*5		–74	–65	dBc
		20	Dup_Out – Ant	*5		–74	–65	dBc

Item	Symbol	State	Port	Condition	Min.	Typ.	Max.	Unit
Switching speed	TSW					2	5	µs
Bias current	I_{DD}			V_{DD} = 3.0V		6	50	µA
Control current	Ictl			Vctl (H) = 3V		1	20	µA

*1 Pin = 29.5dBm, 0/3V control, V_{DD} = 3.0V, 940 to 958MHz

*2 Pin = 29.5dBm, 0/3V control, V_{DD} = 3.0V, 1,429 to 1,453MHz

*3 Pin = 7dBm, 0/3V control, V_{DD} = 3.0V, 810 to 885MHz

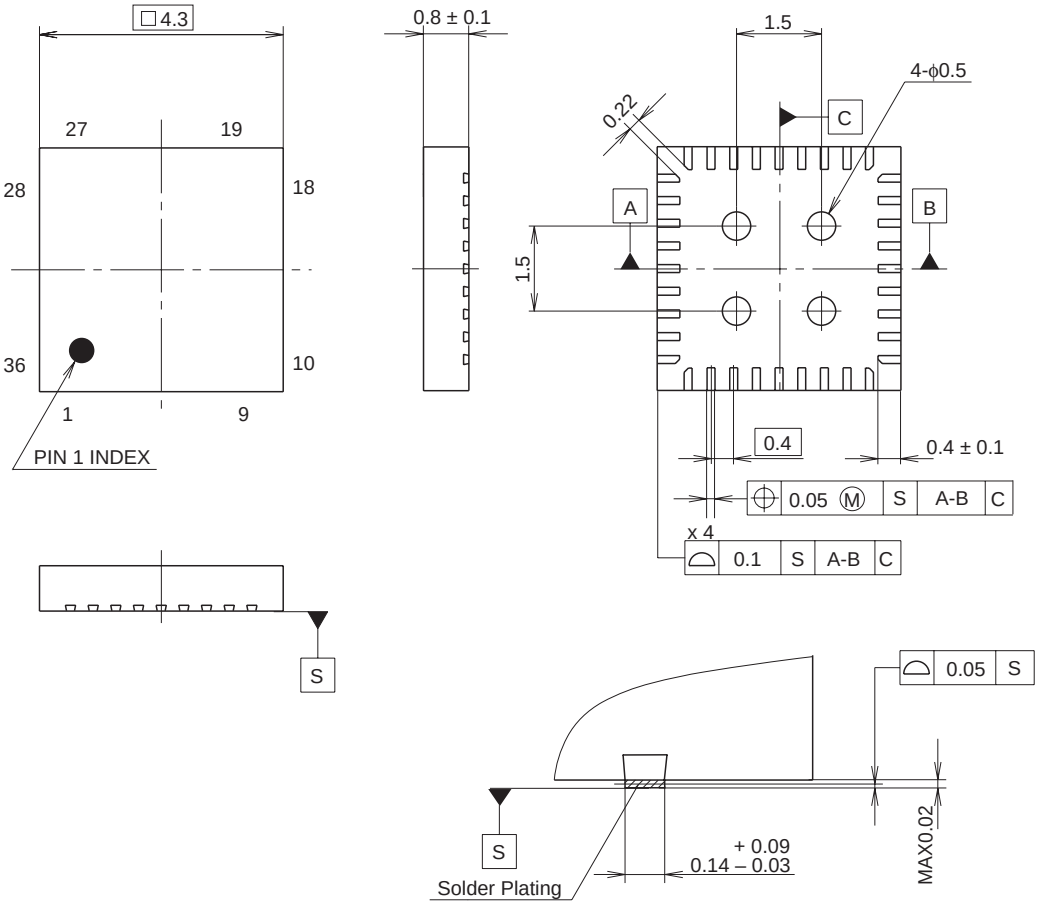
*4 Pin = 7dBm, 0/3V control, V_{DD} = 3.0V, 1,477 to 1,501MHz

*5 π/4-shifted DQPSK, Pin = 29.5dBm, 0/3V control, V_{DD} = 3.0V, 940 to 958MHz,
ACP (±50kHz) < – 65dBc, ACP (±100kHz) < – 75dBc, 2nd harmonics < – 65dBc, 3rd harmonics < – 65dBc

*6 π/4-shifted DQPSK, Pin = 29.5dBm, 0/3V control, V_{DD} = 3.0V, 1,429 to 1,453MHz,
ACP (±50kHz) < – 65dBc, ACP (±100kHz) < – 75dBc, 2nd harmonics < – 65dBc, 3rd harmonics < – 65dBc

Package Outline Unit: mm

36PIN VQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	VQFN-36P-02
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.04g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm