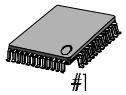
GENERAL DESCRIPTION

KS7214 is Timing control IC for generating timing signal & sync signal which required camera system using monochrome CCD Image sensor.

48 - QFP - 0707



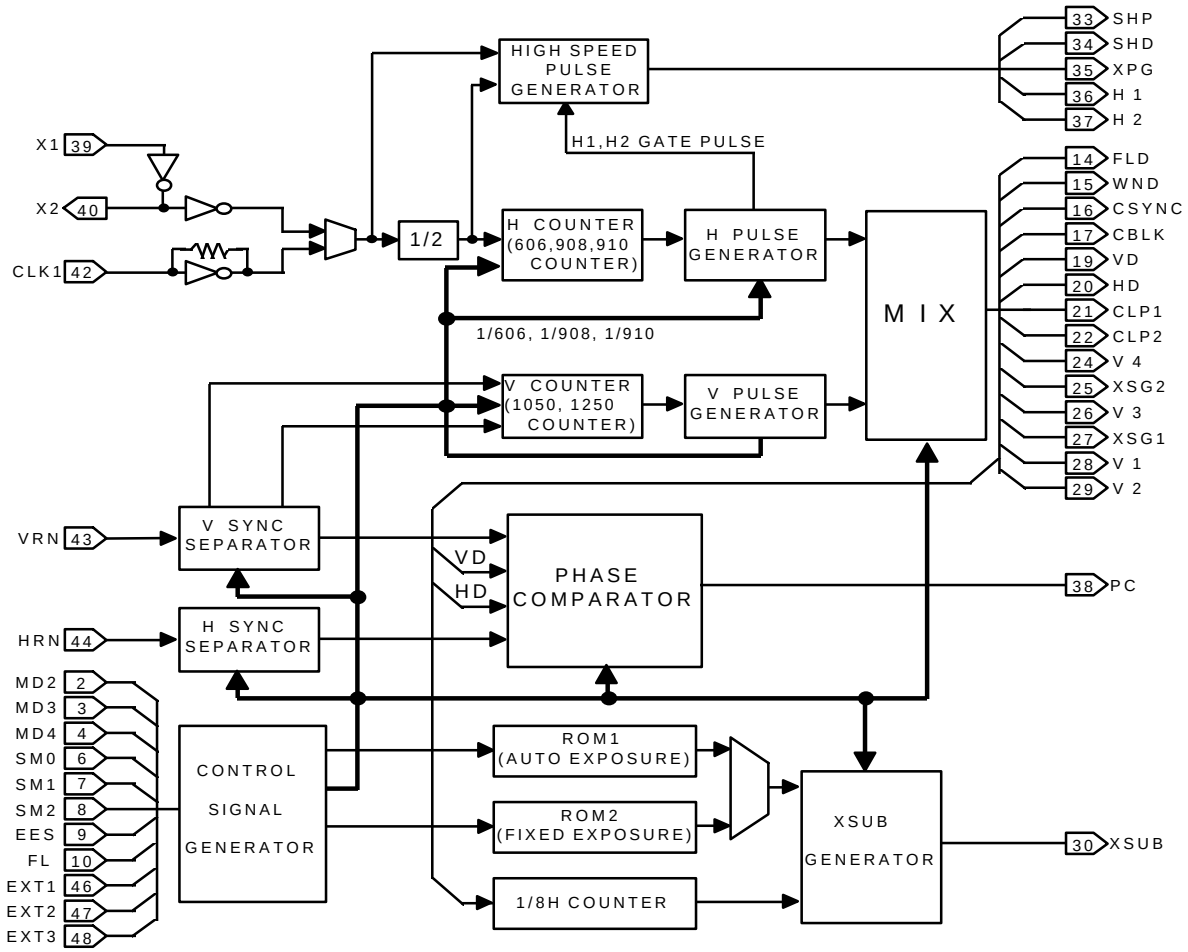
FUNCTIONS

- EIA / CCIR STANDARDS TIMING MODE
- HI-BAND / NORMAL TIMING MODE
- FRAME / FIELD ACCUMULATION MODE
- INTERLACE / NON - INTERLACE MODE
- EXTERNAL SYNCHRONIZATION MODE
- ELECTRONIC IRIS (ELECTRONIC SHUTTER)
- SYNC SIGNAL GENERATION
- OSCILLATION FREQUENCY :
  EIA NORMAL MODE : 19.06992 MHz
  CCIR NORMAL MODE : 18.93750 MHz
  EIA HI-BAND MODE : 28.63636 MHz
  CCIR HI-BAND MODE : 28.37500 MHz

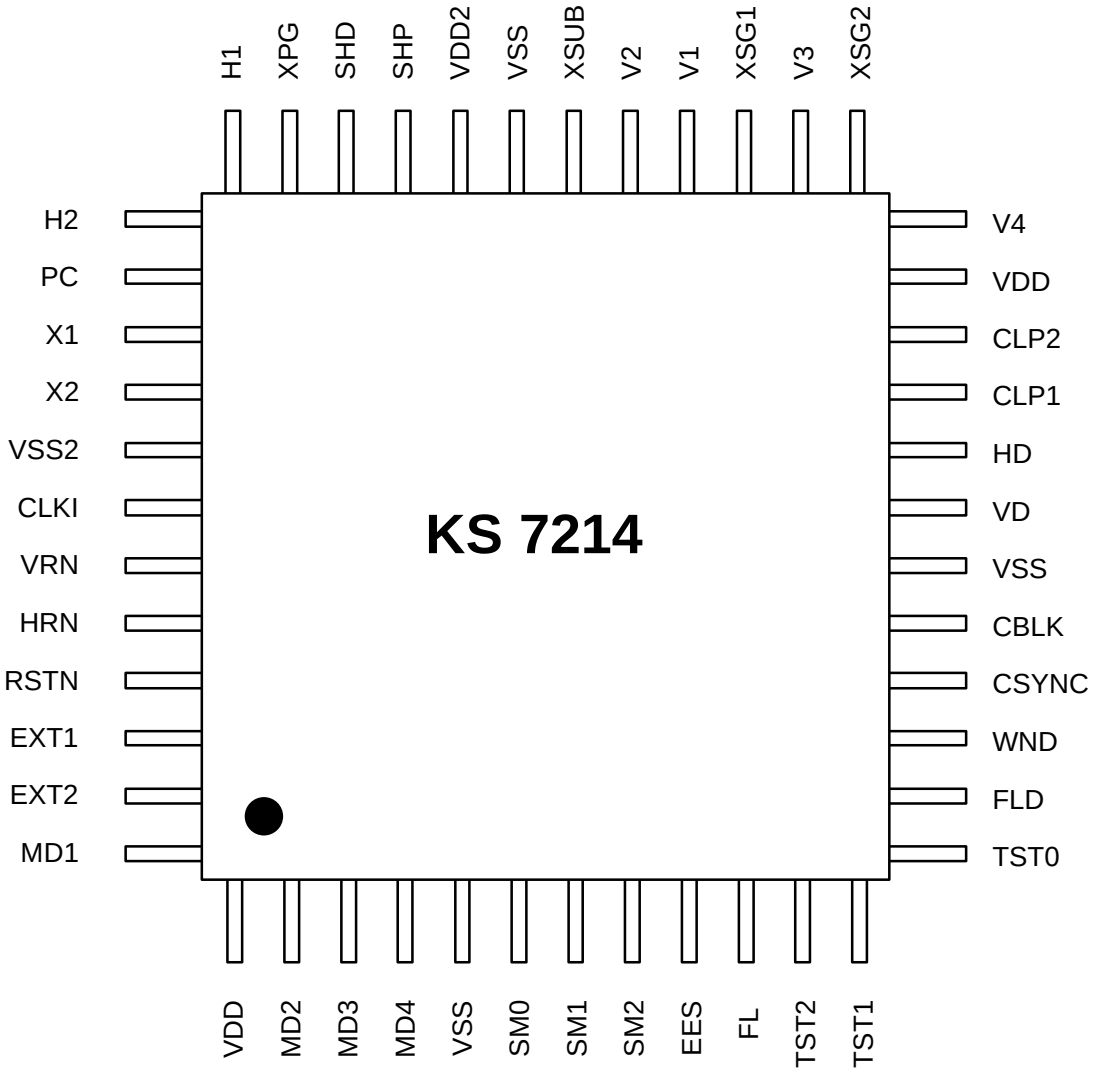
ORDERING INFORMATION

Device	Package	Operating Temperature
KS7214	48-QFP-0707	- 20°C ~ +75 °C

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Pin Description
1	VDD	-	Power Supply
2	MD2	I	Mode Switching; HI-Band: High, Normal: Low (with Pull-down)
3	MD3	I	Mode Switching; Non - Interlace: High, Interlace: Low (with Pull-down)
4	MD4	I	Mode Switching; Frame : High, Field: Low (with Pull-down)
5	VSS	-	Ground
6	SM0	I	Shutter Speed Control (with Pull-down)
7	SM1	I	Shutter Speed Control (with Pull-down)
8	SM2	I	Shutter Speed Control (with Pull-down)
9	EES	I	Electronic Shutter Mode; Auto Mode: High, Fixed Mode: Low (with Pull-down)
10	FL	I	Flickerless Shutter Mode; Flickerless Mode: High (with Pull-down)
11	TST2	I	Test Mode Select 2 (with Pull-down)
12	TST1	I	Test Mode Select 1 (with Pull-down)
13	TST0	I	Test Mode Select 0 (with Pull-down)
14	FLD	O	Field Seperation Pulse
15	WND	O	Window Pulse
16	CSYNC	O	Composite Sync Pulse
17	CBLK	O	Composite Blank Pulse
18	VSS	-	Ground
19	VD	O	Vertical Drive Pulse
20	HD	O	Horizontal Drive Pulse
21	CLP1	O	Clamp Pulse 1
22	CLP2	O	Clamp Pulse 2
23	VDD	-	Power Supply
24	V4	O	CCD Vertical Register Drive Pulse 4

PIN DESCRIPTION (Continued)

Pin No.	Pin Name	I/O	Pin Description
25	XSG2	O	CCD Sensor Read Out Pulse 2
26	V3	O	CCD Vertical Register Drive Pulse 3
27	XSG1	O	CCD Sensor Read Out Pulse 1
28	V1	O	CCD Vertical Register Drive Pulse 1
29	V2	O	CCD Vertical Register Drive Pulse 2
30	XSUB	O	CCD Discharge Pulse
31	VSS	-	Ground
32	VDD2	-	Power Supply 2
33	SHP	O	Precharge Sample & Hold Pulse
34	SHD	O	Data Sample & Hold Pulse
35	XPG	O	CCD Reset Gate Pulse
36	H1	O	CCD Horizontal Register Drive Pulse
37	H2	O	CCD Horizontal Register Drive Pulse
38	PC	O	Phase Comparator Output
39	X1	I	Oscillator Input
40	X2	O	Oscillator Output
41	VSS2	-	Ground 2
42	CLKI	I	Clock Input For EXT. Sync Mode
43	VRN	I	Vertical PLL Reference For External Sync Mode (Schmitt Pull-up)
44	HRN	I	Horizontal PLL Reference For External Sync Mode (Schmitt Pull-up)
45	RSTN	I	System Initialization Pulse (Schmitt Pull- up)
46	EXT1	I	External Sync Mode Select (with Pull-down)
47	EXT2	I	External Sync Mode Select (with Pull-down)
48	MD1	I	Mode Switching; CCIR: High, EIA: Low (with Pull-down)

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

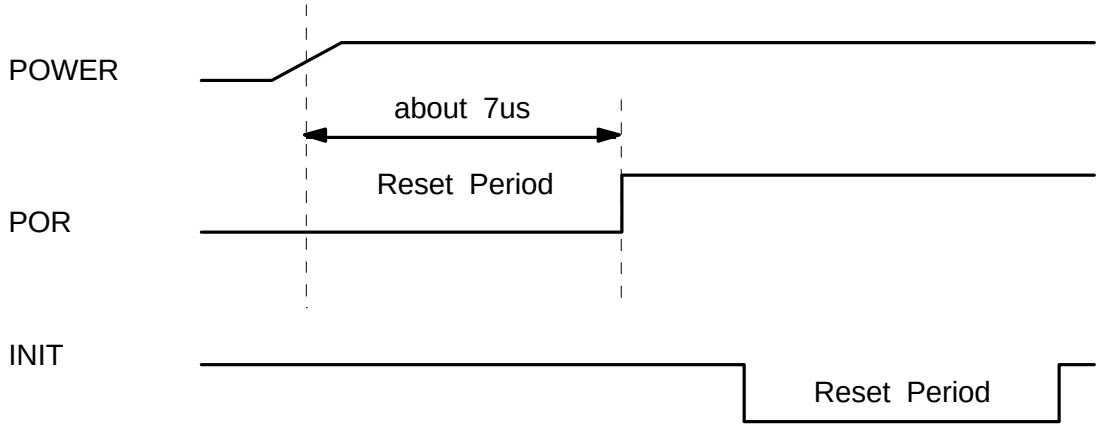
PARAMETER	SYMBOL	CONDITION	UNIT
SUPPLY VOLTAGE	VDD	VSS - 0.3 ~ + 7.0	V
INPUT VOLTAGE	VI	VSS - 0.3 ~ VDD + 0.3	V
OUTPUT VOLTAGE	VO	VSS - 0.3 ~ VDD + 0.3	V
OPERATING TEMP.	T_{opr}	0 ~ + 70	°C
STORAGE TEMP.	T_{str}	- 40 ~ + 125	°C
LATCH-UP CURRENT	I_{LU}	100	mA

DC CHARACTERISTICS (Ta = 25 °C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VDD	-	4.75	5.00	5.25	V
Input voltage1 (Normal input)	VIH 1	CMOS Level Interface	0.7VDD	-	-	V
	VIL 1	CMOS Level Interface	-	-	0.3VDD	V
Input voltage2 (Pin 43, 44, 45)	VIH2	CMOS Level schmmit trigger	0.8VDD	-	-	V
	VIL2	CMOS Level schmmit trigger	-	-	0.2VDD	V
Input Current 1(With pull-down)	IIH1	VI = VDD	50	-	200	uA
	IIL1	VI = VSS	-10	-	10	uA
Input Current 2	IIH2	VI = VDD	-10	-	10	uA
(With pull-up: Pin 43, 44, 45)	IIL2	VI = VSS	-200	-	-50	uA
Input Current 3	IIH3	VI = VDD	-40	-	40	uA
(Normal Input: Pin 42)	IIL3	VI = VSS	-40	-	40	uA
Output voltage 1(Normal output)	VOH1	IOH = -2mA	2.4	-	-	V
	VOL1	IOL = 2mA	-	-	0.4	V
Output voltage 2 (Pin 33, 34, 35)	VOH2	IOH = -4mA	2.4	-	-	V
	VOL2	IOL = 4mA	-	-	0.4	V
Output voltage 3 (Pin 36, 37)	VOH3	IOH = -16mA	2.4	-	-	V
	VOL3	IOL = 16mA	-	-	0.4	V
Output voltage 4 (Pin 40)	VOH4	IOH = -1mA	2.4	-	-	V
	VOL4	IOL = 1mA	-	-	0.4	V
Operating current	IDD	VDD = 5.25V	-	25	50	mA
Static current	I_{ST}	VDD = 5.25V	-	420	-	uA

OPERATION EXPLANATION

INTERNAL RESET OPERATION
* Including power on reset. (Typ. 7us)
* Rstn low active reset at the internal mode



EXTERNAL SYNCHRONIZATION OPERATION

EXT 1	EXT 2	MODE
0	0	Internal Sync. Mode
1	1	External Composite Sync. Mode
1	0	Line Lock Sync. Mode
1	1	Separate Sync. Mode

HD PHASE SELECTION

TST 2	TST 1	TST0	MODE
0	0	0	NORMAL HD
1	1	1	REVERSED HD
ELSE			REVERSED

ELECTRONIC SHUTTER

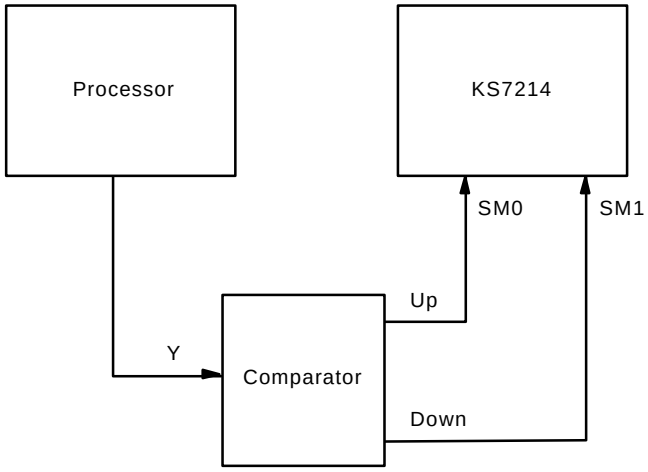
There are two electronic shutter modes in KS7214.
One is a Fixed Iris mode that controls shutter speed through parallel interface with external pin.
The other is a Auto Iris mode that controls electronic Iris automatically by detecting the light amount of current objects from the signal process IC.

FIXED SHUTTER MODE

MD1	FL	SM2	SM1	SM0	SHUTTER SPEEDB	
					STEP	REAL
L	L	L	L	L	1/60	1/60
L	L	L	L	H	1/250	1/251
L	L	L	H	L	1/500	1/513
L	L	L	H	H	1/1000	1/1006
L	L	H	L	L	1/2000	1/1936
L	L	H	L	H	1/5000	1/5034
L	L	H	H	L	1/10000	1/10489
L	L	H	H	H	1/30000	1/31469
L	H	X	X	X	1/100 *	1/101
H	L	L	L	L	1/50	1/50
H	L	L	L	H	1/250	1/249
H	L	L	H	L	1/500	1/510
H	L	L	H	H	1/1000	1/999
H	L	H	L	L	1/2000	1/1923
H	L	H	L	H	1/5000	1/5000
H	L	H	H	L	1/10000	1/10416
H	L	H	H	H	1/30000	1/31249
H	H	X	X	X	1/120 *	1/120

* FLICKERLESS MODE

AUTO SHUTTER MODE



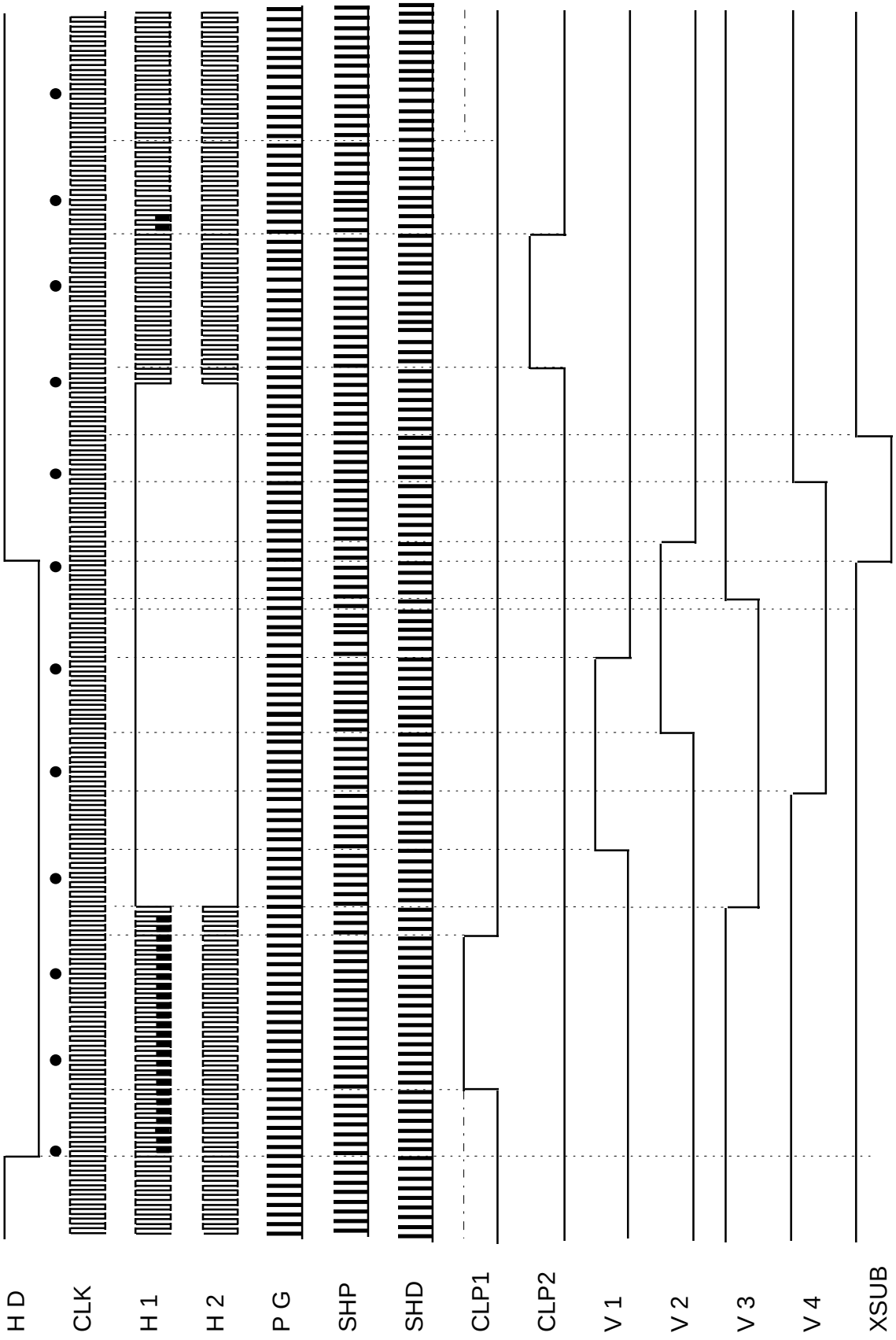
SM1	SM0	Auto Shutter Mode
0	0	Shutter Speed Hold
0	1	Shutter Speed UP
1	0	Shutter Speed DOWN
1	1	Shutter Speed Hold

< Auto shutter application >

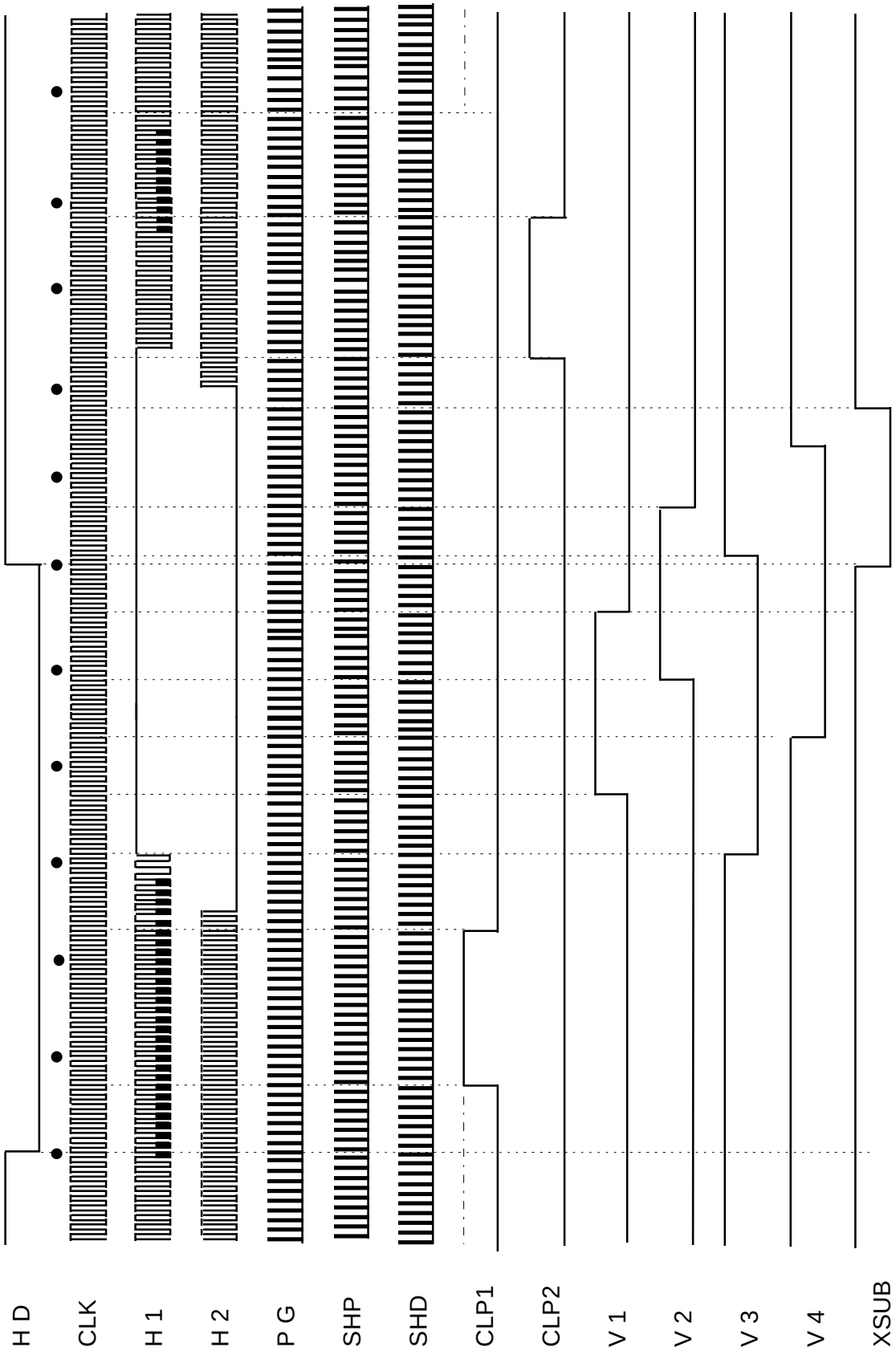
NO	Step Period	EIA		CCIR	
		Step	Shutter Speed	Step	Shutter Speed
1	7H	8	1/60 ~ 1/76	8	1 / 50 ~ 1 / 75
2	5H	7	1/77 ~ 1/91	7	1 / 76 ~ 1 / 91
3	4H	9	1/92 ~ 1/116	9	1 / 92 ~ 1 / 115
4	3H	12	1/117 ~ 1/157	12	1 / 116 ~ 1 / 156
5	2H	18	1/158 ~ 1/247	18	1 / 157 ~ 1 / 245
6	1H	50	1/248 ~ 1/1154	50	1 / 246 ~ 1 / 1146
7	1 / 2H	18	1/1155 ~ 1/3402	18	1 / 1147 ~ 1 / 3378
8	1 / 4H	12	1/3403 ~ 1/9682	12	1 / 3379 ~ 1 / 9615
9	1 / 8H	11	1/9683 ~ 1/125875	11	1/9616 ~ 1/124999

< Auto shutter speed table >

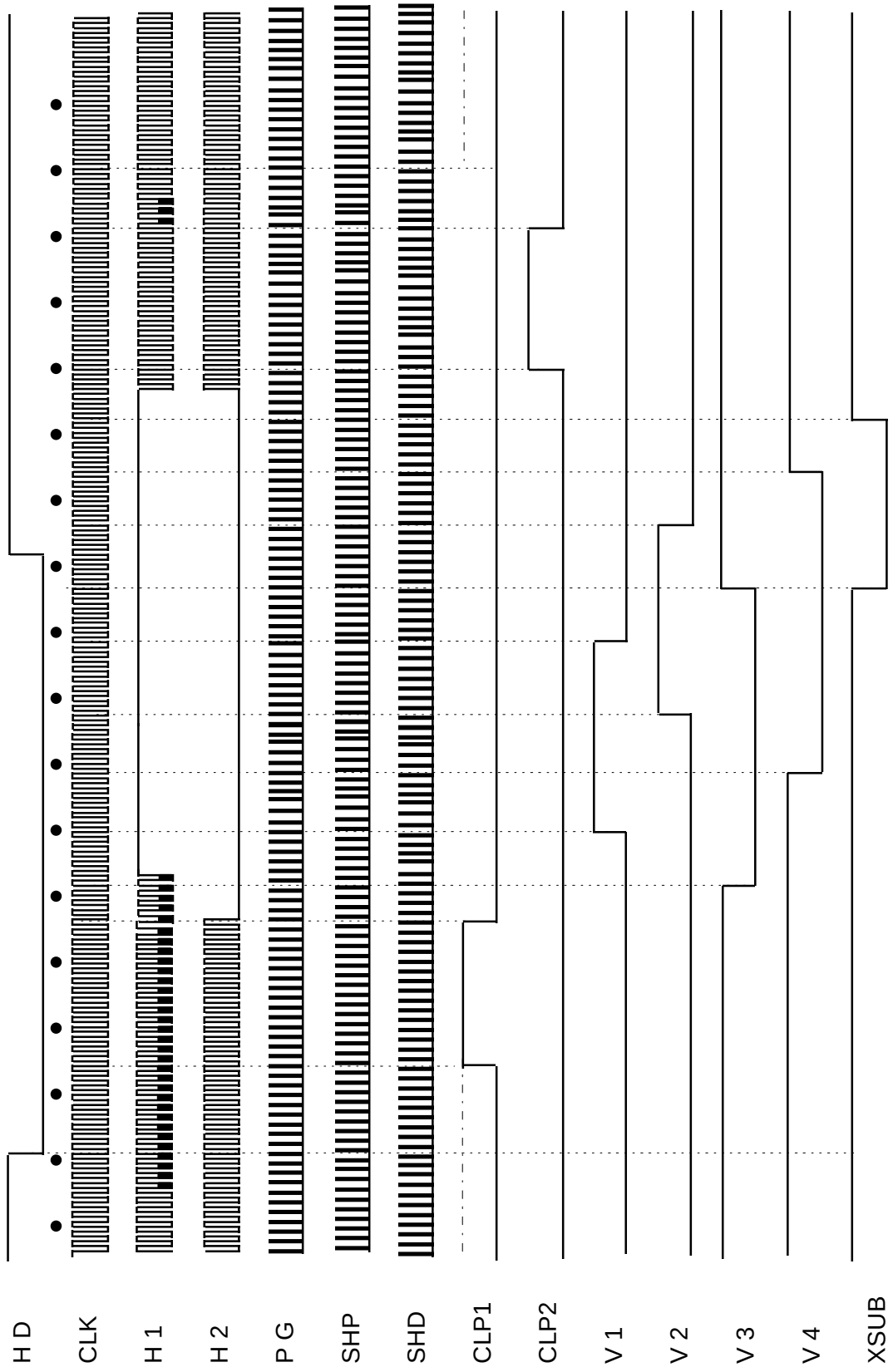
* HORIZONTAL TIMING CHART FOR EIA NORMAL



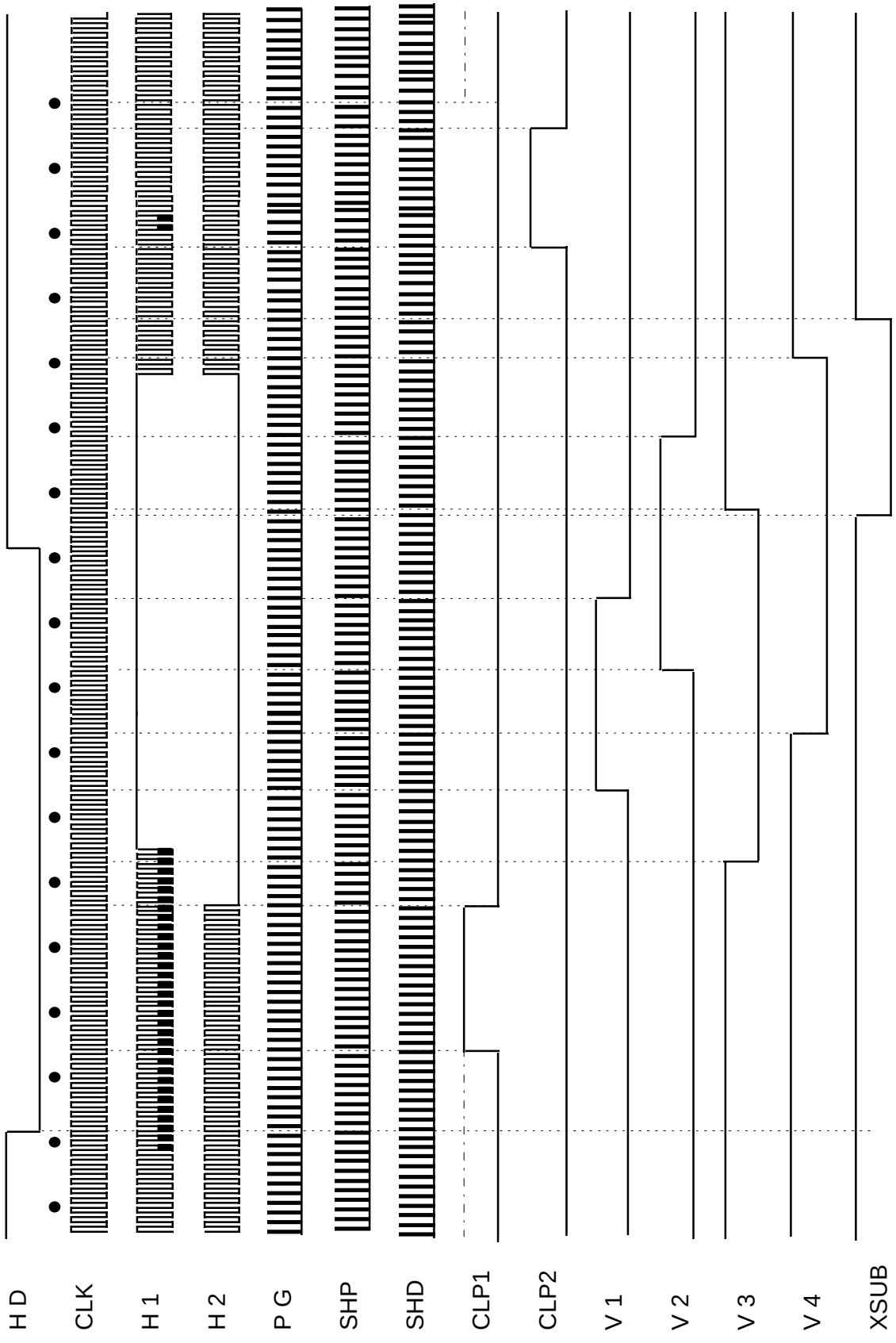
* HORIZONTAL TIMING CHART FOR CCIR NORMAL

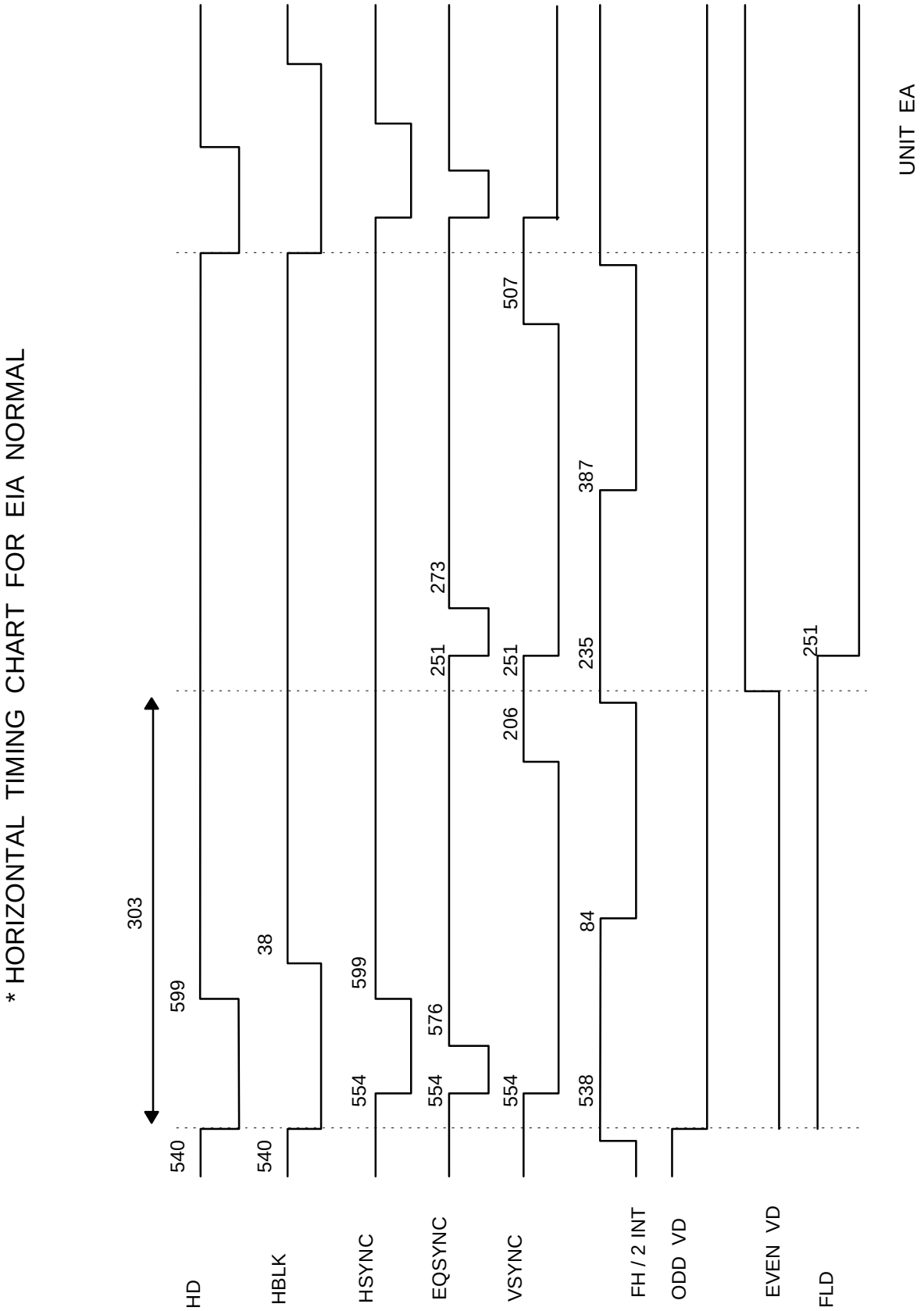


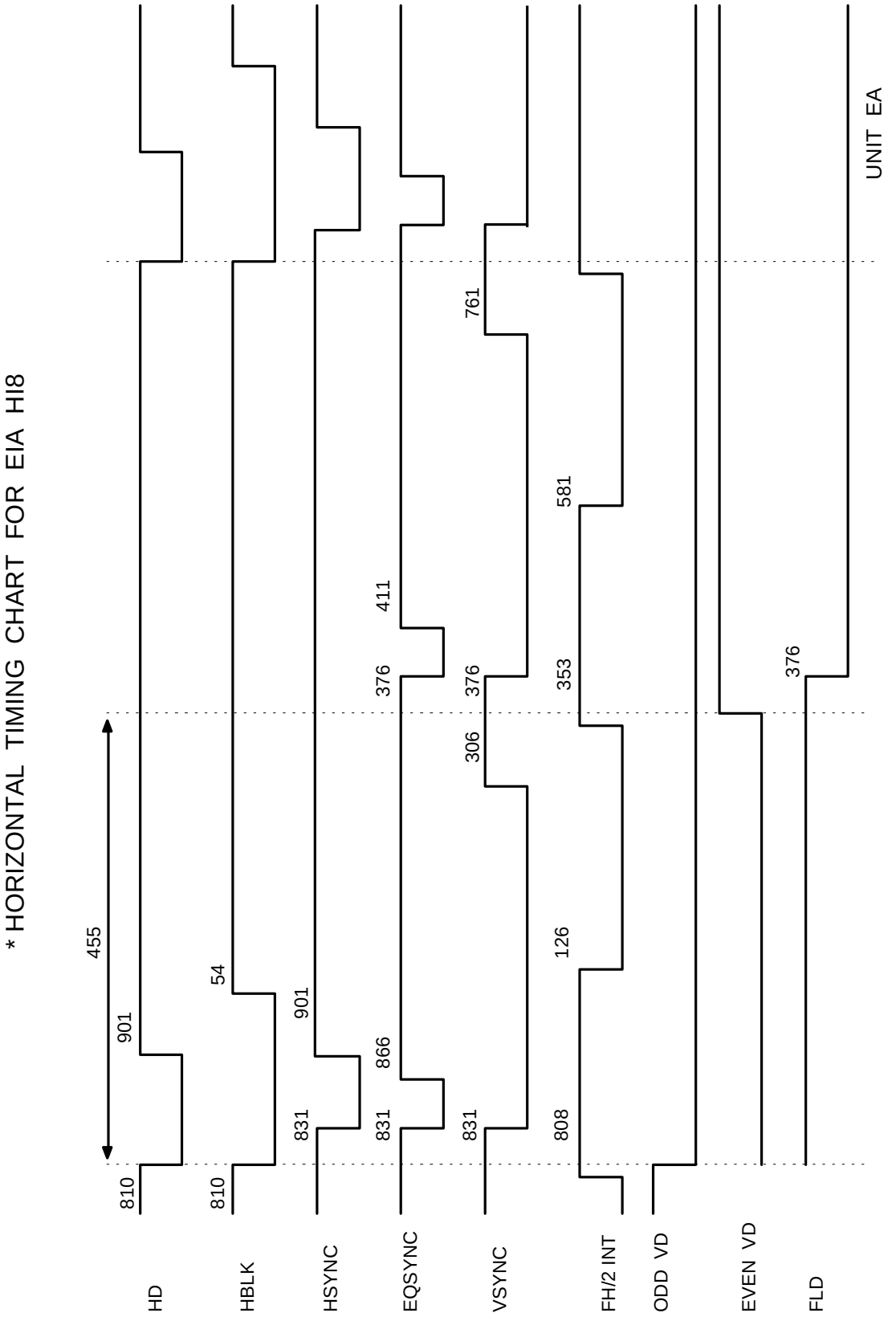
* HORIZONTAL TIMING CHART FOR EIA HI8

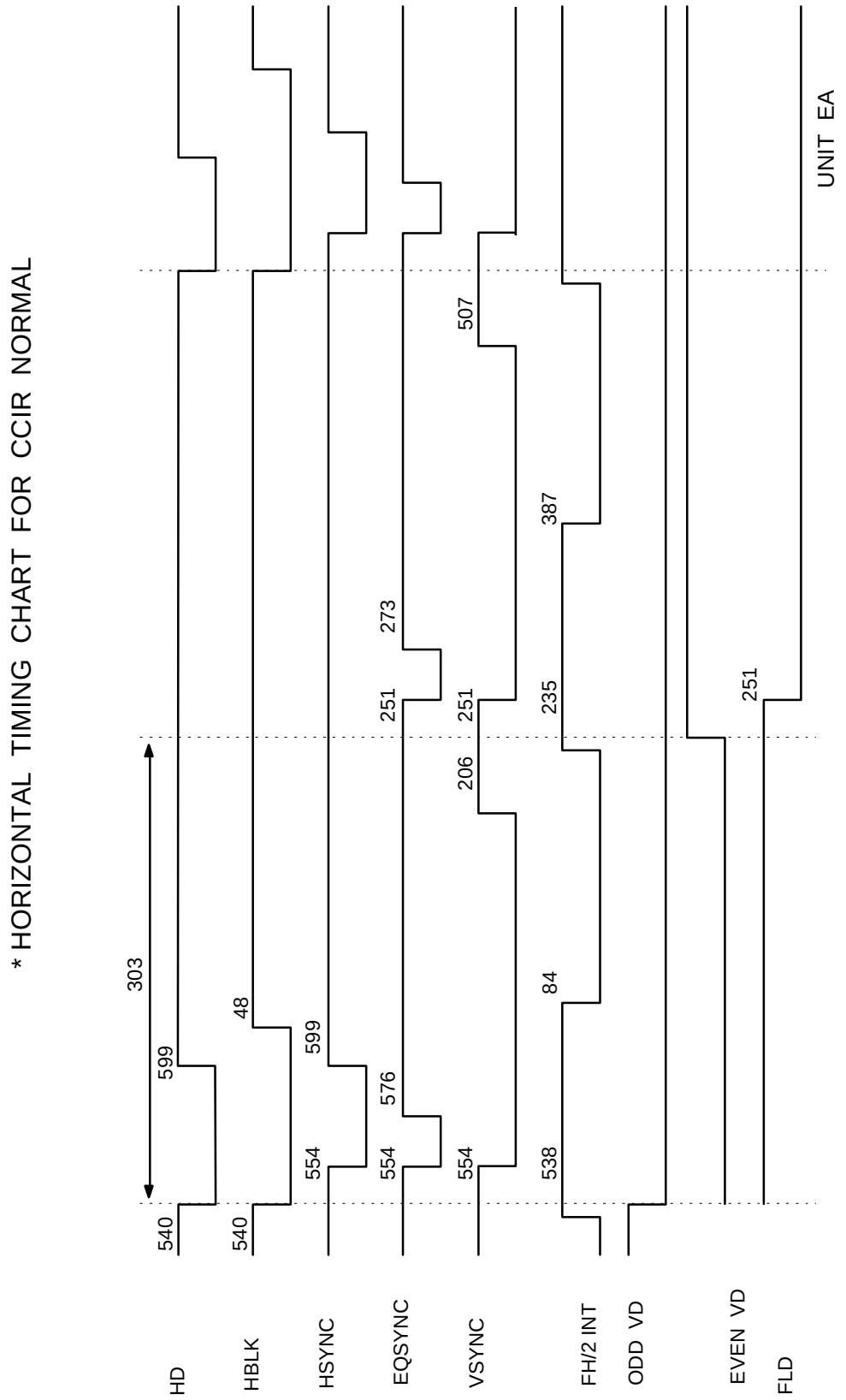


* HORIZONTAL TIMING CHART FOR CCIR HI8

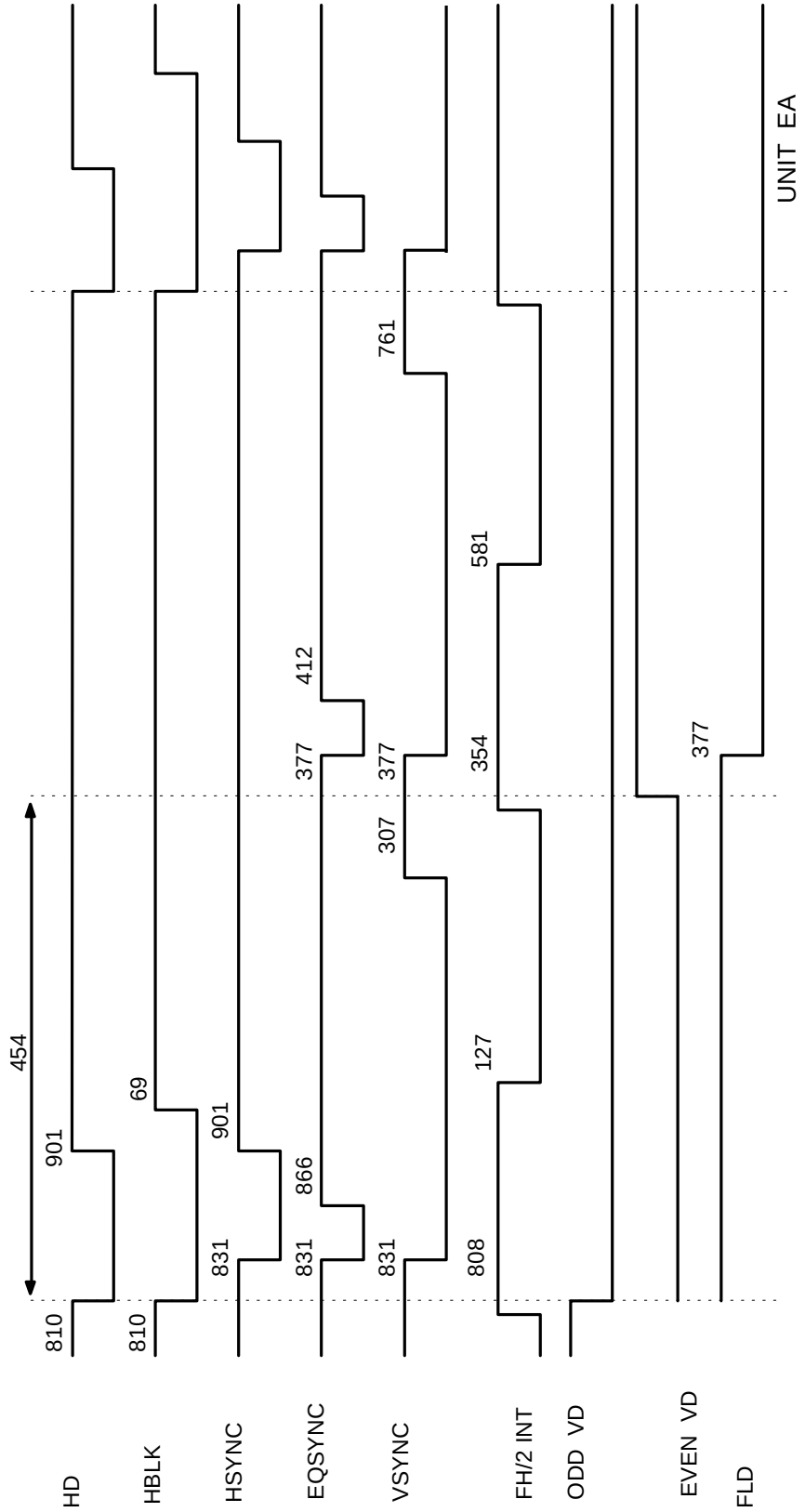



* HORIZONTAL TIMING CHART FOR EIA NORMAL
UNIT EA
HD
HBLK
HSYNC
EQSYNC
VSYNC
FH / 2 INT
ODD VD
EVEN VD
FLD
303
599
540
38
540
599
554
576
554
554
273
251
251
507
206
387
235
84
538
251

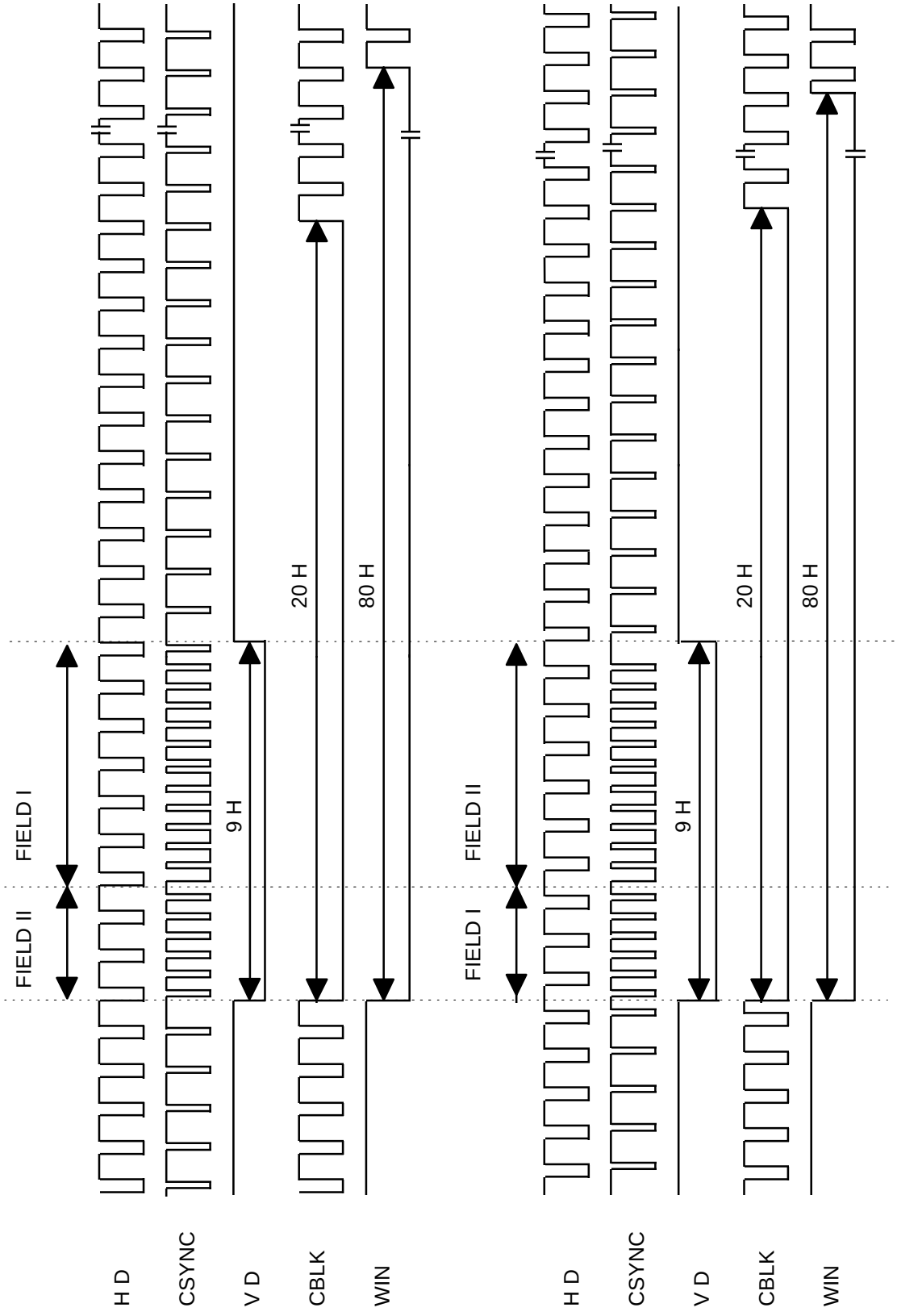

* HORIZONTAL TIMING CHART FOR EIA HI8
HD
HBLK
HSYNC
EQSYNC
VSYNC
FH/2 INT
ODD VD
EVEN VD
FLD
UNIT EA
455
901
810
54
810
901
831
411
866
376
831
761
376
306
831
581
353
126
808
376


* HORIZONTAL TIMING CHART FOR CCIR NORMAL
UNIT EA
HD
HBLK
HSYNC
EQSYNC
VSYNC
FH/2 INT
ODD VD
EVEN VD
FLD
303
599
540
48
540
599
554
554
576
273
554
251
206
251
507
84
538
387
235
251

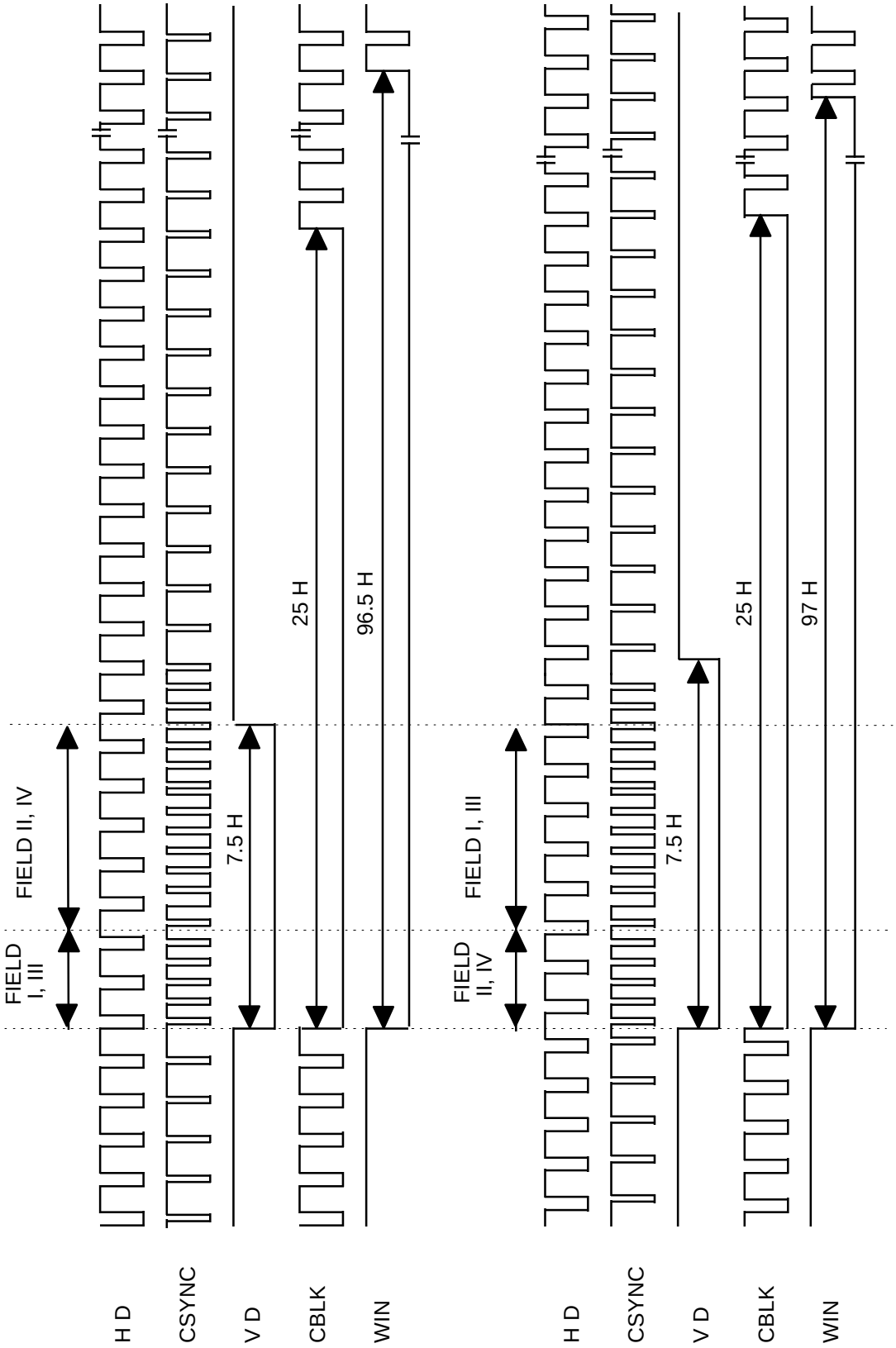
* HORIZONTAL TIMING CHART FOR CCIR HI8



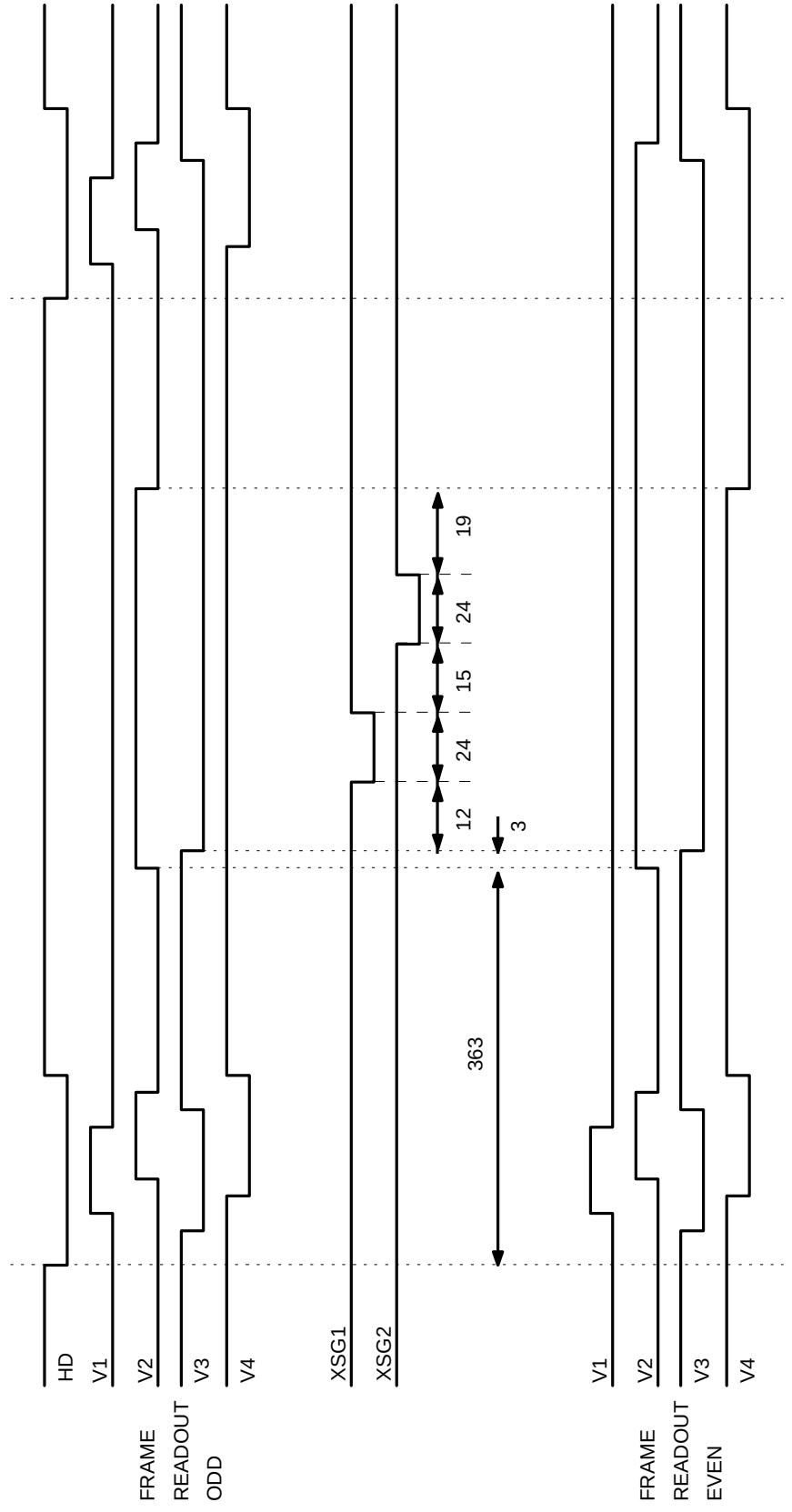
* VERTICAL TIMING CHART FOR EIA



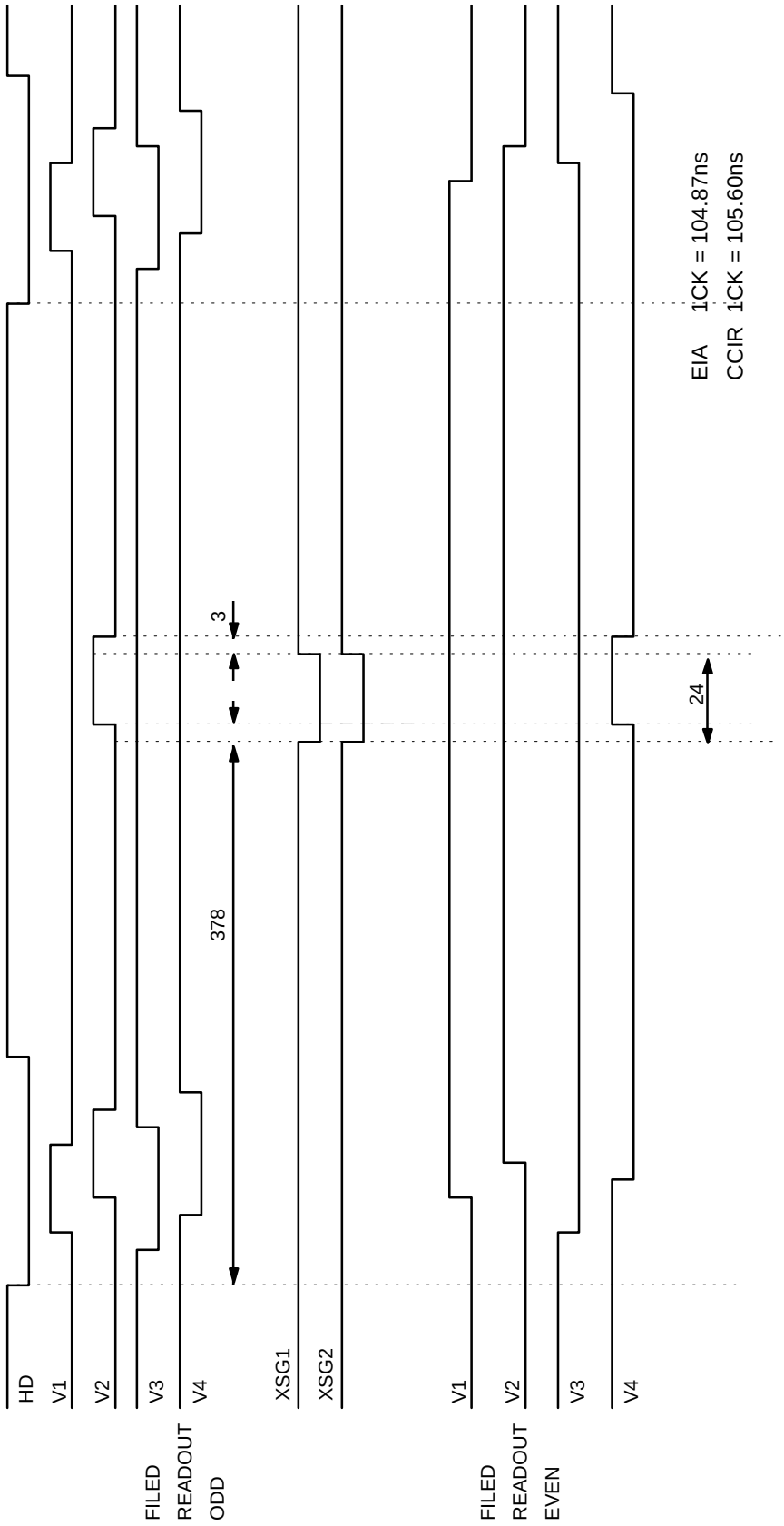
* VERTICAL TIMING CHART FOR CCIR



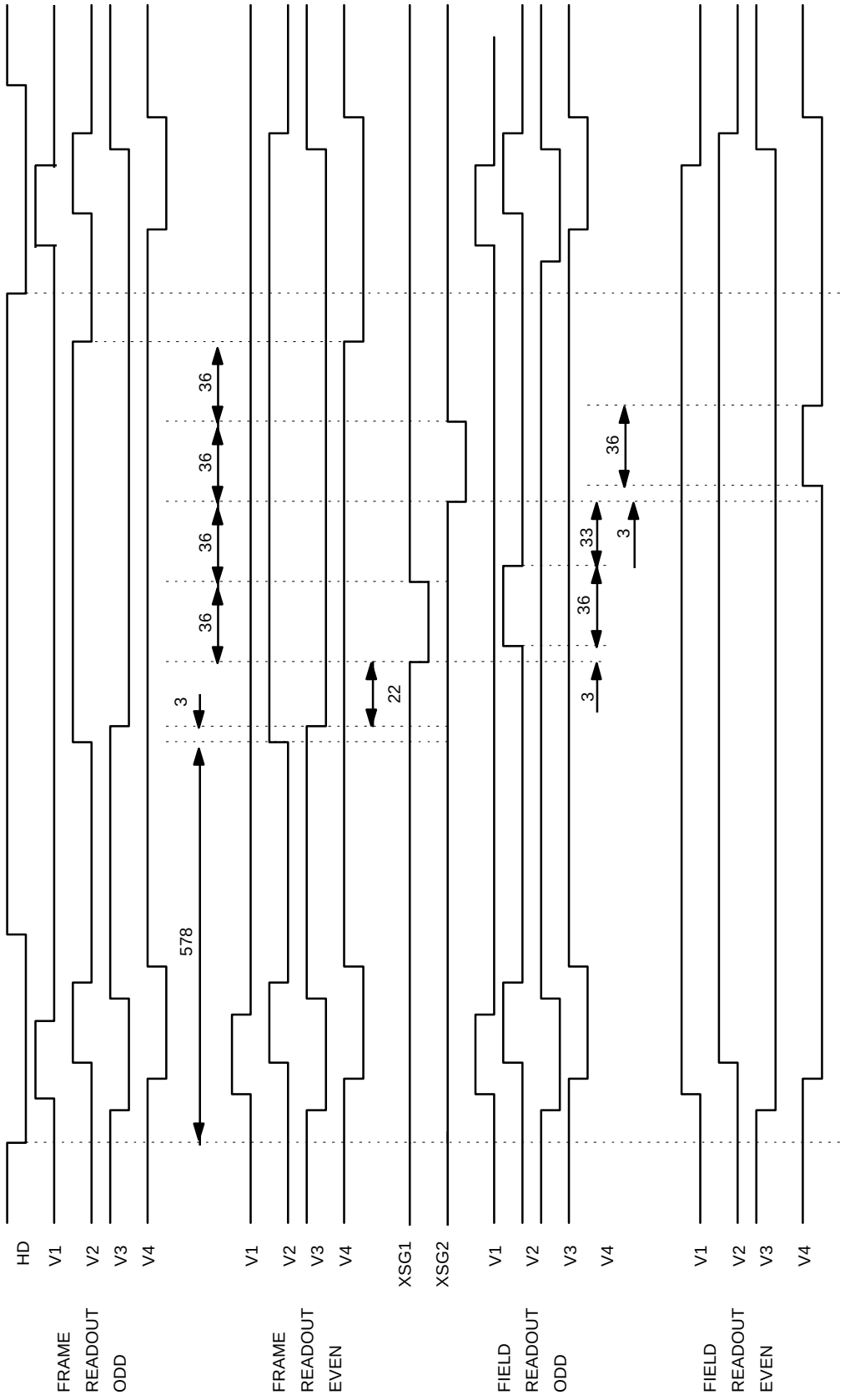
* VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR NORMAL EIA AND CCIR



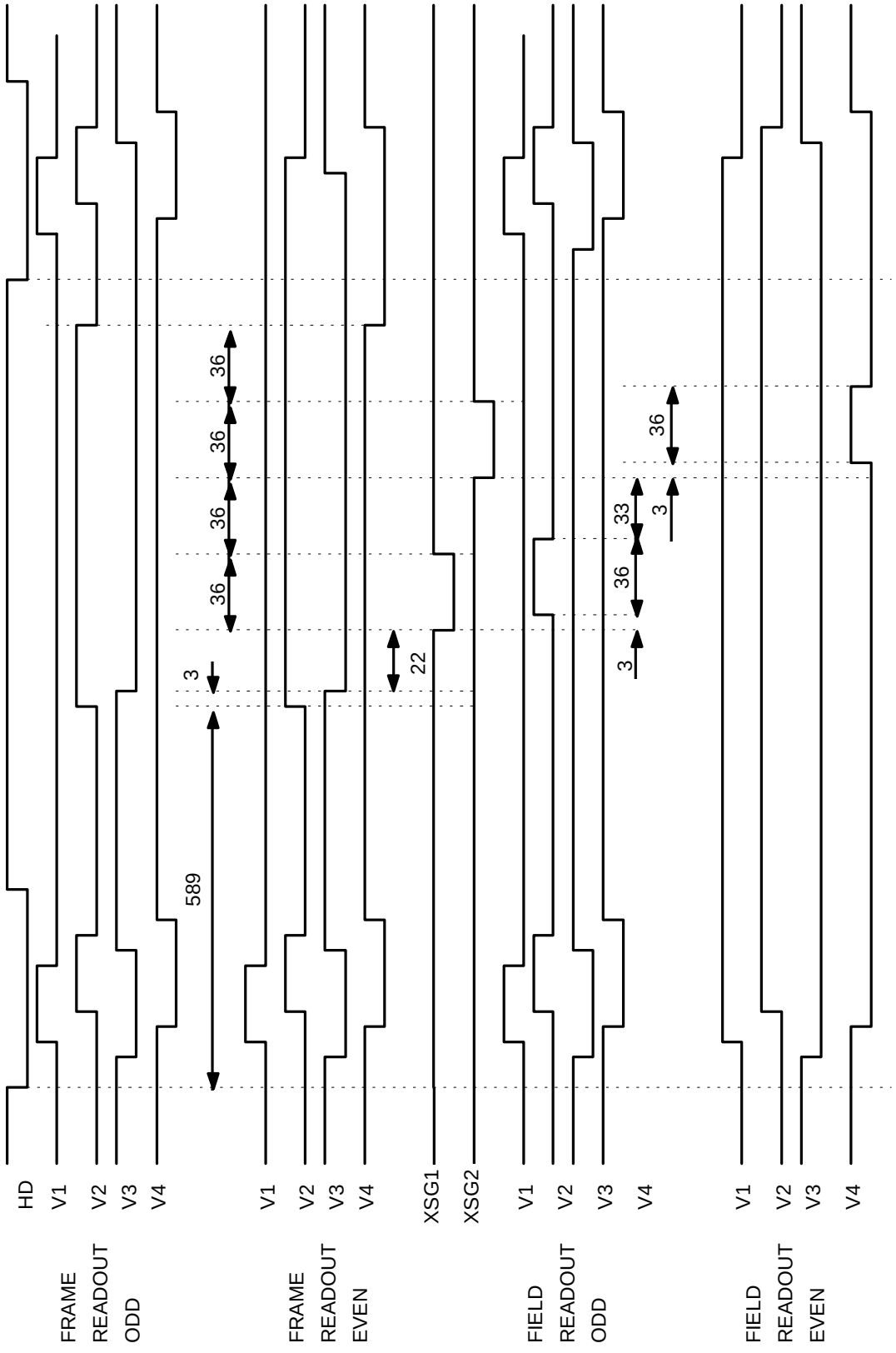
* VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR NORMAL EIA AND CCIR



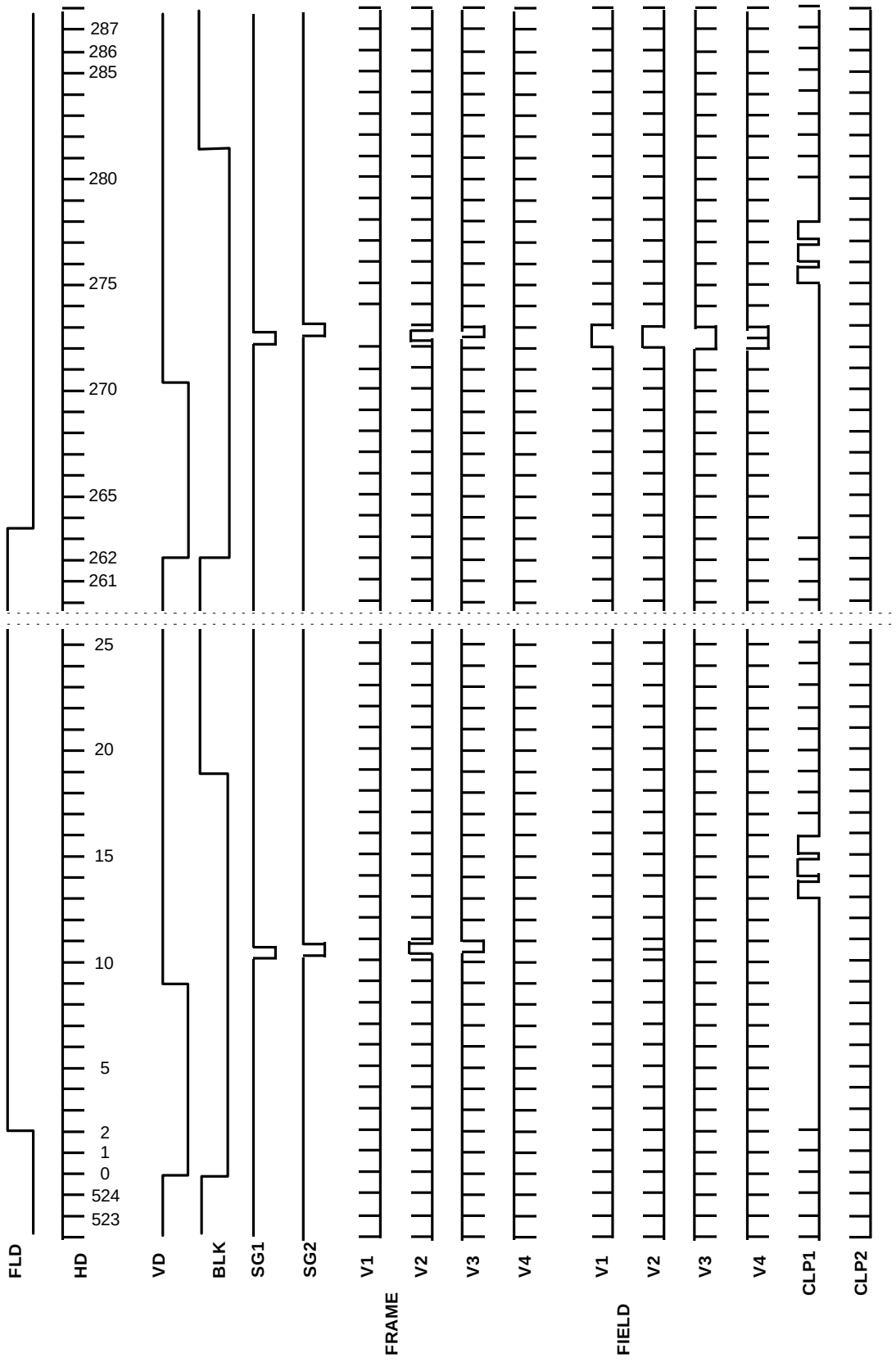
* VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR HI8 EIA UNIT : 1CK = 69.84ns



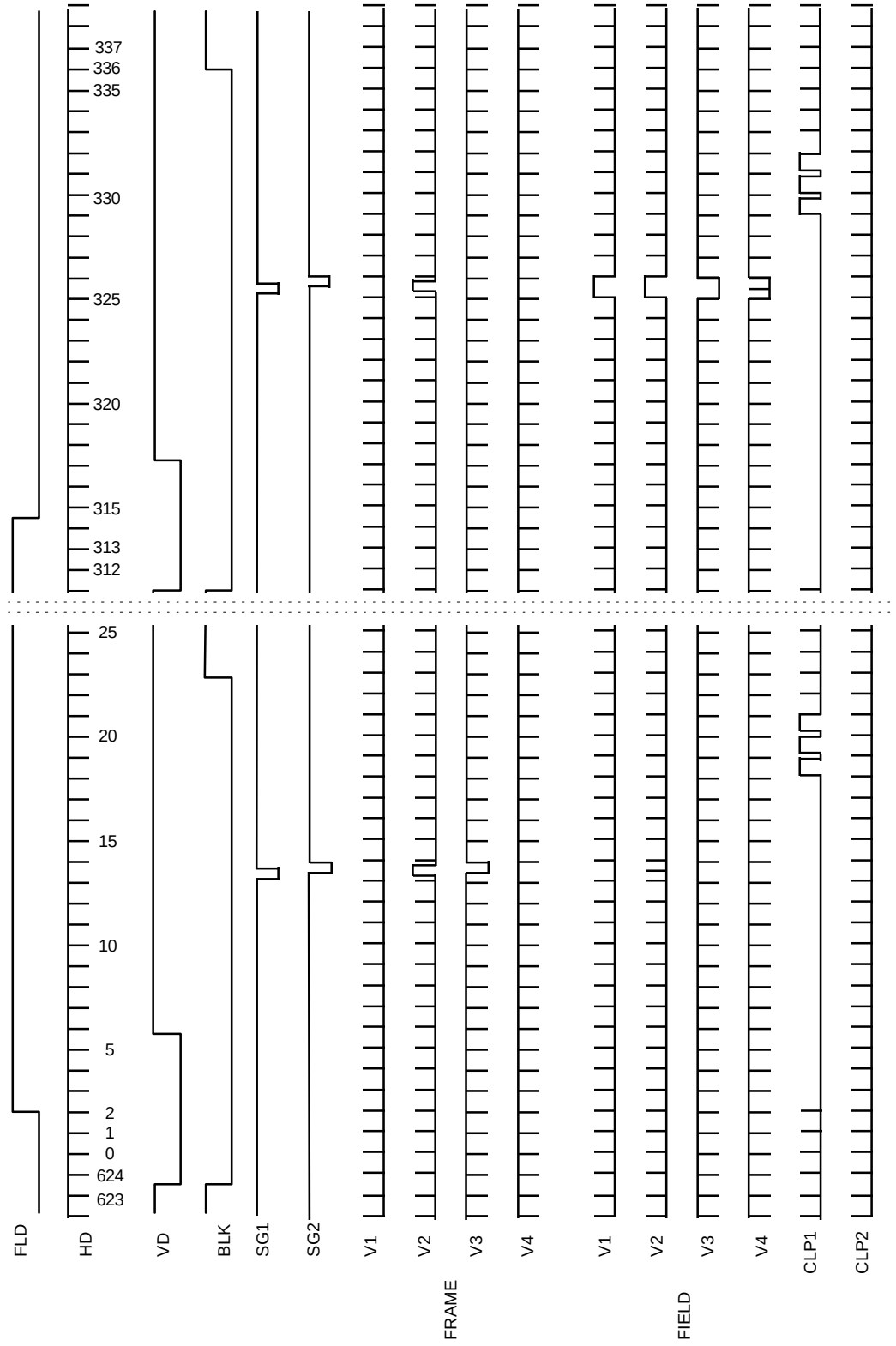
* VERTICAL CCD REGISTER DRIVING PULSE TIMING CHART FOR HI8 CCIR UNIT : 1CK = 70.48ns



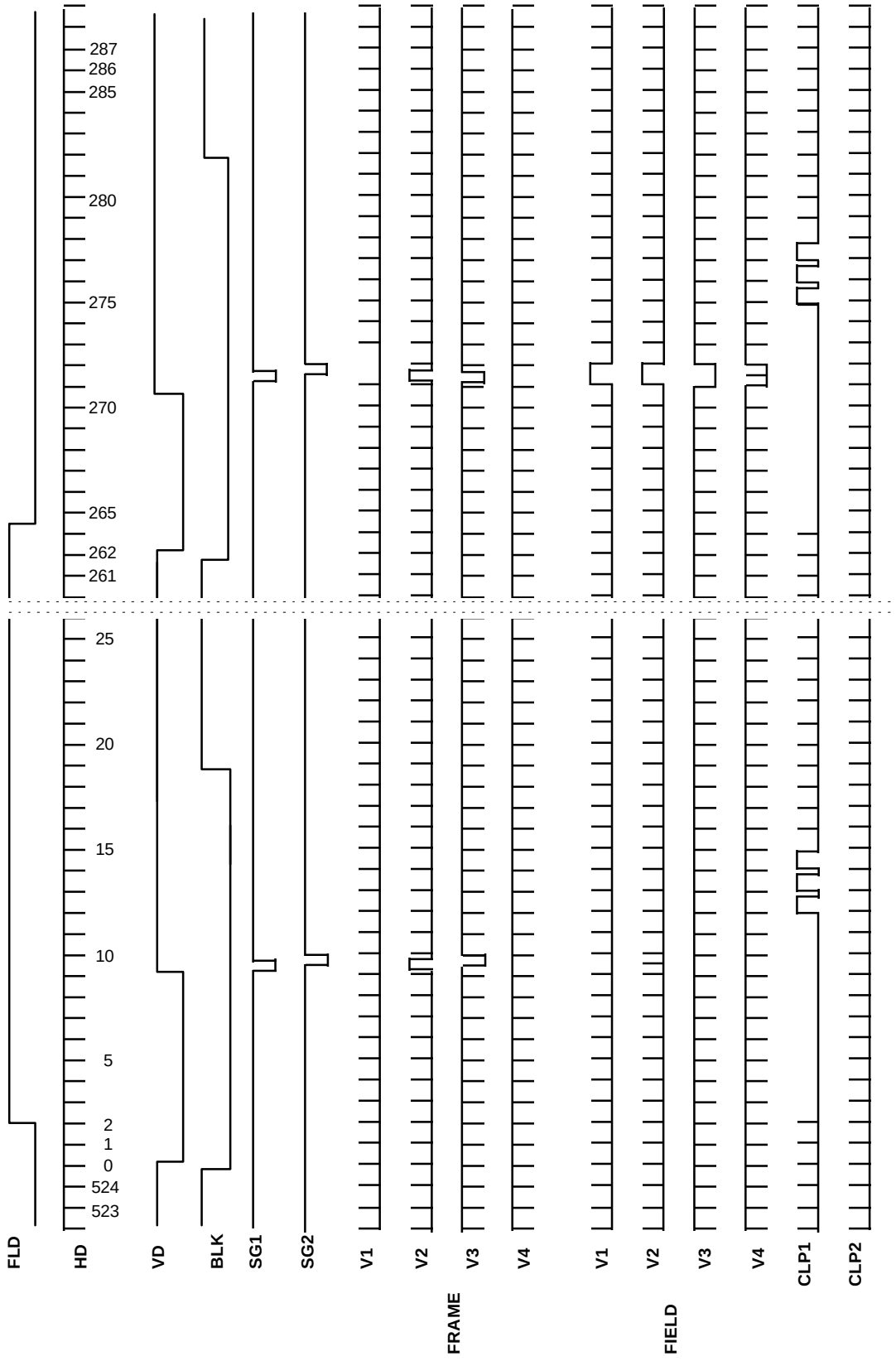
NORMAL EIA VERTICAL TIMING CHART AT INTERLACE



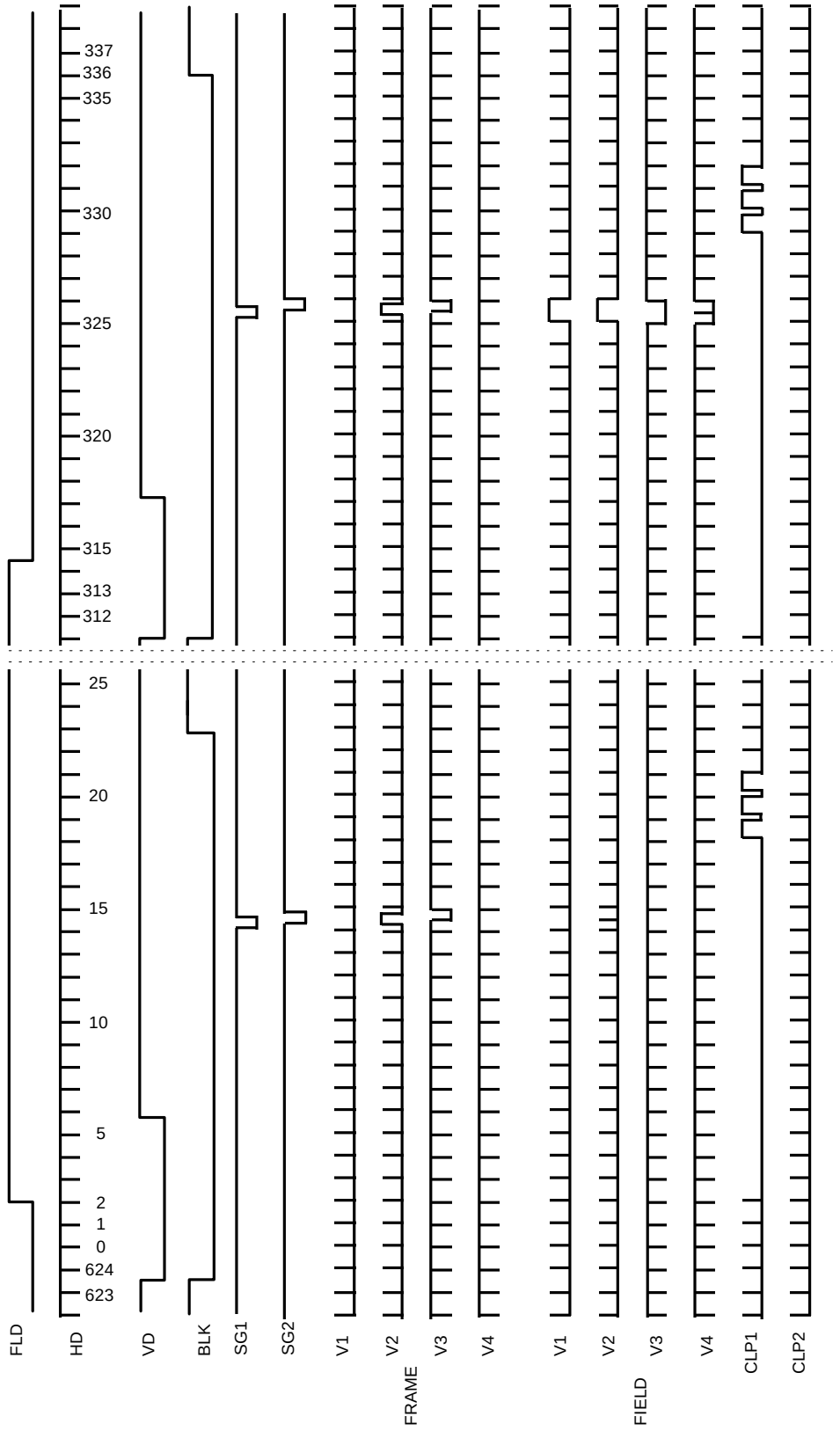
NORMAL CCIR VERTICAL TIMING CHART AT INTERLACE



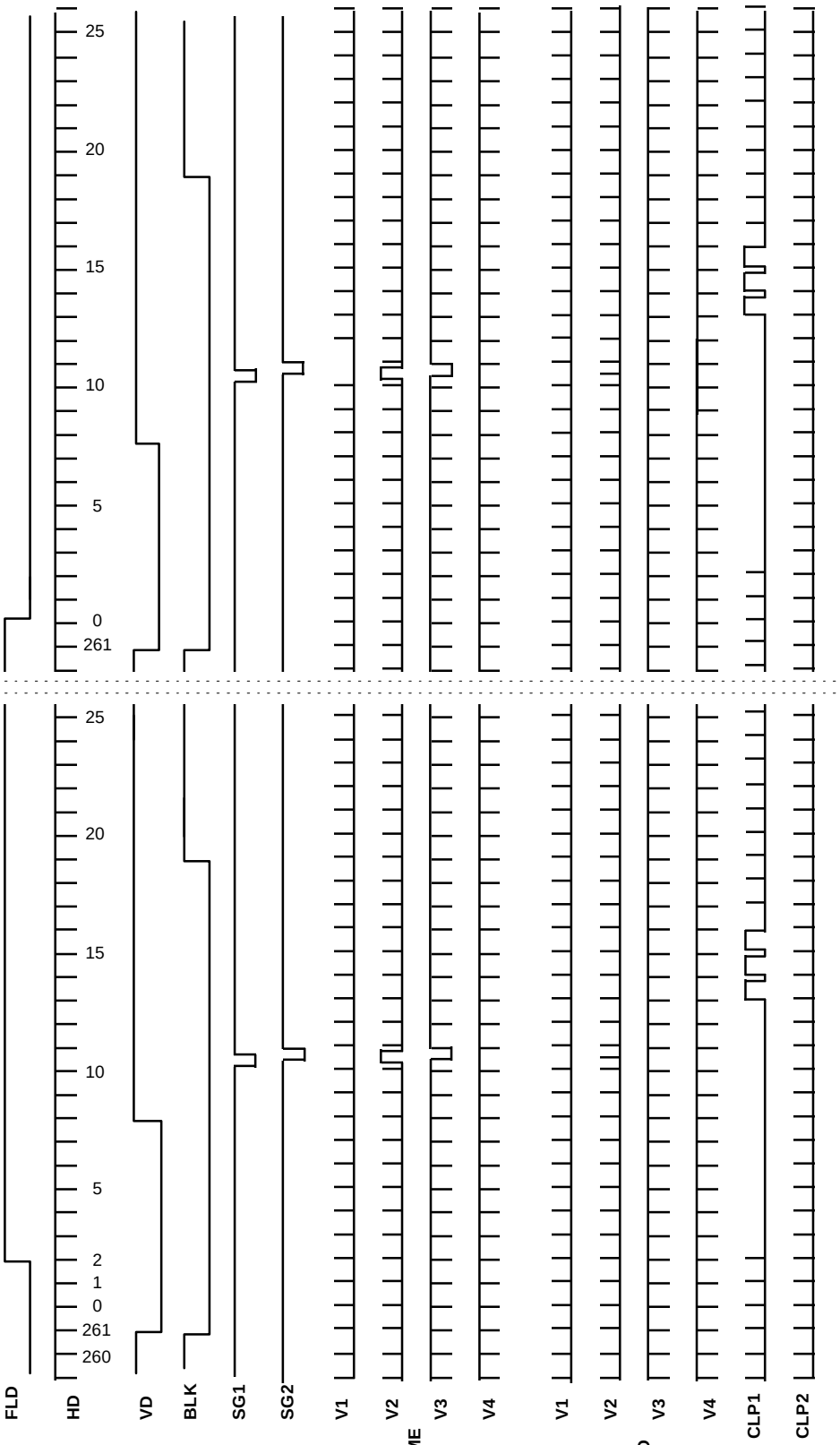
HI8 EIA VERTICAL TIMING CHART AT INTERLACE



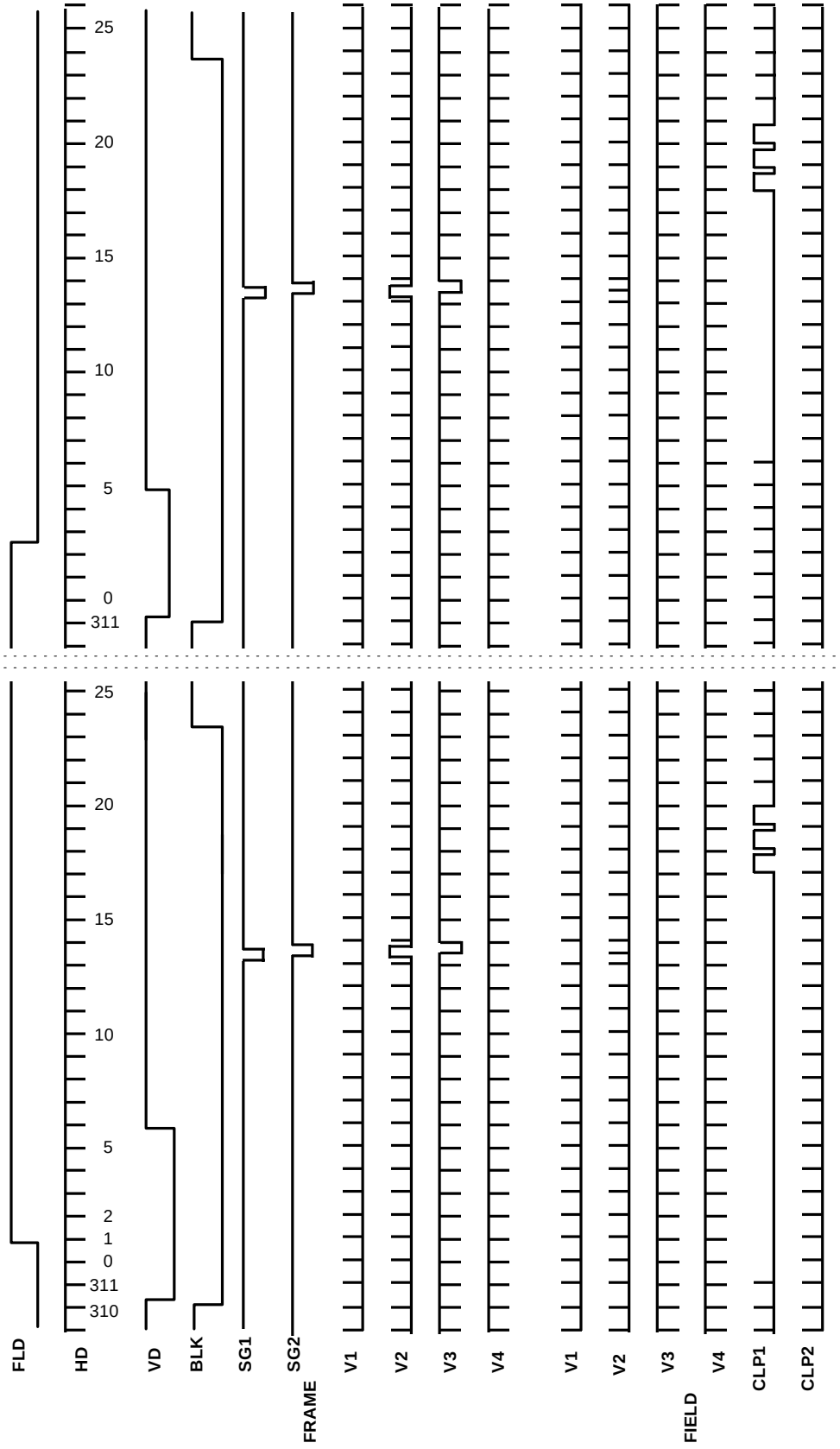
HI8 CCIR VERTICAL TIMING CHART AT INTERLACE



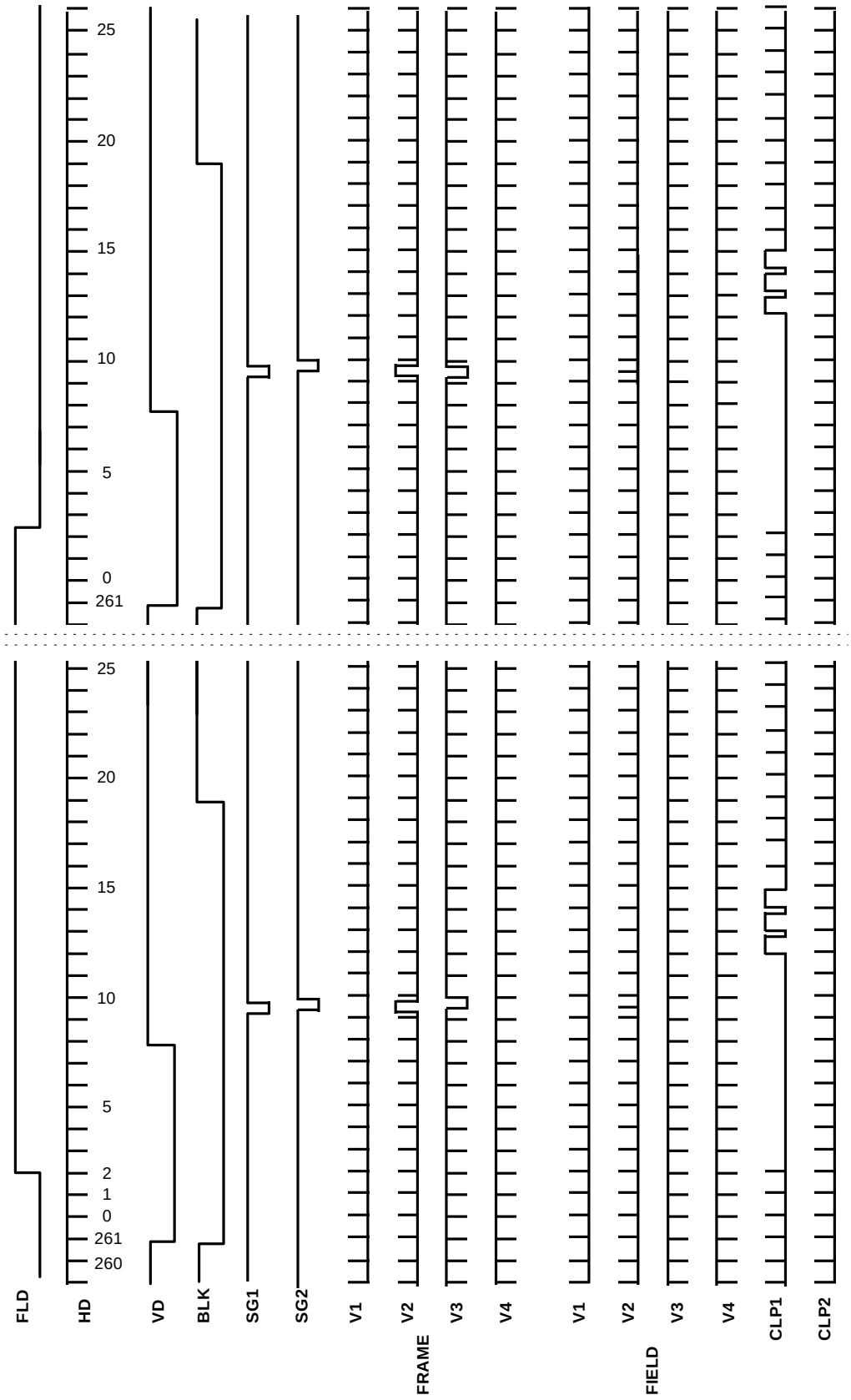
NORMAL EIA VERTICAL TIMING CHART AT NON - INTERLACE



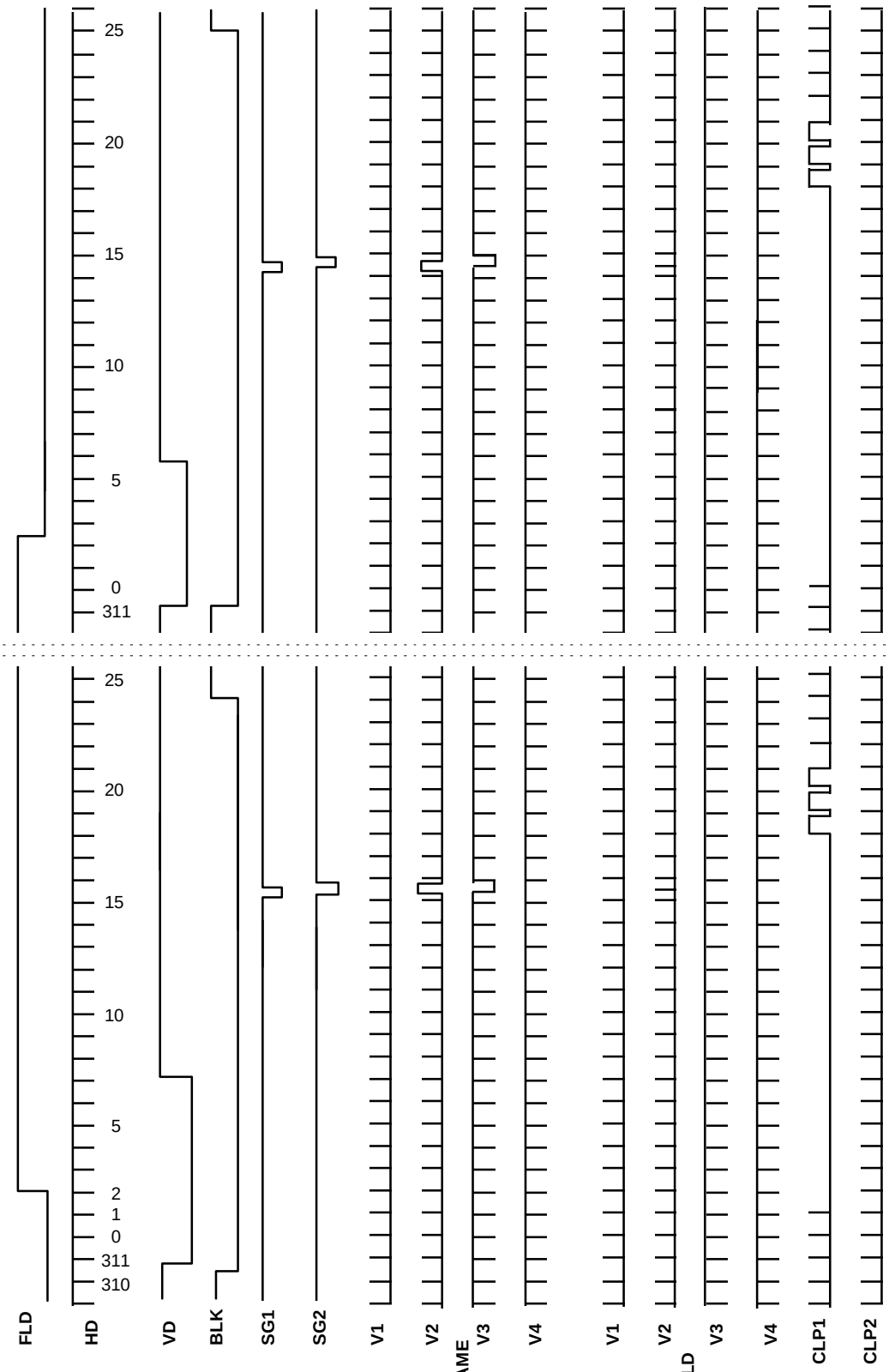
NORMAL CCIR VERTICAL TIMING CHART AT NON - INTERLACE



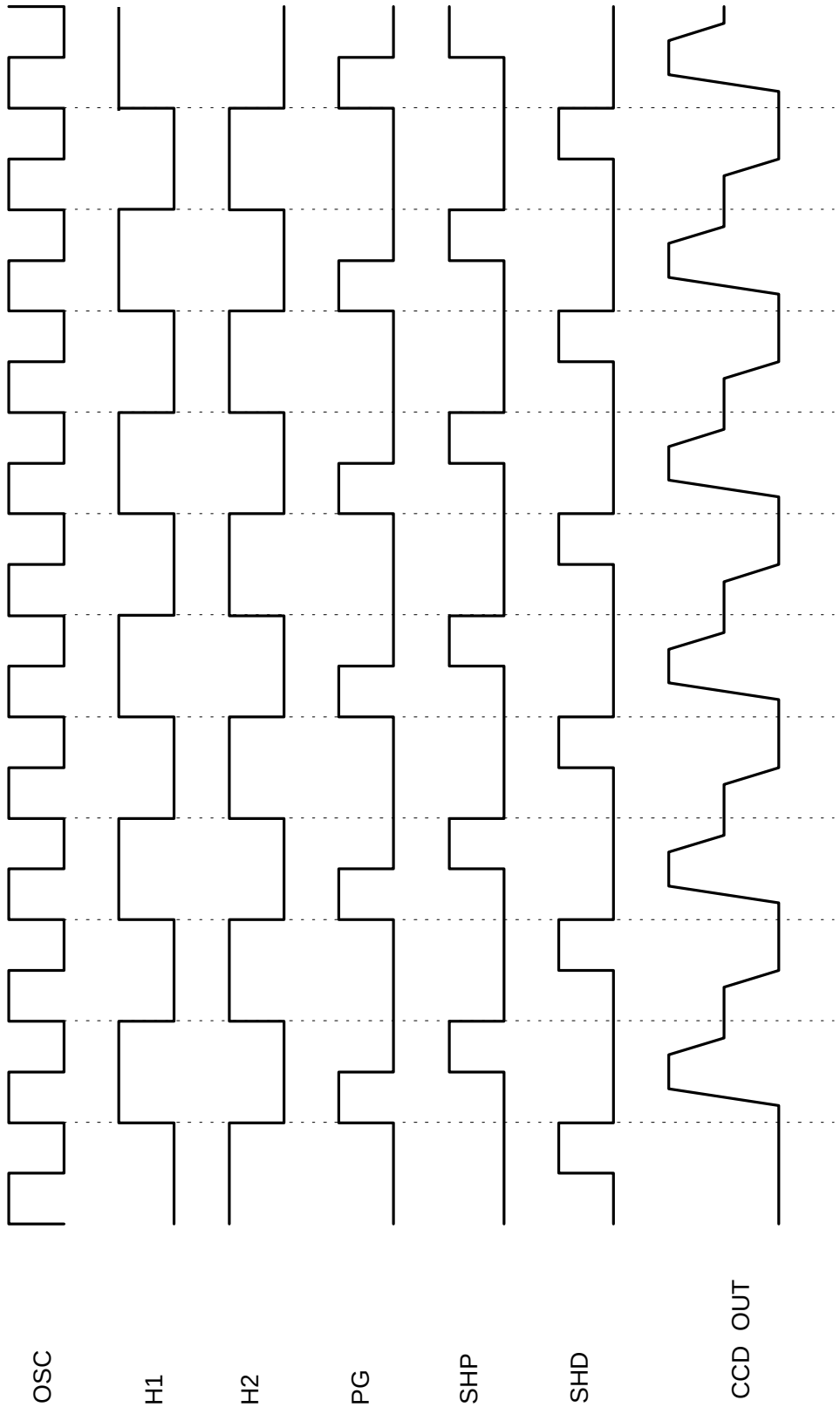
HI8 EIA VERTICAL TIMING CHART AT NON - INTERLACE



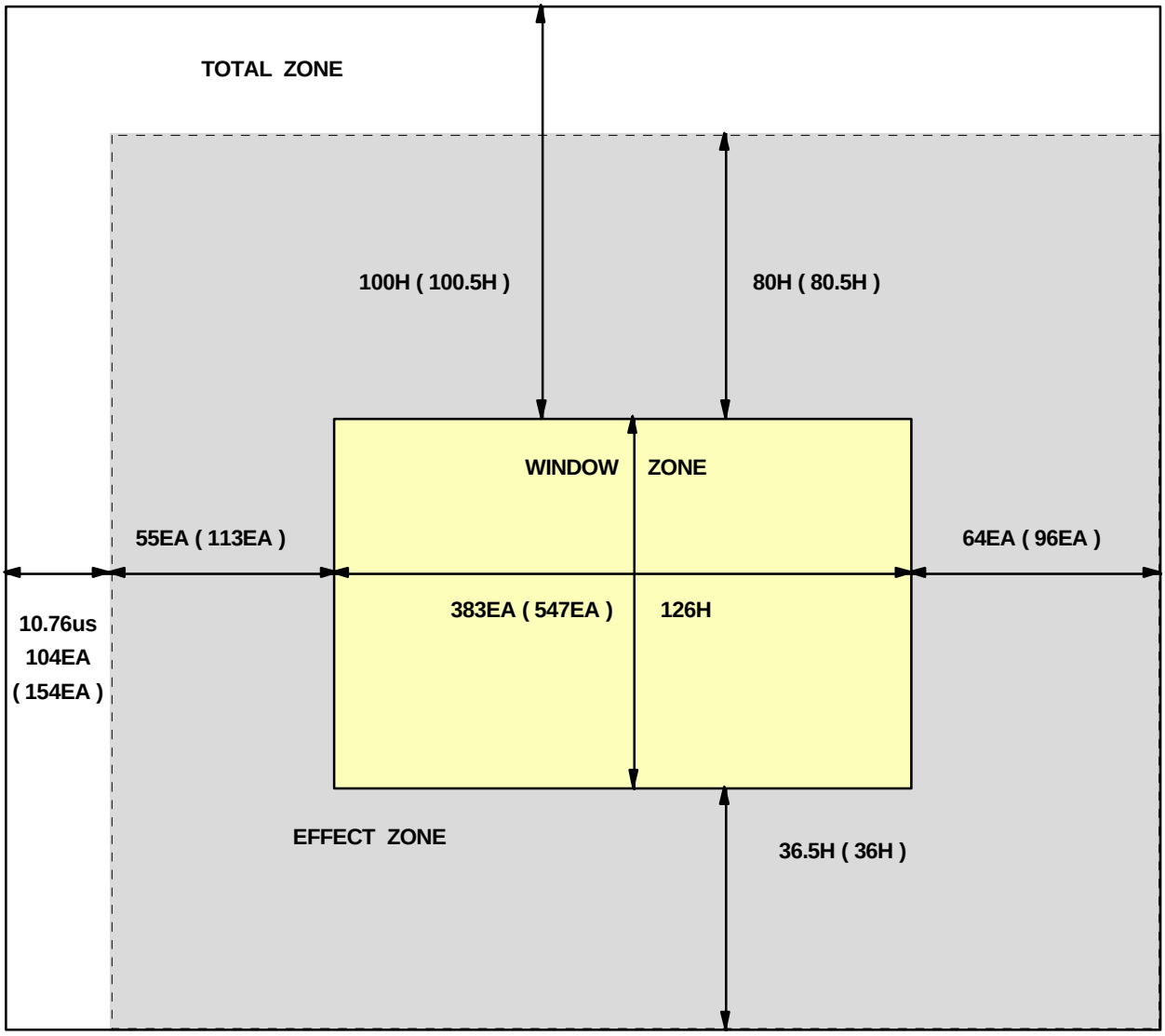
HI8 CCIR VERTICAL TIMING CHART AT NON - INTERLACE



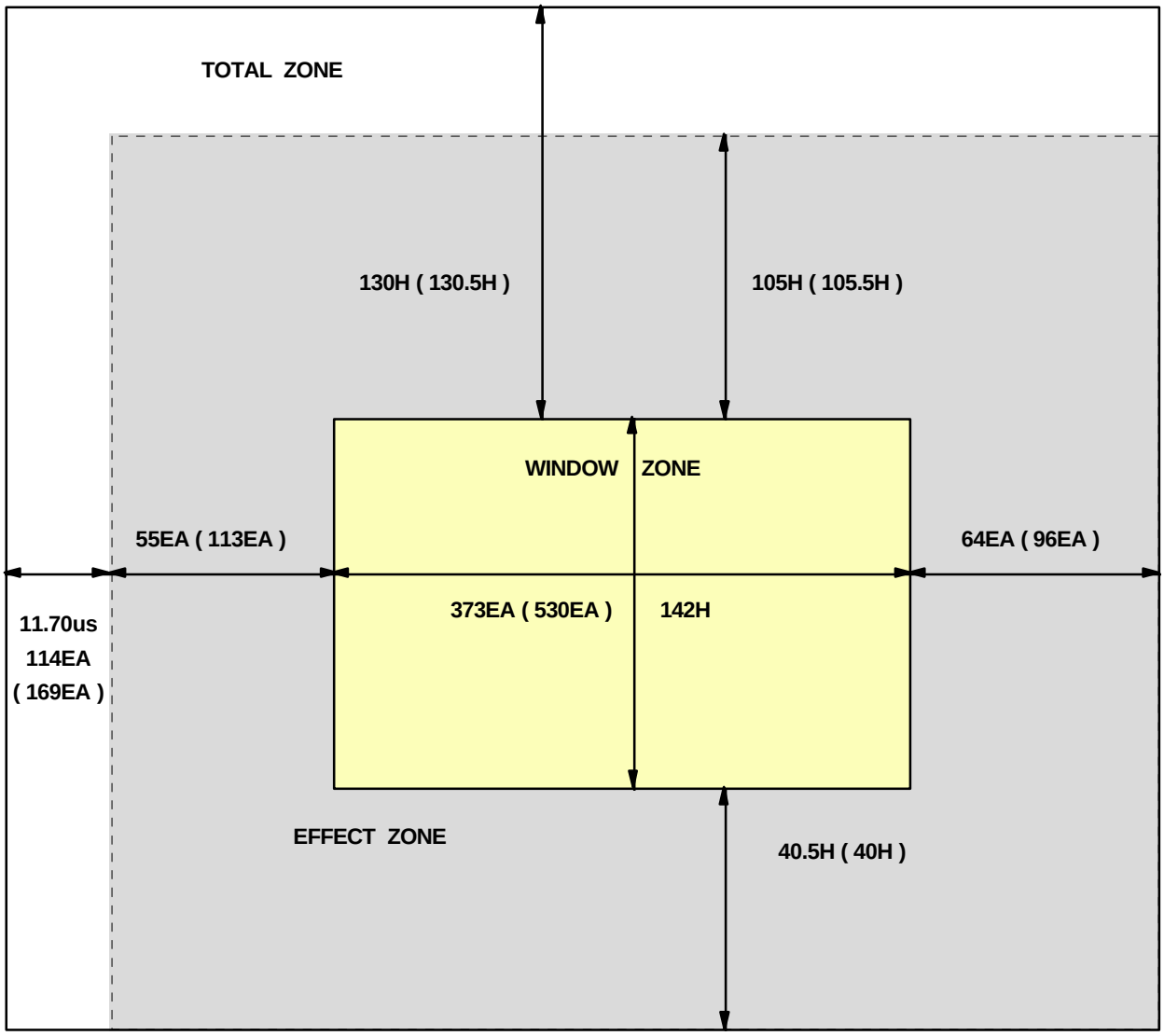
HIGH SPEED PHASE TIMING CHART



EIA NORMAL/HI8 WINDOW AREA

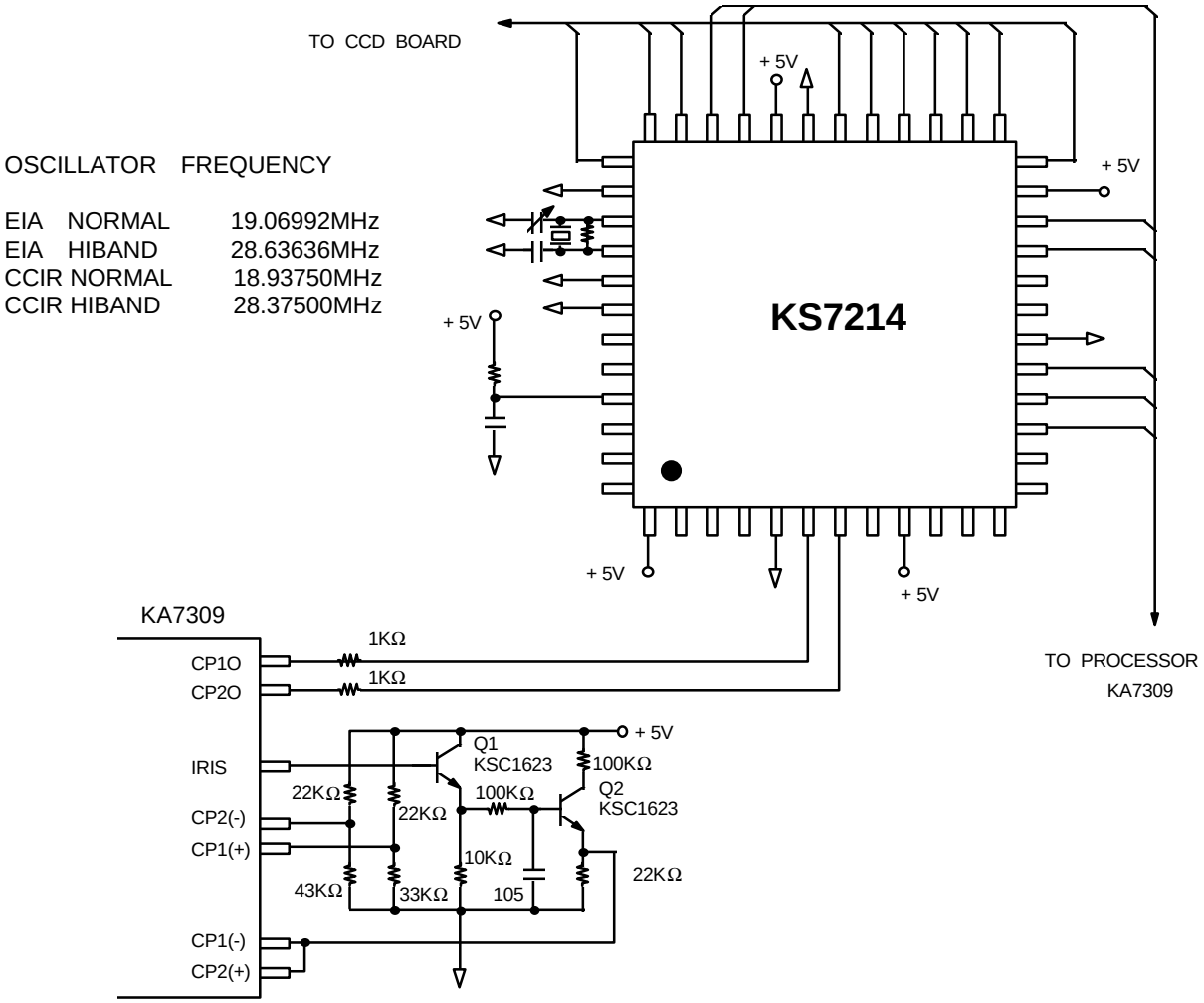


CCIR NORMAL/HI8 WINDOW AREA



APPLIATION EXAMPLE

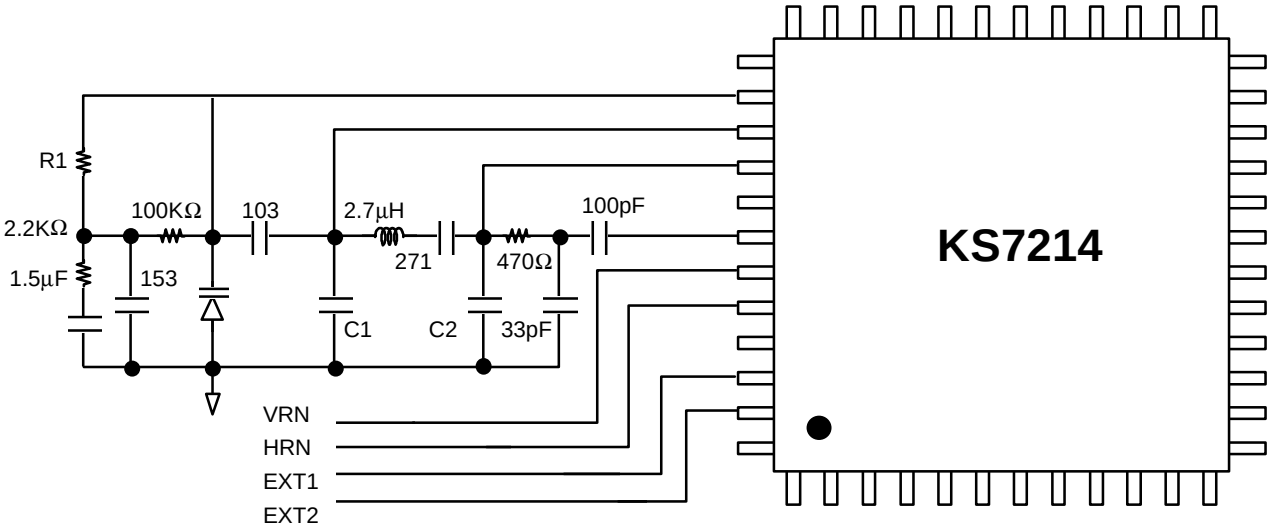
EIA NORMAL AUTO IRIS MODE APPLICATION



OSCILLATOR FREQUENCY

EIA NORMAL	19.06992MHz
EIA HIBAND	28.63636MHz
CCIR NORMAL	18.93750MHz
CCIR HIBAND	28.37500MHz

APPLIATION EXAMPLE (Continued)



MODE	EXT1	EXT2	VRN	HRN
COMP.SYNC	0	1	-	COMP.SYNC
LINE LOCK	1	0	60Hz	-
SEPA.SYNC	1	1	VD	HD

PACKAGE DIMENSION

48-QFP-0707

unit : mm