

# MC10EP52, MC100EP52

## 3.3V / 5V ECL Differential Data and Clock D Flip-Flop

The MC10EP/100EP52 is a differential data, differential clock D flip-flop. The device is pin and functionally equivalent to the EL52 device.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EP52 allow the device to also be used as a negative edge triggered device.

The EP52 employs input clamping circuitry so that under open input conditions (pulled down to  $V_{EE}$ ) the outputs of the device will remain stable.

The 100 Series contains temperature compensation.

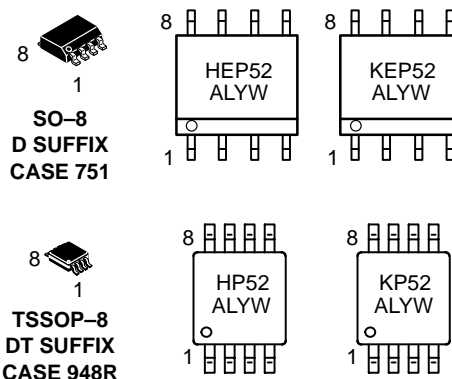
- 330 ps Typical Propagation Delay
- Maximum Frequency > 4 GHz Typical
- PECL Mode:  $V_{CC} = 3.0\text{ V to }5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V to }-5.5\text{ V}$
- Open Input Default State
- Safety Clamp on Inputs
- Q Output Will Default LOW with Inputs Open or at  $V_{EE}$



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### MARKING DIAGRAMS\*



H = MC10                      L = Wafer Lot  
K = MC100                    Y = Year  
A = Assembly Location      W = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC10EP52D	SO-8	98 Units/Rail
MC10EP52DR2	SO-8	2500 Tape & Reel
MC100EP52D	SO-8	98 Units/Rail
MC100EP52DR2	SO-8	2500 Tape & Reel
MC10EP52DT	TSSOP-8	100 Units/Rail
MC10EP52DTR2	TSSOP-8	2500 Tape & Reel
MC100EP52DT	TSSOP-8	100 Units/Rail
MC100EP52DTR2	TSSOP-8	2500 Tape & Reel

# MC10EP52, MC100EP52

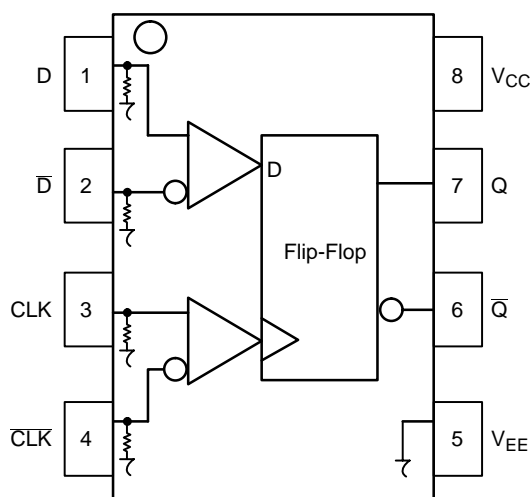


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

## PIN DESCRIPTION

PIN	FUNCTION
CLK*, $\overline{\text{CLK}}^*$	ECL Clock Inputs
D*, $\overline{\text{D}}^*$	ECL Data Input
Q, $\overline{\text{Q}}$	ECL Data Outputs
V <sub>CC</sub>	Positive Supply
V <sub>EE</sub>	Negative Supply

\* Pins will default LOW when left open.

## TRUTH TABLE

D	CLK	Q
L	Z	L
H	Z	H

Z = LOW to HIGH Transition

## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1.)	Level 1
Flammability Rating Oxygen Index	UL-94 code V-0 A 1/8" 28 to 34
Transistor Count	155 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 2.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	PECL Mode Power Supply	V <sub>EE</sub> = 0 V		6	V
V <sub>EE</sub>	NECL Mode Power Supply	V <sub>CC</sub> = 0 V		-6	V
V <sub>I</sub>	PECL Mode Input Voltage NECL Mode Input Voltage	V <sub>EE</sub> = 0 V V <sub>CC</sub> = 0 V	V <sub>I</sub> $\leq$ V <sub>CC</sub> V <sub>I</sub> $\geq$ V <sub>EE</sub>	6 -6	V V
I <sub>out</sub>	Output Current	Continuous Surge		50 100	mA mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			$\pm$ 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	$^{\circ}$ C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	$^{\circ}$ C
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	$^{\circ}$ C/W $^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	$^{\circ}$ C/W
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	$^{\circ}$ C/W $^{\circ}$ C/W
$\theta_{JC}$	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	$^{\circ}$ C/W
T <sub>sol</sub>	Wave Solder	<2 to 3 sec @ 248 $^{\circ}$ C		265	$^{\circ}$ C

2. Maximum Ratings are those values beyond which device damage may occur.

# MC10EP52, MC100EP52

## 10EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 3.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
$V_{OH}$	Output HIGH Voltage (Note 4.)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
$V_{OL}$	Output LOW Voltage (Note 4.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2090		2415	2155		2480	2215		2540	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1365		1690	1430		1755	1490		1815	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 5.)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

3. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

4. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 10EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 6.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
$V_{OH}$	Output HIGH Voltage (Note 7.)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
$V_{OL}$	Output LOW Voltage (Note 7.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	3790		4115	3855		4180	3915		4240	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	3065		3390	3130		3455	3190		3515	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 8.)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

7. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 10EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ , $V_{EE} = -5.5\text{ V}$ to $-3.0\text{ V}$ (Note 9.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
$V_{OH}$	Output HIGH Voltage (Note 10.)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
$V_{OL}$	Output LOW Voltage (Note 10.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1210		-885	-1145		-820	-1085		-760	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 11.)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .

10. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

11.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP52, MC100EP52

## 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 12.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
$V_{OH}$	Output HIGH Voltage (Note 13.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
$V_{OL}$	Output LOW Voltage (Note 13.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 14.)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

12. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

13. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

14.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 15.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
$V_{OH}$	Output HIGH Voltage (Note 16.)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
$V_{OL}$	Output LOW Voltage (Note 16.)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	3055		3375	3055		3375	3055		3375	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 17.)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

15. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

16. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

17.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ , $V_{EE} = -5.5\text{ V}$ to $-3.0\text{ V}$ (Note 18.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	26	34	44	26	35	45	28	37	47	mA
$V_{OH}$	Output HIGH Voltage (Note 19.)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
$V_{OL}$	Output LOW Voltage (Note 19.)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 20.)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

18. Input and output parameters vary 1:1 with  $V_{CC}$ .

19. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

20.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP52, MC100EP52

**AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 21.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency (See Figure 2. $F_{\max}/\text{Jitter}$ )		> 4			> 4			> 4		GHz
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Propagation Delay to Output Differential CLK, $\overline{\text{CLK}} \rightarrow \text{Q}, \overline{\text{Q}}$	250	300	350	280	330	380	310	360	410	ps
$t_{\text{S}}$ $t_{\text{H}}$	Setup Time Hold Time	50 0			50 0			50 0			ps
$t_{\text{JITTER}}$	Cycle-to-Cycle Jitter (See Figure 2. $F_{\max}/\text{Jitter}$ )		.2	< 1		.2	< 1		.2	< 1	ps
$V_{\text{PP}}$	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
$t_{\text{r}}$ $t_{\text{f}}$	Output Rise/Fall Times (20% – 80%) Q, $\overline{\text{Q}}$	70	110	170	80	120	180	90	130	200	ps

21. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to  $V_{CC} - 2.0\text{ V}$ .

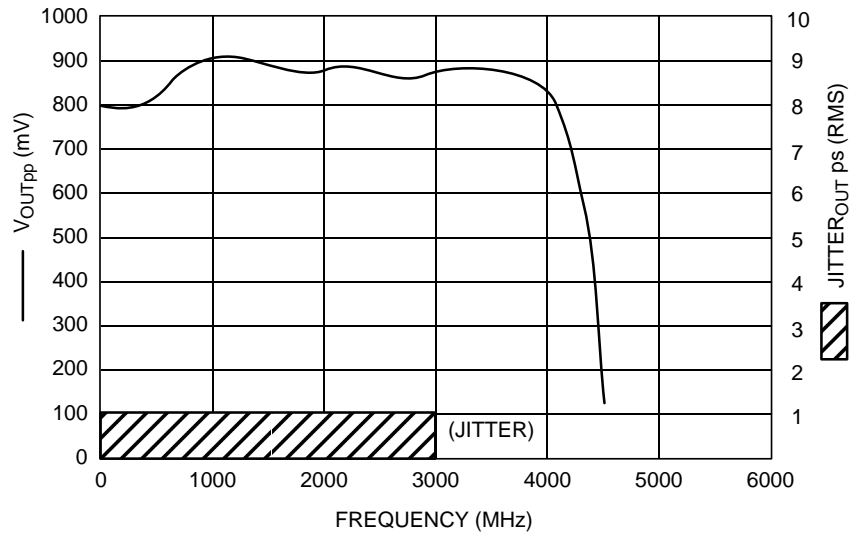
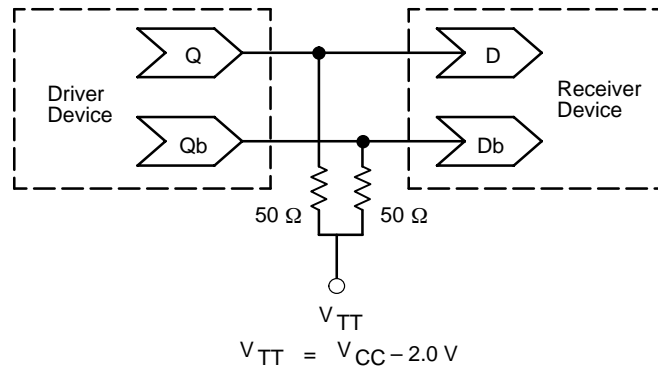


Figure 2.  $F_{\max}/\text{Jitter}$

## MC10EP52, MC100EP52



**Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020 – Termination of ECL Logic Devices.)**

### Resource Reference of Application Notes

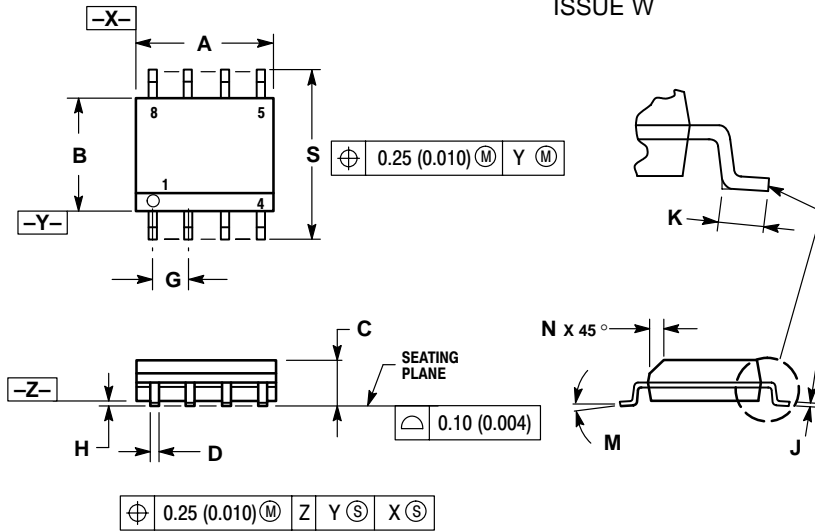
- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

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# MC10EP52, MC100EP52

## PACKAGE DIMENSIONS

### SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE W

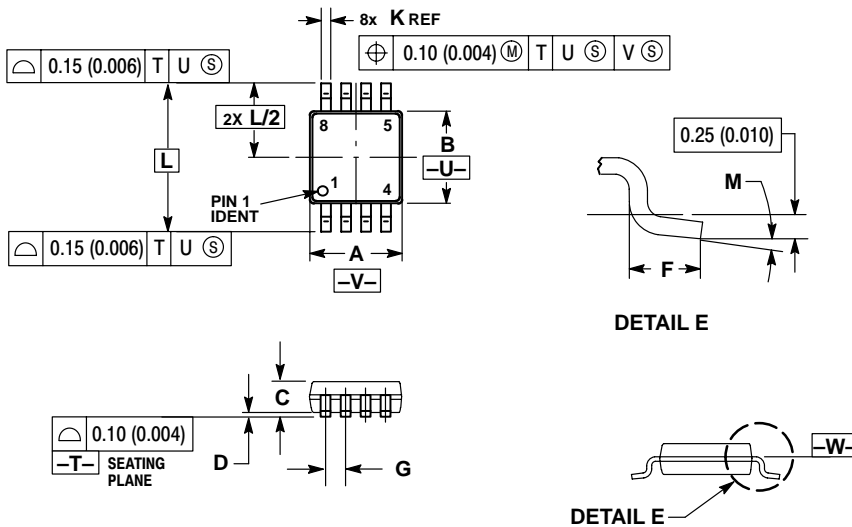


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

# MC10EP52, MC100EP52

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