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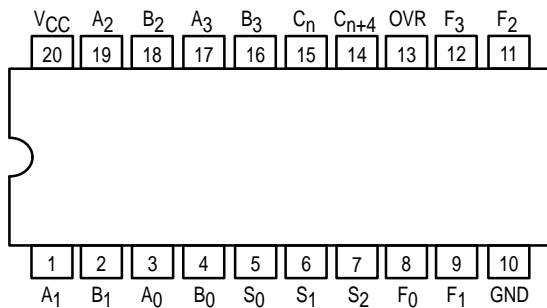


4-BIT ARITHMETIC LOGIC UNIT

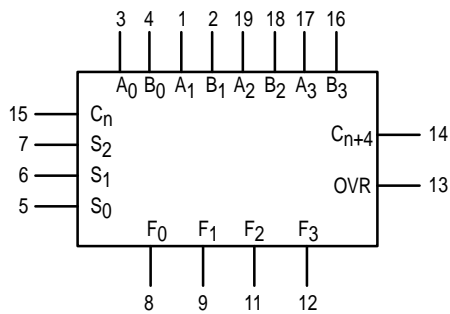
The MC54/74F382 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional Select input codes force the Function outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, refer to the F381 data sheet.

- Performs Six Arithmetic and Logic Functions
- Selectable Low (Clear) and High (Preset) Functions
- LOW Input Loading Minimizes Drive Requirements
- Carry Output for Ripple Expansion
- Overflow Output for Twos Complement Arithmetic

CONNECTION DIAGRAM

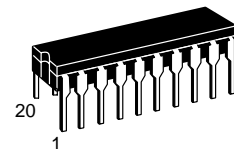


LOGIC SYMBOL

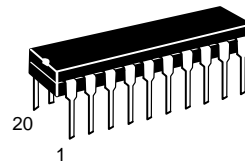


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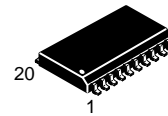
4-BIT ARITHMETIC LOGIC UNIT FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

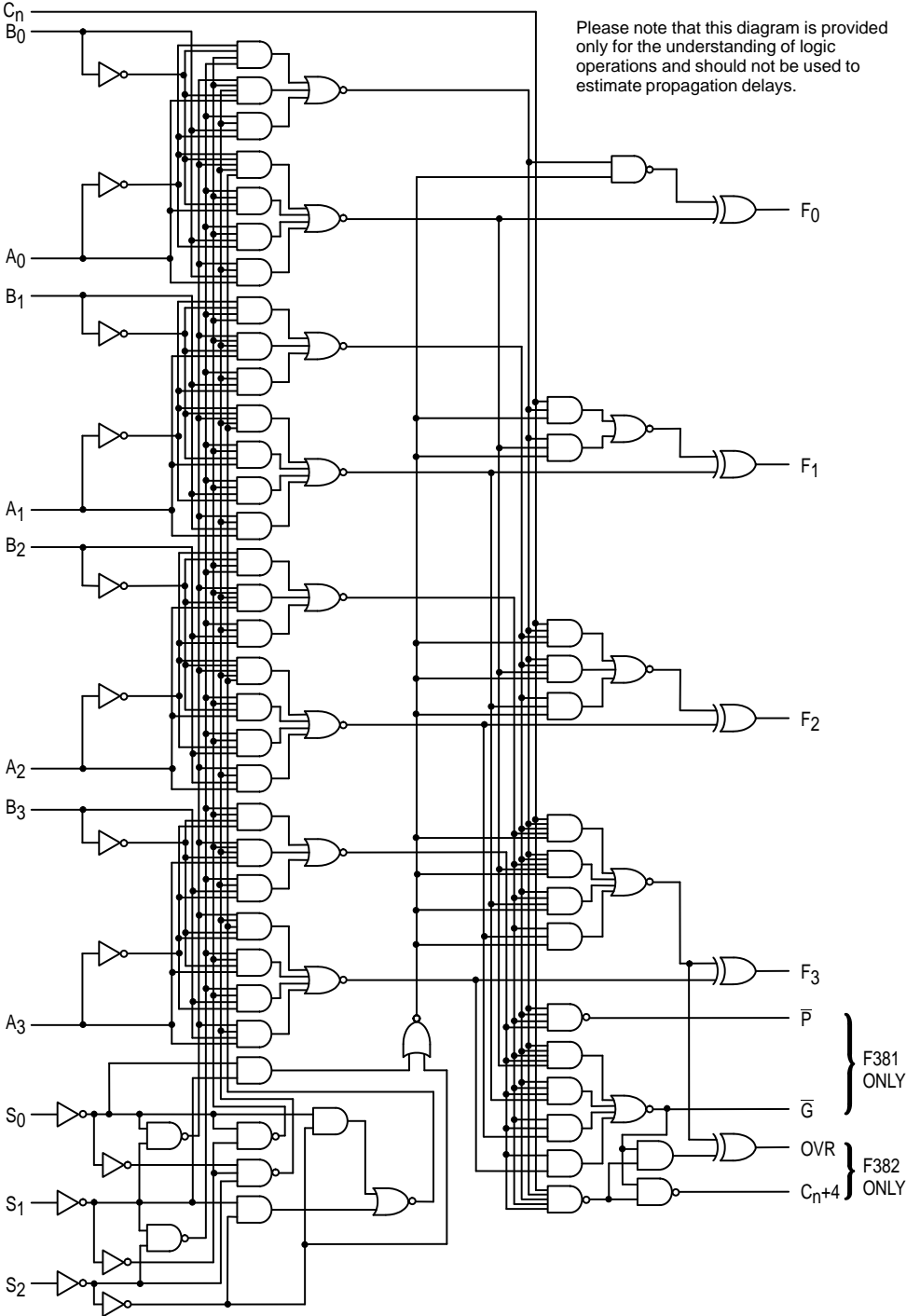
MC54FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-1.0	mA
I _{OL}	Output Current — Low	54, 74			20	mA

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LOGIC DIAGRAM



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage			-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.5	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.5 V
		74	2.7	3.4	V	I _{OH} = -1.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA	V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
				100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current S ₀ -S ₂ Inputs			-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
	Other Inputs			-2.4	mA		
	C _n Input			-3.0	mA		
I _{OS}	Output Short Circuit Current (Note 2)	-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current		54	81	mA	S ₀ , C _n = HIGH; Other Inputs GND	V _{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

Signals applied to the Select inputs S₀-S₂ determine the mode of operation, as indicated in the Function Select Table. An extensive listing of input and output levels is shown in the Truth Table. The circuit performs the arithmetic functions for either active HIGH or active LOW operands, with output levels in the same convention. In the Subtract operating modes, it is necessary to force a carry (HIGH for active HIGH operands,

LOW for active LOW operands) into the C_n input of the least significant package. Ripple expansion is illustrated in Figure 1. The overflow output OVR is the Exclusive-OR of C_{n+3} and C_{n+4}; a HIGH signal on OVR indicates overflow in two's complement operation. Typical delays for Figure 1 are given in Figure 2.

FUNCTION SELECT TABLE

Select			Operation
S ₀	S ₁	S ₂	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	A⊕B
H	L	H	A + B
L	H	H	AB
H	H	H	Preset

H = HIGH Voltage Level

L = LOW Voltage Level

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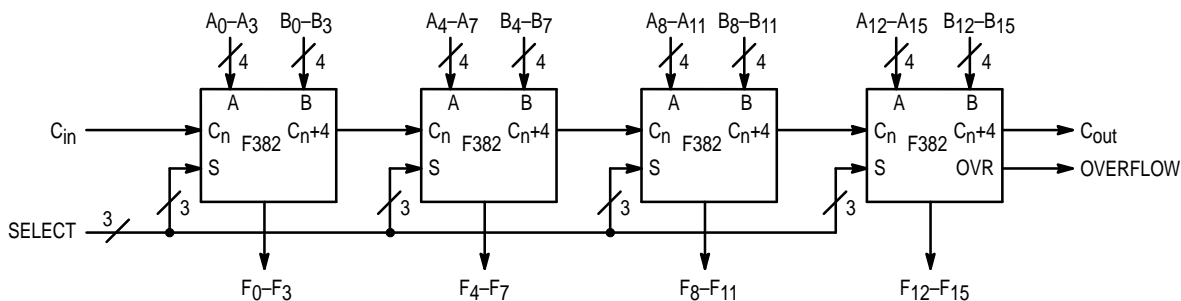


Figure 1. 16-Bit Ripple Carry ALU Expansion

Path Segment	Toward F	Output $C_n + 4, OVR$
A_i or B_j to $C_n + 4$	6.5 ns	6.5 ns
C_n to $C_n + 4$	6.3 ns	6.3 ns
C_n to $C_n + 4$	6.3 ns	6.3 ns
C_n to F	8.1	—
C_n to $C_n + 4, OVR$	—	8.0 ns
Total Delay	27.2 ns	27.1 ns

Figure 2. 16-Bit Delay Tabulation

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A = -55\text{ to }+125^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$		$T_A = 0\text{ to }70^\circ\text{C}$ $V_{CC} = 5.0\text{ V } \pm 10\%$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to F_i	3.0 2.5	8.1 5.7	12 8.0	3.0 2.5	15 11	3.0 2.5	13 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay Any A or B to Any F	4.0 3.5	10.4 8.2	15 11	4.0 3.5	18 14	4.0 3.5	16 12	ns
t_{PLH} t_{PHL}	Propagation Delay S_i to F_j	6.0 4.0	11 8.2	15 20.5	6.0 4.0	21 23.5	6.0 4.0	16 21.5	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_j to $C_n + 4$	3.5 3.0	6.0 6.5	8.5 9.0	3.5 3.0	11.5 12.5	3.5 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay S_i to OVR or $C_n + 4$	7.0 4.5	12.5 9.0	16.5 12	7.0 4.5	19.5 15	7.0 4.5	17.5 13	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $C_n + 4$	2.5 2.5	5.6 6.3	8.0 9.0	2.5 2.5	11 12	2.5 2.5	9.0 10	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to OVR	3.5 3.5	8.0 7.1	11 10	3.5 3.5	14 13	3.5 3.5	12 11	ns
t_{PLH} t_{PHL}	Propagation Delay A_i or B_j to OVR	6.5 5.5	11.5 8.0	15.5 10.5	6.5 5.5	18.5 13.5	6.5 5.5	16.5 11.5	ns

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TRUTH TABLE

Function	INPUTS						OUTPUTS							
	S ₀	S ₁	S ₂	C _n	A _n	B _n	F ₀	F ₁	F ₂	F ₃	OVR	C _{n+4}		
CLEAR	0	0	0	0	X	X	0	0	0	0	1	1		
				1	X	X	0	0	0	0	1	1		
B MINUS A	1	0	0	0	0	0	1	1	1	1	0	0		
				0	0	1	0	1	1	1	0	1		
				0	1	0	0	0	0	0	0	0	0	
				0	1	1	1	1	1	1	1	0	0	
				1	0	0	0	0	0	0	0	0	1	
				1	0	1	1	1	1	1	1	0	1	
				1	1	0	1	0	0	0	0	0	0	0
A MINUS B	0	1	0	0	0	0	1	1	1	1	0	0		
				0	0	1	0	0	0	0	0	0	0	
				0	1	0	0	1	1	1	1	0	1	
				0	1	1	1	1	1	1	1	0	0	
				1	0	0	0	0	0	0	0	0	1	
				1	0	1	1	0	0	0	0	0	0	0
				1	1	0	1	1	1	1	1	0	1	1
A PLUS B	1	1	0	0	0	0	0	0	0	0	0	0		
				0	0	1	1	1	1	1	0	0		
				0	1	0	1	1	1	1	0	0		
				0	1	1	0	1	1	1	0	1		
				1	0	0	0	1	0	0	0	0	0	
				1	0	1	0	0	0	0	0	0	1	
				1	1	0	0	0	0	0	0	0	1	
A⊕B	0	0	1	X	0	0	0	0	0	0	0	0		
				X	0	1	1	1	1	1	0	0		
				0	1	0	1	1	1	1	0	0		
				X	1	1	0	0	0	0	1	1		
				1	1	0	1	1	1	1	1	1		
A + B	1	0	1	X	0	0	0	0	0	0	0	0		
				X	0	1	1	1	1	1	0	0		
				X	1	0	1	1	1	1	0	0		
				0	1	1	1	1	1	1	0	0		
				1	1	1	1	1	1	1	1	1		
AB	0	1	1	X	0	0	0	0	0	0	1	1		
				X	0	1	0	0	0	0	0	0		
				X	1	0	0	0	0	0	1	1		
				0	1	1	1	1	1	1	0	0		
				1	1	1	1	1	1	1	1	1		
PRESET	1	1	1	X	0	0	1	1	1	1	0	0		
				X	0	1	1	1	1	1	0	0		
				X	1	0	1	1	1	1	0	0		
				0	1	1	1	1	1	1	0	0		
				1	1	1	1	1	1	1	1	1		

1 = HIGH Voltage Level
 0 = LOW Voltage Level
 X = Immaterial