Motorola Semiconductor Technical Data

Addendum to
68HC912BD32
Technical Data

This addendum provides changes to the 68HC912BD32 Advance Information Technical Data Book (Motorola document order number MC68HC912BD32/D Rev. 1.0).

SPI Data Register (SP0DR) Reset Value

On page 163, there is a discrepancy in the definition of the effect of reset on the SP0DR register. The reset values in the register diagram should be ignored as this register is unaffected by reset.

SP0DR — SPI Data Register   **$00D5**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

Wait I_{DD} in Single-Chip Mode at 10MHz

The wait I_{DD} limit in single-chip mode at 10MHz has been changed from 6mA to 8mA. This applies to Table 68 on page 258.

Table 68 Supply Current

V_{DD} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted

Characteristic	Symbol	8 MHz Typical	4 MHz	8 MHz	10 MHz	Unit
WAIT: (All peripheral functions shut down) Single-chip mode	W_{IDD}		3	5	8	mA

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