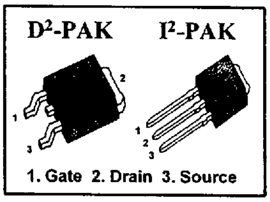
Advanced Power MOSFET

SSW/I6N70A

FEATURES

- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 25 µA (Max.) @ V_{DS} = 700V
- Low $R_{DS(ON)}$: 1.552 Ω (Typ.)

BV_{DSS} = 700 V
$R_{DS(on)}$ = 1.8 Ω
I_D = 6 A



Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	700	V
I_D	Continuous Drain Current (T_C=25 ℃)	6	A
	Continuous Drain Current (T_C=100 ℃)	3.8	
I_{DM}	Drain Current-Pulsed • •	24	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy • •	582	mJ
I_{AR}	Avalanche Current • •	6	A
E_{AR}	Repetitive Avalanche Energy • •	13	mJ
dv/dt	Peak Diode Recovery dv/dt • •	2.5	V/ns
P_D	Total Power Dissipation (T_A=25 ℃) *	3.1	W
	Total Power Dissipation (T_C=25 ℃)	130	W
	Linear Derating Factor	1.04	W/℃
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	℃
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.96	℃/W
$R_{\theta JA}$	Junction-to-Ambient *	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

* When mounted on the minimum pad size recommended (PCB Mount).

SAMSUNG
ELECTRONICS

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	700	--	--	V	V_{GS}=0V,I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.79	--	V/°C	I_D=250μA *See Fig 7*
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V,I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=30V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	25	μA	V_{DS}=700V
		--	--	250		V_{DS}=560V,T_C=125 °C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	1.8	Ω	V_{GS}=10V,I_D=3A ④
g_{fs}	Forward Transconductance	--	4.12	--	℧	V_{DS}=50V,I_D=3A ④
C_{iss}	Input Capacitance	--	920	1200	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz *See Fig 5*
C_{oss}	Output Capacitance	--	100	115		
C_{rss}	Reverse Transfer Capacitance	--	45	55		
$t_{d(on)}$	Turn-On Delay Time	--	18	45	ns	V_{DD}=350V,I_D=6A, R_G=11.5• • *See Fig 13* ④⑤
t_r	Rise Time	--	23	55		
$t_{d(off)}$	Turn-Off Delay Time	--	76	160		
t_f	Fall Time	--	26	60		
Q_g	Total Gate Charge	--	51	67	nC	V_{DS}=560V,V_{GS}=10V, I_D=6A *See Fig 6 & Fig 12* ④⑤
Q_{gs}	Gate-Source Charge	--	8.3	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	23.1	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	6	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	24		
V_{SD}	Diode Forward Voltage ④	--	--	1.4	V	T_J=25 °C ,I_S=6A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	440	--	ns	T_J=25 °C ,I_F=6A di_F/dt=100A/μs ④
Q_{rr}	Reverse Recovery Charge	--	4.05	--	μC	

Notes ;

• •Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

• •L=30mH, I_{AS}=6A, V_{DD}=50V, R_G=27Ω, Starting T_J=25 °C

• •I_{SD} 6A, di/dt 140A/μs, V_{DD} BV_{DSS} , Starting T_J=25 °C

• •Pulse Test : Pulse Width = 250μs, Duty Cycle 2%

• •Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

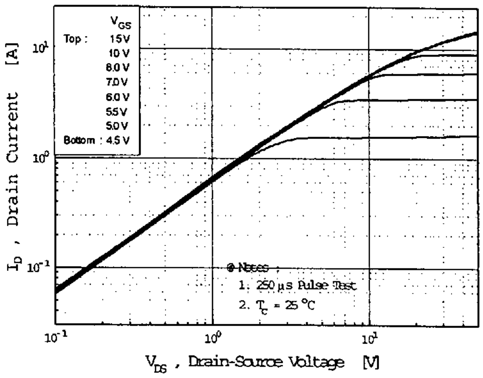


Fig 2. Transfer Characteristics

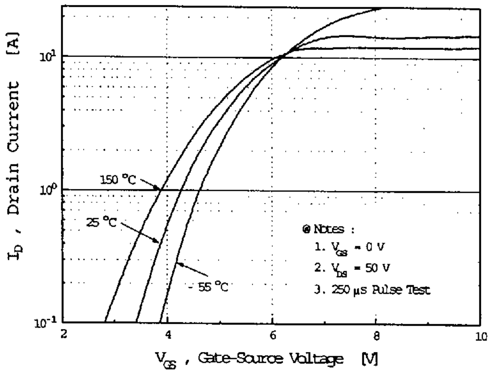


Fig 3. On-Resistance vs. Drain Current

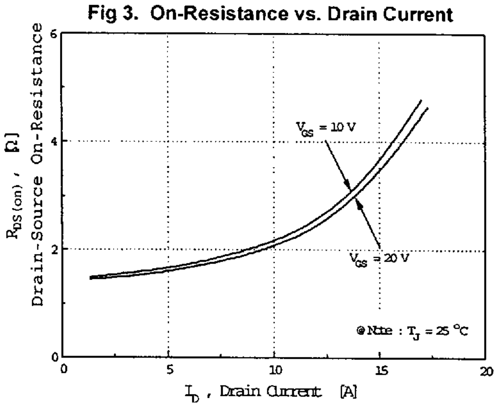


Fig 4. Source-Drain Diode Forward Voltage

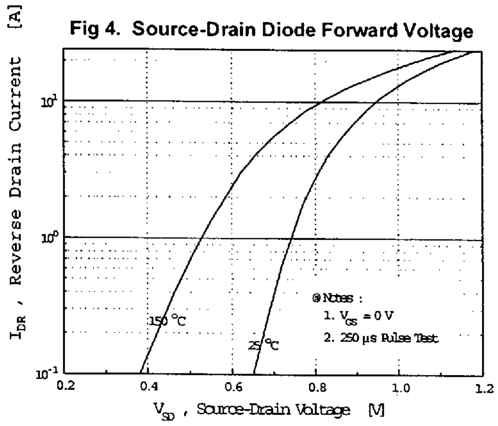


Fig 5. Capacitance vs. Drain-Source Voltage

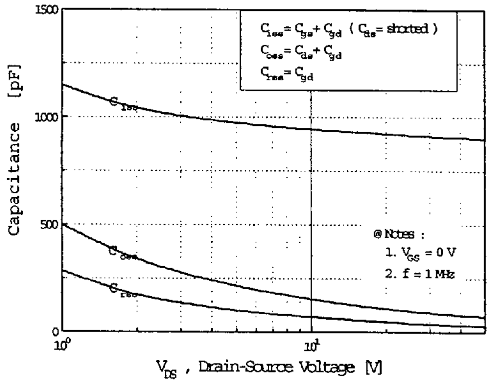


Fig 6. Gate Charge vs. Gate-Source Voltage

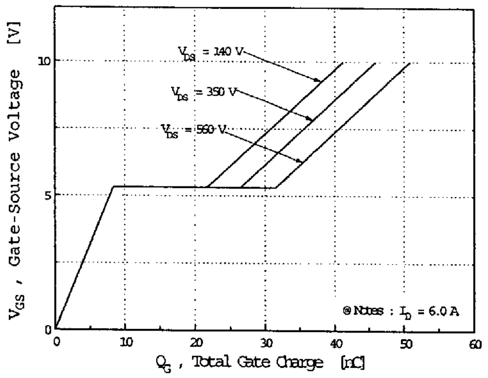


Fig 7. Breakdown Voltage vs. Temperature

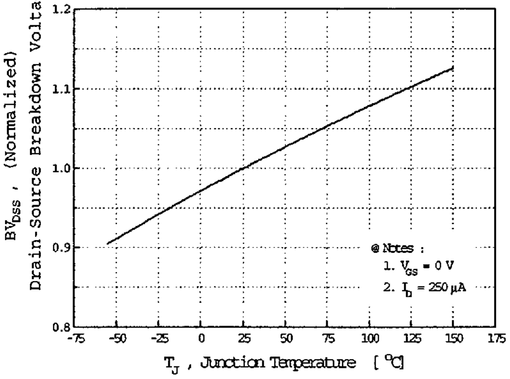


Fig 8. On-Resistance vs. Temperature

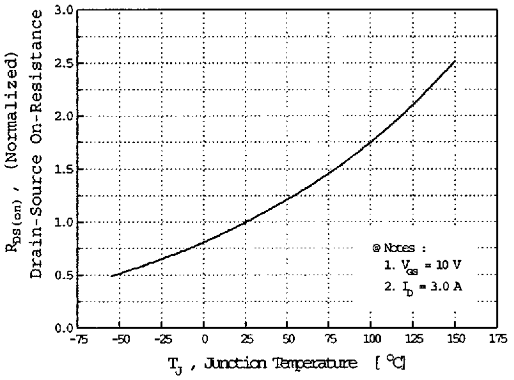


Fig 9. Max. Safe Operating Area

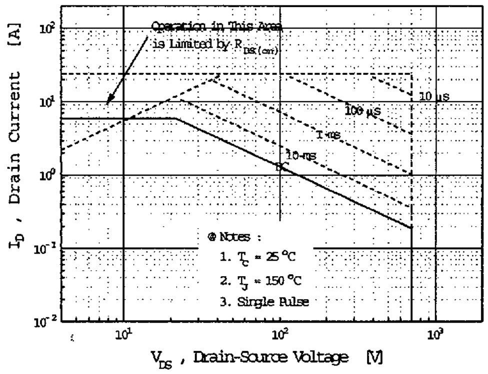


Fig 10. Max. Drain Current vs. Case Temperature

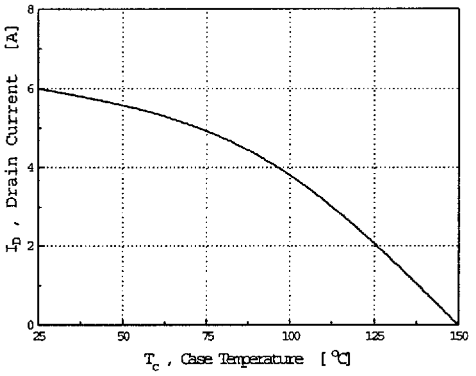
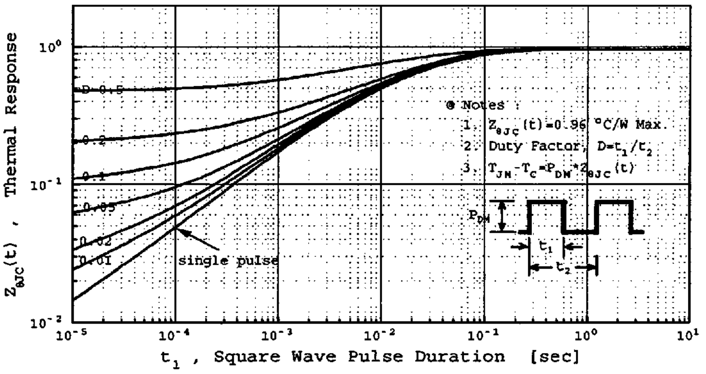


Fig 11. Thermal Response



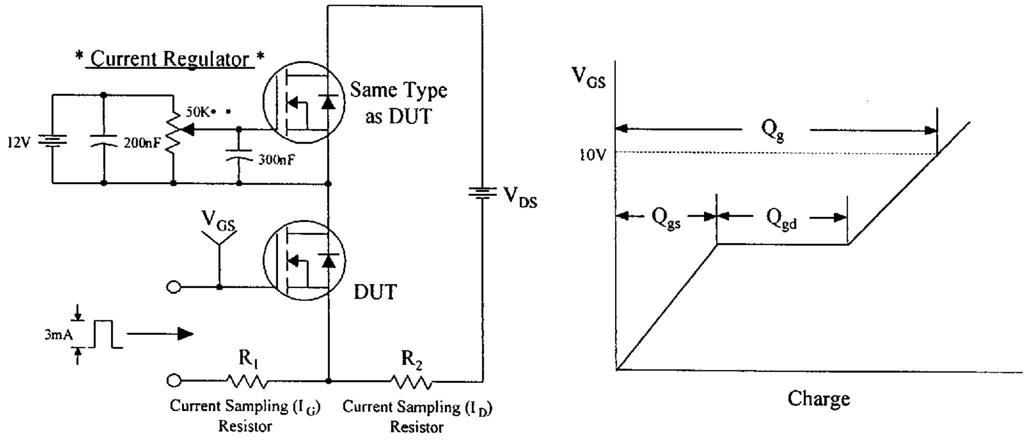


Fig 12. Gate Charge Test Circuit & Waveform

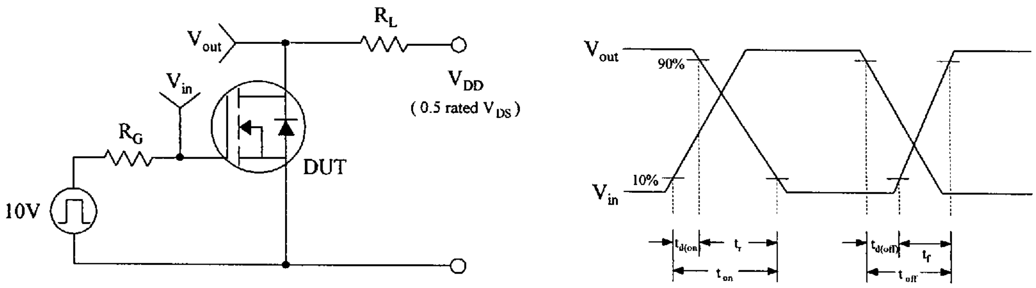


Fig 13. Resistive Switching Test Circuit & Waveforms

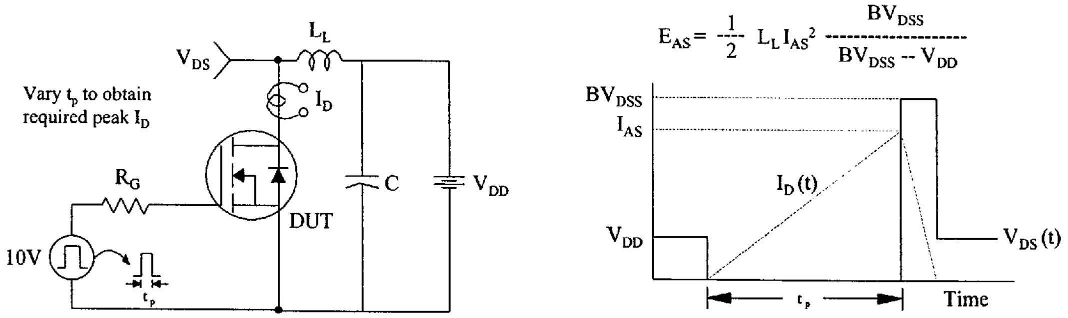
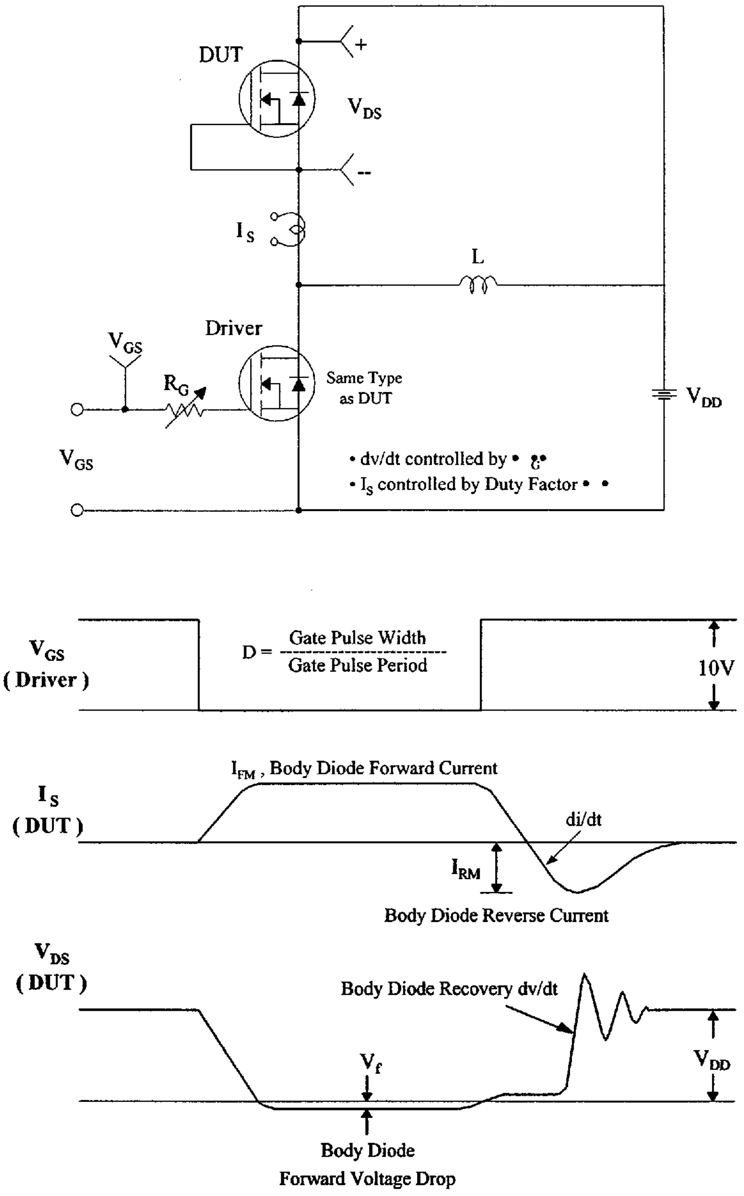


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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