1 PRODUCT OVERVIEW

SAM87RI PRODUCT FAMILY

Samsung's SAM87RI family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes.

A dual address/data bus architecture and a large number of bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations. Many SAM87RI microcontrollers have an external interface that provides access to external memory and other peripheral devices.

S3C9004/P9004/C9014/P9014 MICROCONTROLLER

The S3C9004/P9004/C9014/P9014 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87RI CPU core.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The S3C9004/P9004/C9014/P9014 has 4 K bytes of program memory on-chip.

Using the SAM87RI design approach, the following peripherals were integrated with the SAM87RI core:

— Five configurable I/O ports (32 pins)

— 12 bit-programmable pins for external interrupts

— 8-bit timer/counter with three operating modes

The S3C9004/P9004/C9014/P9014 is a versatile microcontroller that can be used in a wide range of general purpose applications. It is especially suitable for use as a keyboard controller and is available in a 40-pin DIP and a 44-pin QFP package.

OTP

The S3C9004/C9014 microcontroller is also available in OTP (One Time Programmable) version, S3P9004/P9014. S3P9004/P9014 microcontroller has an on-chip 8-Kbyte one-time-programmable EPROM instead of masked ROM. The S3P9004/P9014 is comparable to S3C9004/C9014, both in function and in pin configuration.

FEATURES

CPU

- SAM87RI CPU core

Memory

- 4-Kbyte internal program memory (ROM)
- 208-byte internal register file
- 8-Kbyte external program memory
- 8-Kbyte external data memory

Instruction Set

- 41 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 1.5 µs at 4 MHz f_{OSC}

Interrupts

- 14 interrupt sources with one vector, Each source has its pending bit
- One level, one vector interrupt structure

Oscillation Circuit Options

- 4 MHz RC oscillator with on chip capacitor for **S3C9004/P9004** (–10% RC accuracy at V_{DD} ± 5% and Ta = 0°C–70°C, using 1% external precision resistor)
- RC oscillator for **S3C9004/P9004**
- Crystal/ceramic oscillator for **S3C9014/P9014**

General I/O

- Five ports (32 pins total)
- Three bit-programmable ports (20 pins total)
- Two bit-programmable ports with external interrupts (12 pins total)

Timer/Counter

- One 8-bit basic timer for watchdog function and programmable oscillation stabilization interval generation function
- One 8-bit timer/counter with PWM mode

Operating Temperature Range

- – 40°C to + 85°C

Operating Voltage Range

- 4.5 V to 5.5 V for S3C9004/P9004
- 2.7 V to 5.5 V for S3C9014/P9014

Package Types

- 40-pin DIP

BLOCK DIAGRAM

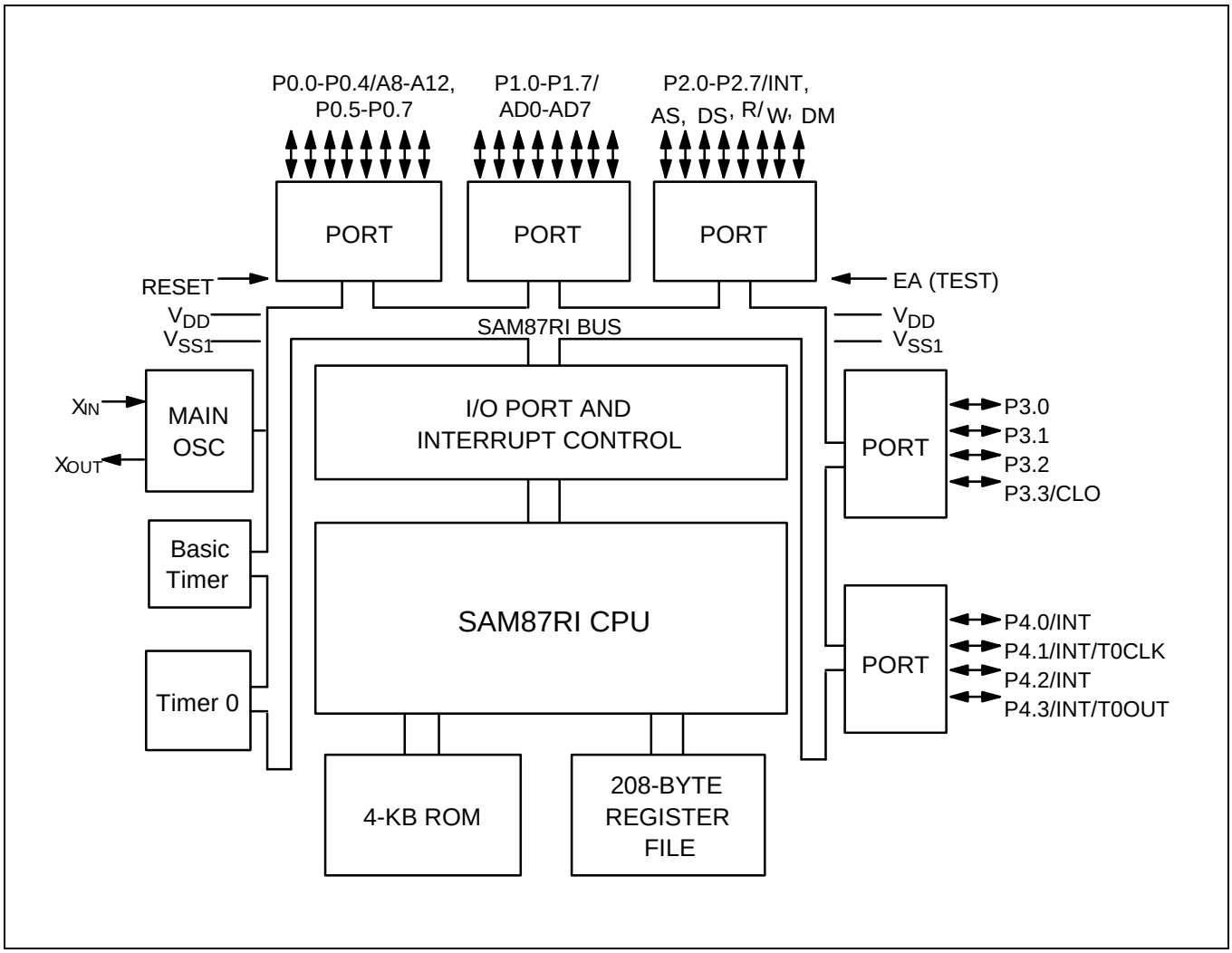


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

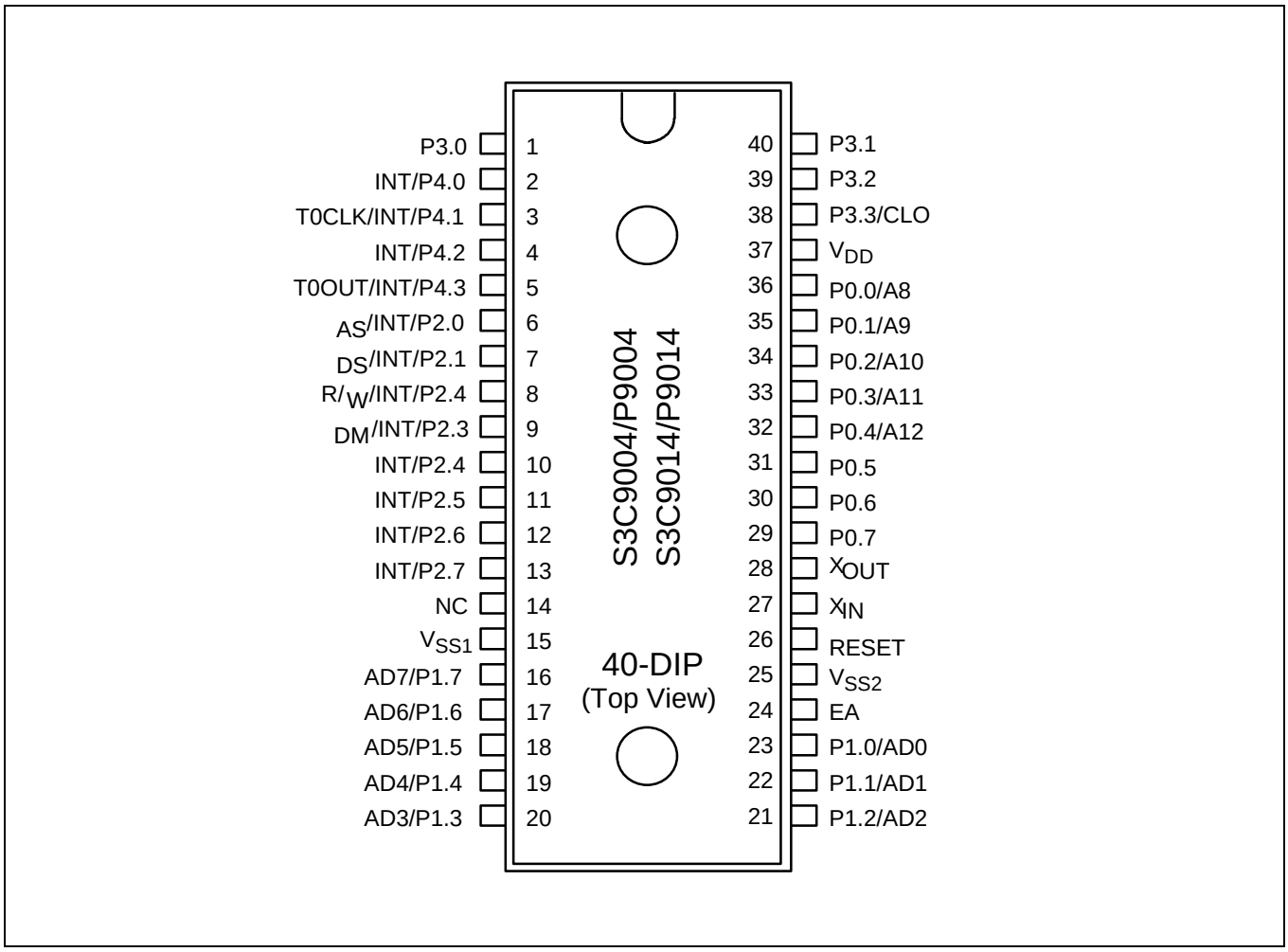


Figure 1-2. Pin Assignment Diagram (40-Pin DIP Package)

PIN DESCRIPTIONS

Table 1-1. S3C9004/P9004/C9014/P9014 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Number	Pin Numbers	Share Pins
P0.0-P0.7	I/O	Bit-programmable I/O port for Schmitt trigger input or open-drain output. Port0 can also be configured as external interface address lines A8-A12.	C	36-29	A8-A12
P1.0-P1.7	I/O	Bit-programmable I/O port for Schmitt trigger input, push-pull, or open-drain output. Port1 can alternatively be used as external interface address/data lines AD0-AD7.	C	23-16	AD0-AD7
P2.0-P2.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Port2 can be individually configured as external interrupt inputs. Especially, P2.0-2.3 can be configured for external bus control signal.	D	6-13	INT, AS, DS, R/W, DM
P3.0-P3.3	I/O	Same general characteristics as Port1. Port3 are designed for to drive LED directly. P3.3 can be used to system clock output (CLO) port.	C	1, 40-38	P3.3/CLO
P4.0-P4.3	I/O	Bit-programmable I/O port. Input mode or n-channel open-drain output mode is software assignable. Port4 can be individually configured as external interrupt inputs. Pull-up resistors are also software assignable. Especially, P4.1 can be used T0CLK input and P4.3 also T0OUT for Timer 0.	D	2-5	INT, T0CLK, T0OUT
X_{IN}, X_{OUT}	–	System clock input and output pin (for RC oscillator, crystal/ceramic oscillator, or external clock source)	–	27, 28	–
INT	I	External interrupt for bit-programmable port2 and port4 pins when set to input mode.	–	2-13	PORT2/ PORT4
RESET	I	RESET signal input pin. Schmitt trigger input with internal pull-up resistor.	A	26	–
EA	I	External Memory Access (EA) pin with 2 modes: 0V = Normal Operation Mode 5V = ROMLESS Operation Mode (Must be connected to V_{SS} during normal operation mode)	B	24	–
V_{DD}	–	Power input pin	–	37	–
V_{SS1}, V_{SS2}	–	Vss1 is a ground power for CPU core. Vss2 is a ground power for I/O and OSC block	–	15, 25	–
NC	–	No connection (This pin would be better connecting to V_{SS})	–	14	–

PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the S3C9004/P9004/C9014/P9014

Circuit Number	Circuit Type	S3C9004/P9004/C9014/P9014 Assignments
A	I	RESET signal input
B	I	EA input
C	I/O	Ports 0, 1, and 3
D	I/O	Ports 2 and 4

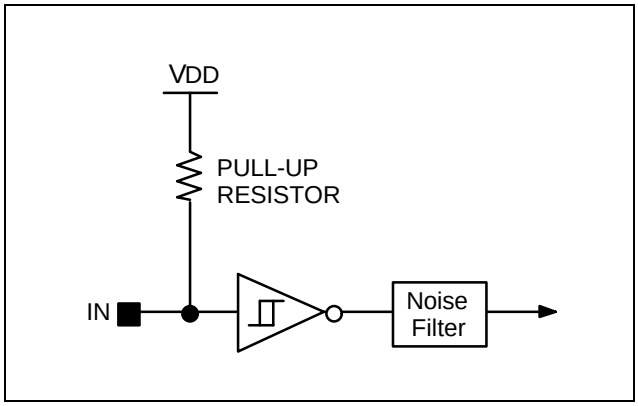


Figure 1-3. Pin Circuit Type A (RESET)

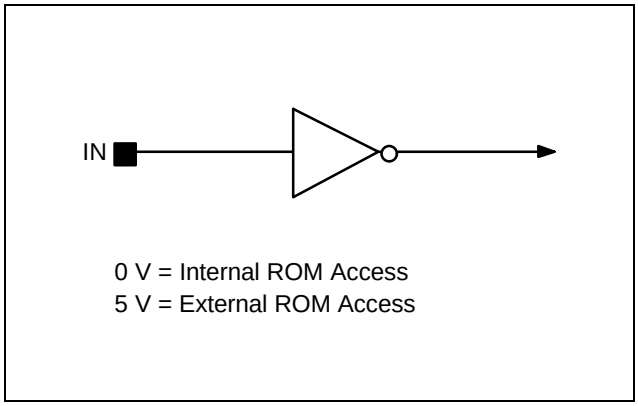
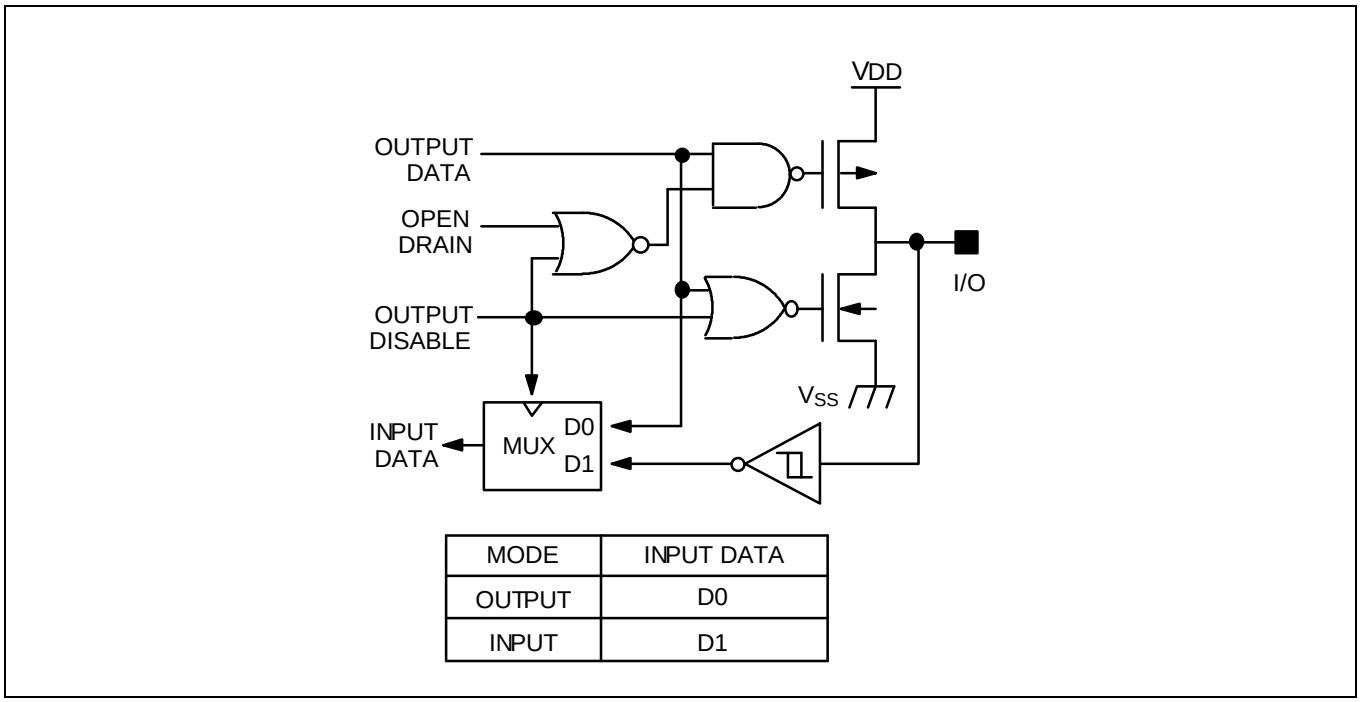
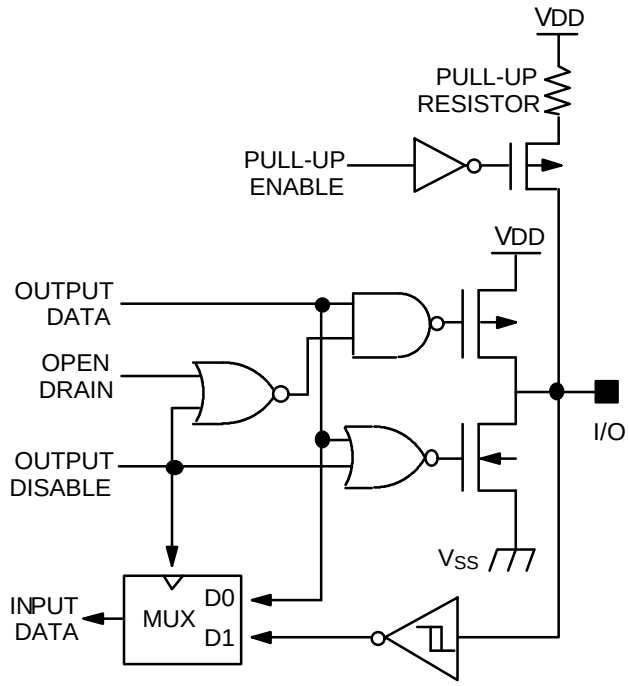


Figure 1-4. Pin Circuit Type B (EA)



MODE	INPUT DATA
OUTPUT	D0
INPUT	D1

Figure 1-5. Pin Circuit Type C (Ports 0, 1, and 3)



MODE	INPUT DATA
OUTPUT	D0
INPUT	D1

Figure 1-6. Pin Circuit Type D (Ports 2 and 4)

APPLICATION CIRCUIT

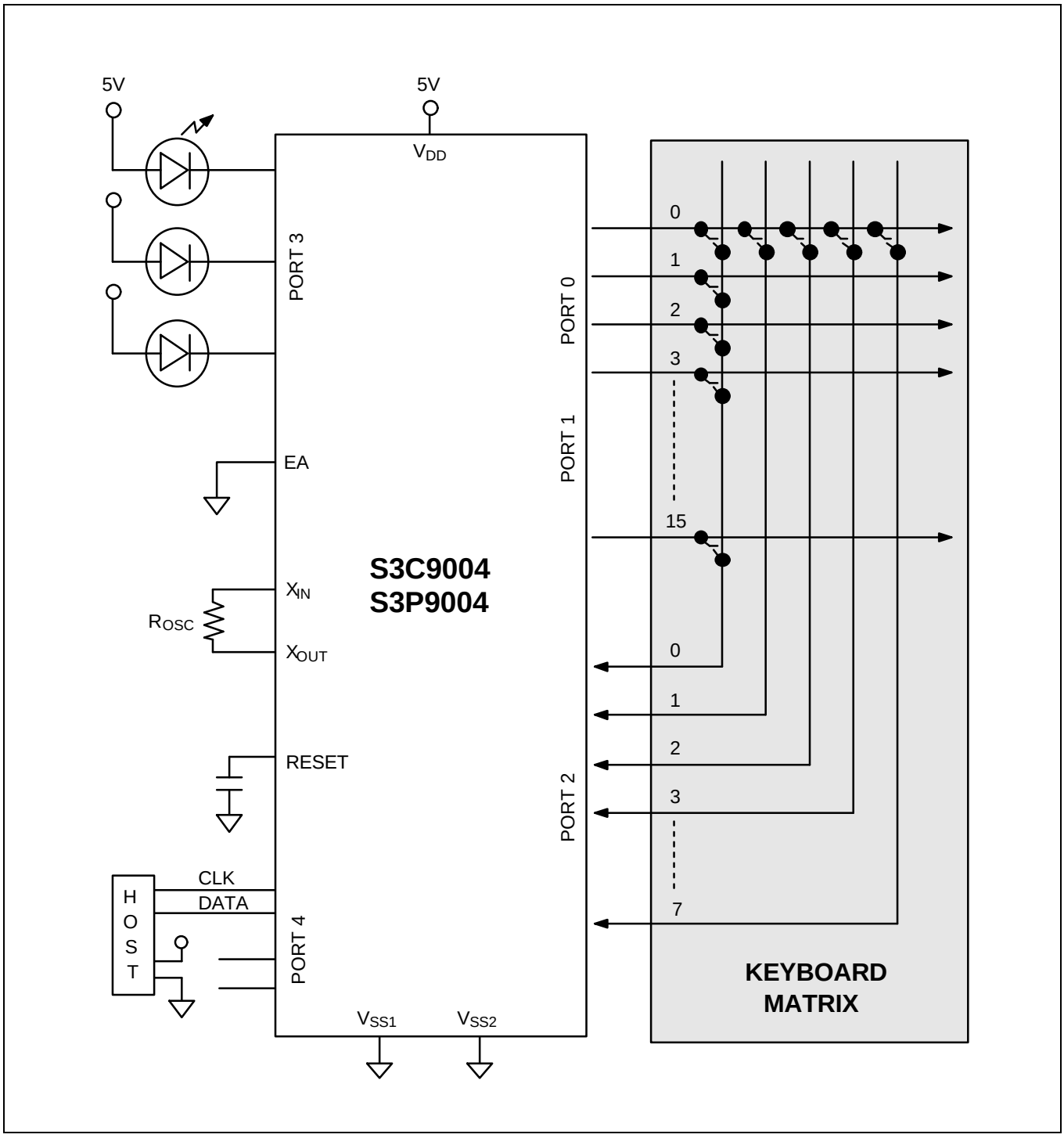


Figure 1-7. Keyboard Control Application Circuit Diagram

12 ELECTRICAL DATA

OVERVIEW

In this section, the following S3C9004/P9004/C9014/P9014 electrical characteristics are presented in tables and graphs:

— Absolute maximum ratings
— D.C. electrical characteristics
— I/O capacitance
— A.C. electrical characteristics
— Input timing for RESET
— Input timing for external interrupts (ports 2 and 4, RESET, and EA)
— Oscillator characteristics
— Oscillation stabilization time
— Clock timing measurement points at X_{IN}
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by a reset
— Stop mode release timing when initiated by an external interrupt
— External Memory timing characteristics (8 MHz)
— External Memory Read and Write timing
— Characteristic curves

Table 12-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{IN}	All input ports	– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_O	All output ports	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output Current Low	I_{OL}	One I/O pin active	+ 25	mA
		Total pin current for ports 3	+ 100	
		Total pin current for ports 0, 1, 2, 4	+ 100	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{STG}	–	– 65 to + 150	°C

Table 12-2. D.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 4.5 V to 5.5 V [1])

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High Voltage	V_{IH1}	All inputs except V_{IH2}	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN}	V_{DD} – 0.5		V_{DD}	
Input Low Voltage	V_{IL1}	All inputs except V_{IL2}		–	0.2 V_{DD}	V
	V_{IL2}	X_{IN}			0.4	
Output High Voltage	V_{OH}	I_{OH} = – 200 µA All outputs except P4.1, P4.3, and port0	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA All outputs except port3	–	–	0.4	V
Output Low Current	I_{OL}	V_{OL}= 3 V Port3 only	8	15	23	mA
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All inputs except I_{LIH2}, P4.0 and P4.1	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, X_{OUT}			20	

Table 12-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40°C to + 85°C, V_{DD} = 4.5 V to 5.5 V (1))

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All inputs except I_{LIL2}, P4.0 and P4.1	–	–	– 3	µA
	I_{LIL2}	V_{IN} = 0 V X_{OUT}, X_{IN}			– 20	
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{DD} All outputs	–	–	3	µA
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0 V All outputs	–	–	– 3	µA
Pull-up Resistors	R_{L1}	V_{IN} = 0 V; Port 2 only	30	60	90	KΩ
	R_{L2}	V_{IN} = 0 V; Port 4 only	1.8	2.8	4.0	
	R_{L3}	V_{IN} = 0 V; RESET only	50	90	150	
Supply Current (2)	I_{DD1}	Normal operation mode 4 MHz CPU clock	–	4.5	10	mA
	I_{DD2}	Idle mode; 4 MHz oscillator		0.9	3	mA
	I_{DD3}	Stop mode		0.5	5	µA

NOTES:

1. The operating voltage range of S3C9014/P9014 is from 2.7 V to 5.5 V according to oscillation frequency.
2. Supply current does not include current drawn through internal pull-up resistors or external output current loads.

Table 12-3. Input/Output Capacitance

(T_A = – 40°C to + 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 12-4. A.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 4.5 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Interrupt Input High, Low Width	t_{INTH}, t_{INTL}	P2 and P4	–	200	–	ns
RESET Input Low Width	t_{RSL}	RESET	–	1,000	–	

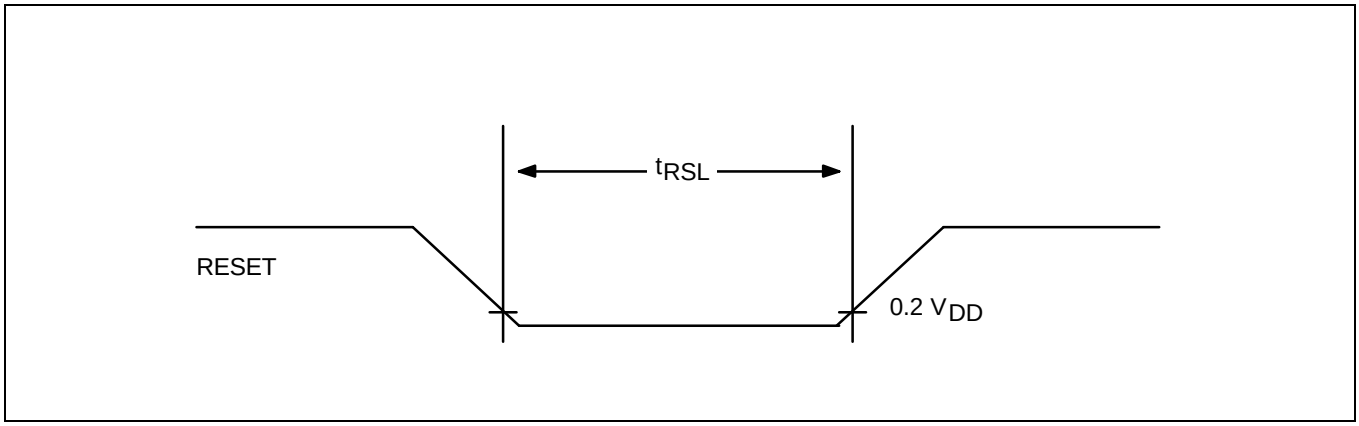


Figure 12-1. Input Timing for RESET

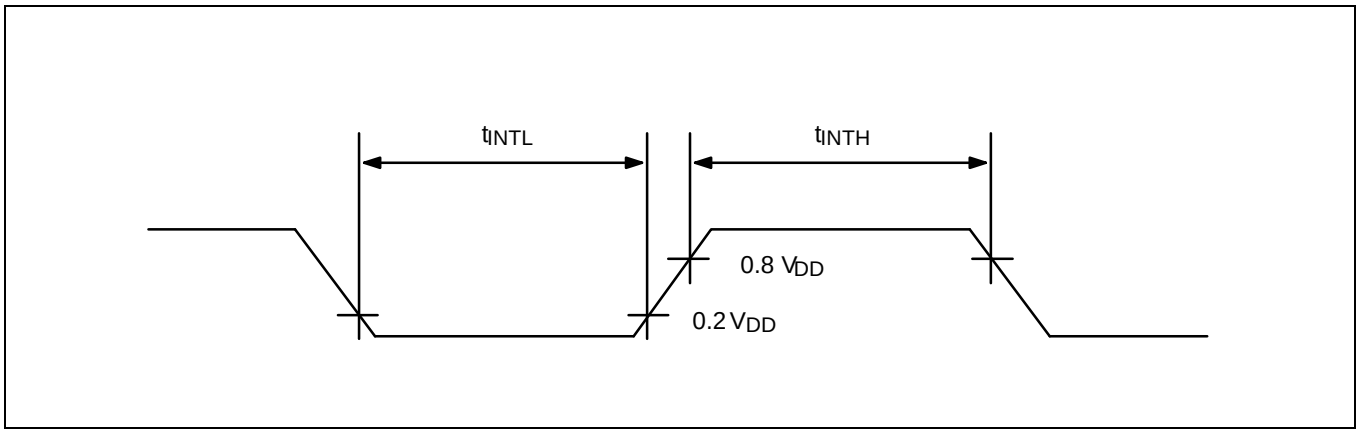
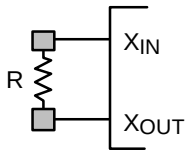
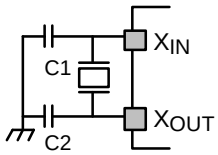


Figure 12-2. Input Timing Measurement Points for Port 2, Port 4, and RESET

Table 12-5. Oscillator Characteristics

(T_A = – 40°C + 85°C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
RC Oscillator (with Internal Capacitor; **for S3C9004/P9004**)		V_{DD} = 4.75 to 5.25 V TA = 0°C + 70°C Tolerance: ± 10% (note)	–	4	–	MHz
Crystal/Ceramic Oscillator (**for S3C9014/P9014**)		Crystal/Ceramic oscillation frequency	1.0	–	8.0	

NOTE: The S3C9004/P9004 provides an internal capacitor to accommodate an RC oscillator configuration. A 1% precision resistor must be used to achieve an oscillation frequency with an acceptable tolerance.

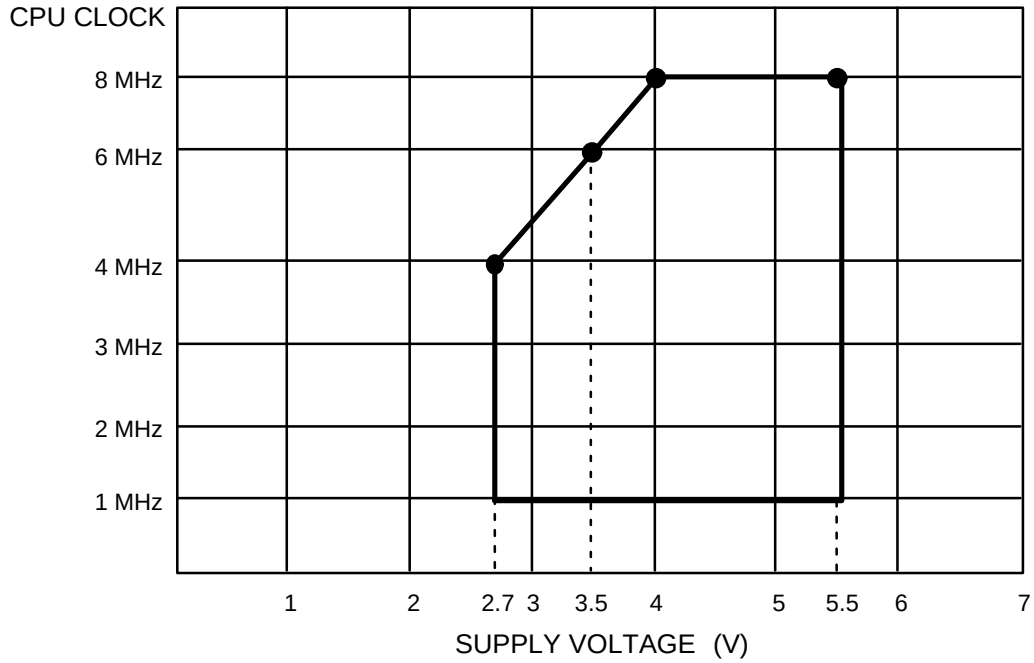


Figure 12-3. Operating Voltage Range (S3C9014/P9014)

Table 12-6. Oscillation Stabilization Time

(T_A = – 40°C + 85°C, V_{DD} = 4.5 V to 5.5 V)

Oscillator	Test Condition	Min	Typ	Max	Unit
Main Crystal Main Ceramic	f_{OSC} = 4 MHz (Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.)	–	–	10	ms
Oscillator Stabilization Wait Time	t_{WAIT} stop mode release time by a reset	–	2^{16} / f_{OSC}	–	
	t_{WAIT} stop mode release time by an interrupt	–	(note)	–	

NOTE: The oscillator stabilization wait time, t_{WAIT}, is determined by the setting in the basic timer control register, BTCON.

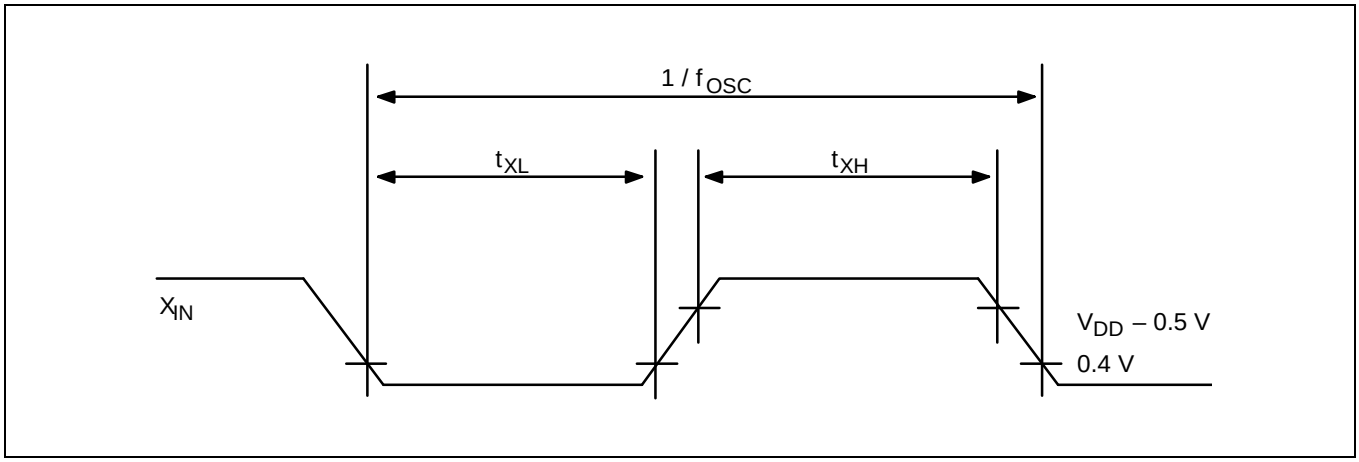


Figure 12-4. Clock Timing Measurement Points at X_{IN}

Table 12-7. Data Retention Supply Voltage in Stop Mode

(T_A = – 40°C + 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}	Stop mode	2.0	–	6	V
Data Retention Supply Current	I_{DDDR}	Stop mode; V_{DDDR} = 2.0 V	–	–	5	µA

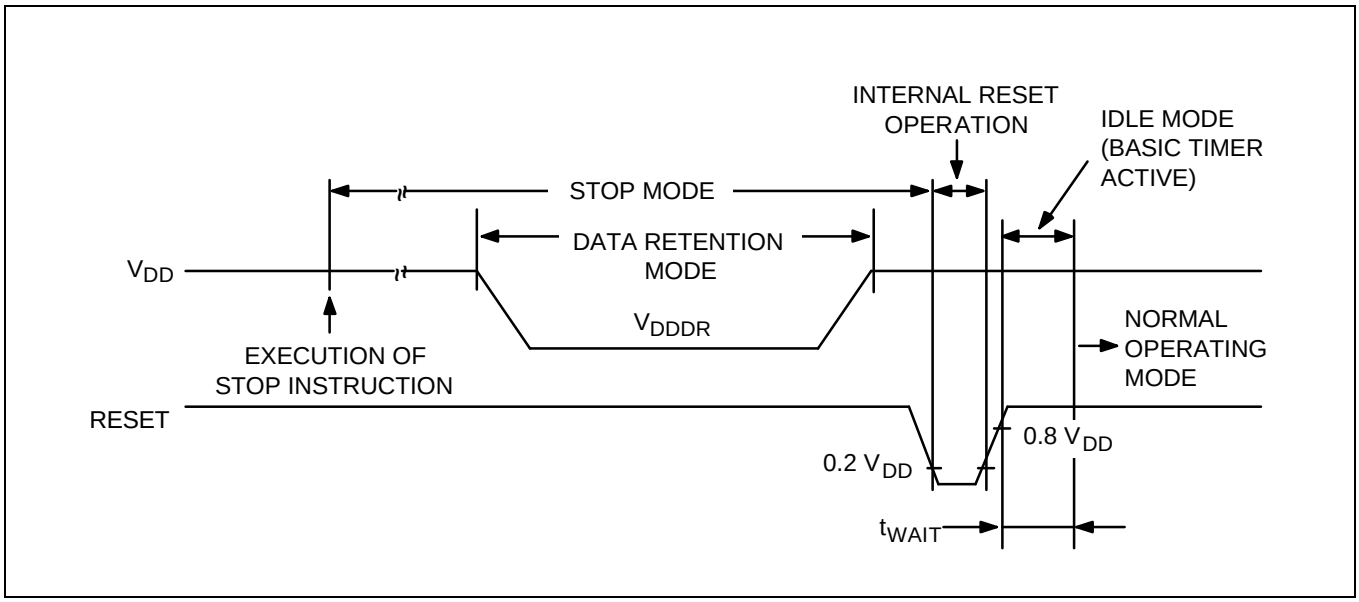


Figure 12-5. Stop Mode Release Timing When Initiated by a Reset

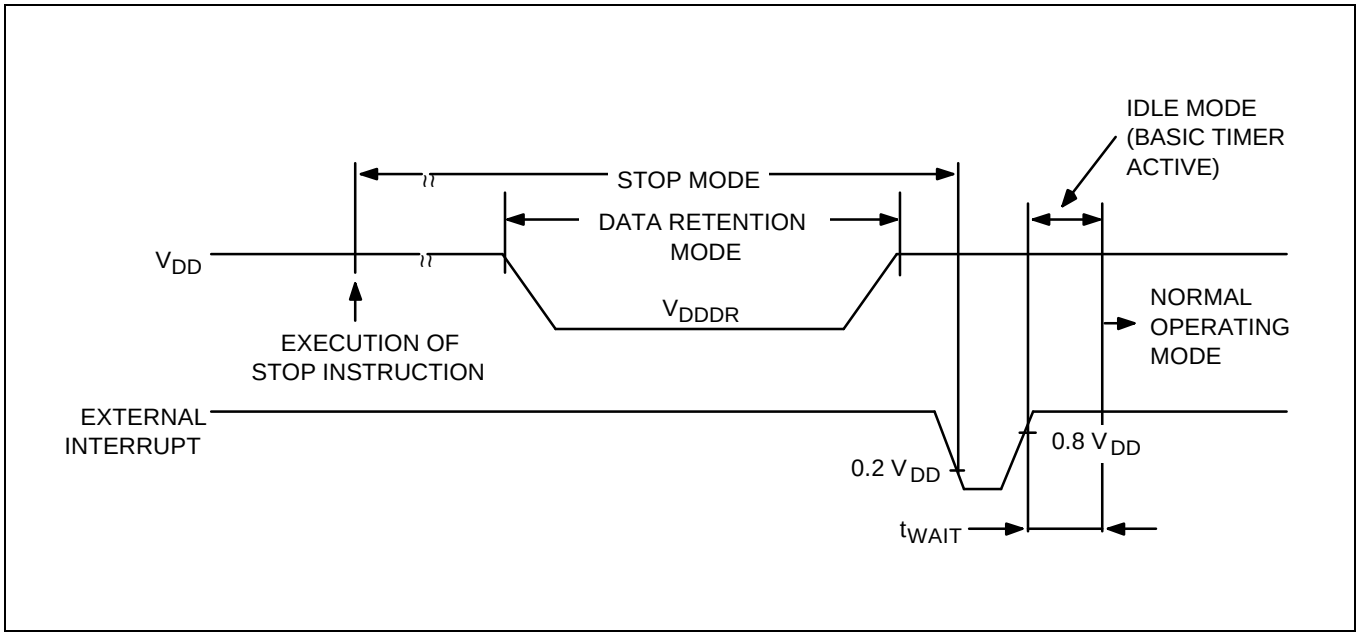


Figure 12-6. Stop Mode Release Timing When Initiated by an External Interrupt

Table 12-8. External Memory Timing Characteristics (4 MHz)

(T_A = – 40°C to + 85°C, V_{DD} = 4.5 V to 5.5 V)

Number	Symbol	Parameter	Normal Timing (ns)	
			Min	Max
1	t_{dA} (AS)	Address valid to AS ↑ delay	10	–
2	t_{dAS} (A)	AS ↑ to address float delay	35	–
3	t_{dAS} (DR)	AS ↑ to read data required valid	–	140
4	t_{wAS}	AS Low width	88	–
5	t_{dA} (DS)	Address float to DS ↓	0	–
6a	t_{wDS} (read)	DS (read) Low width	314	–
6b	t_{wDS} (write)	DS (write) Low width	164	–
7	t_{dDS} (DR)	DS ↓ to read data required valid	–	80
8	t_{hDS} (DR)	Read data to DS ↑ hold time	0	–
9	t_{dDS} (A)	DS ↑ to address active delay	20	–
10	t_{dDS} (AS)	DS ↑ to AS ↓ delay	30	–
11	t_{dDO} (DS)	Write data valid to DS (write) ↓ delay	10	–
12	t_{dRW} (AS)	R/W valid to AS ↑ delay	20	–
13	t_{dDS} (DW)	DS ↑ to write data not valid delay	20	–

NOTES:

1. All times are in nano seconds (ns) and assume an 4 MHz input frequency.
2. Wait states add 100 ns to the time of numbers 3, 6a, 6b, and 7.

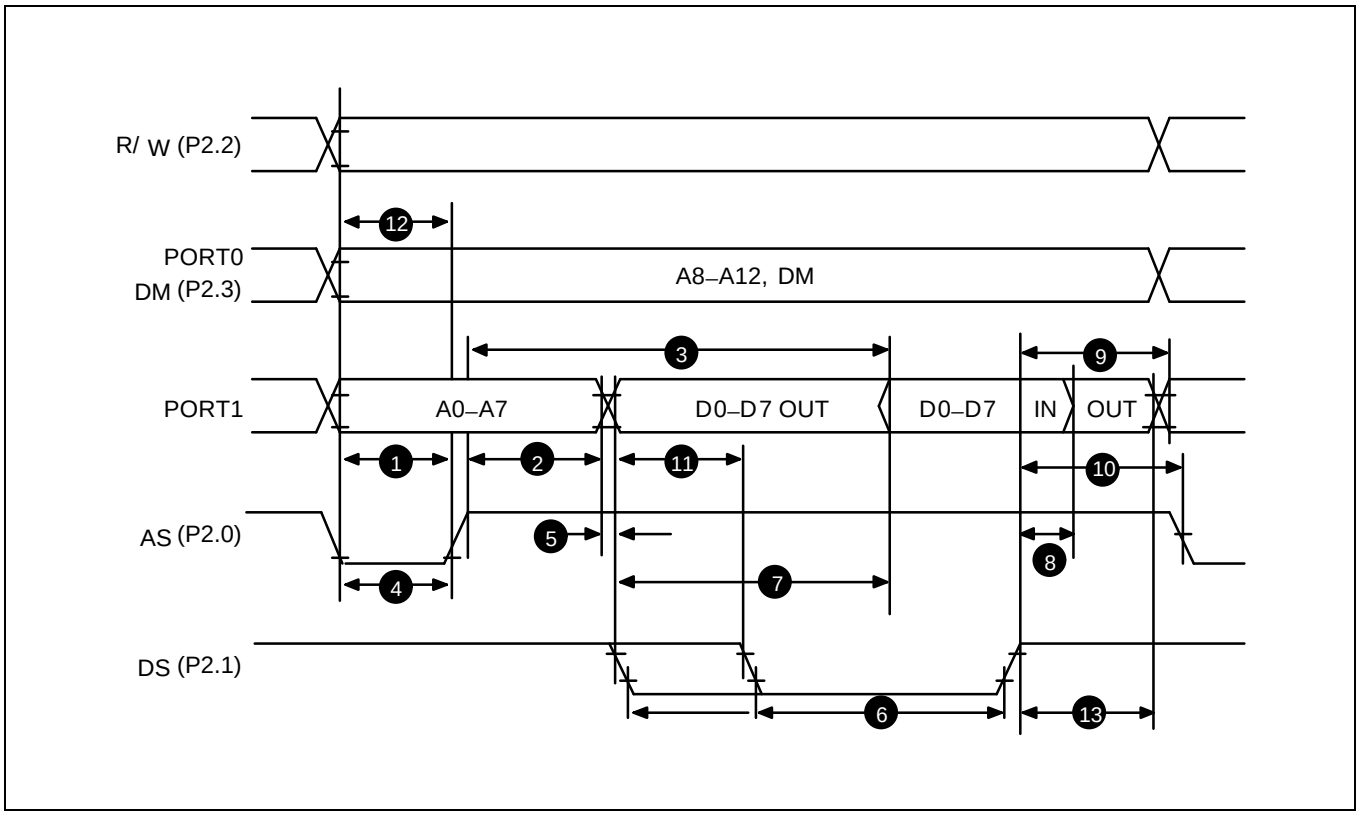


Figure 12-7. External Memory Read and Write Timing

(See Table 12-8 for a description of each timing point.)

CHARACTERISTIC CURVES

NOTE

The characteristic values shown in the following graphs are based on actual test measurements. They do not, however, represent guaranteed operating values.

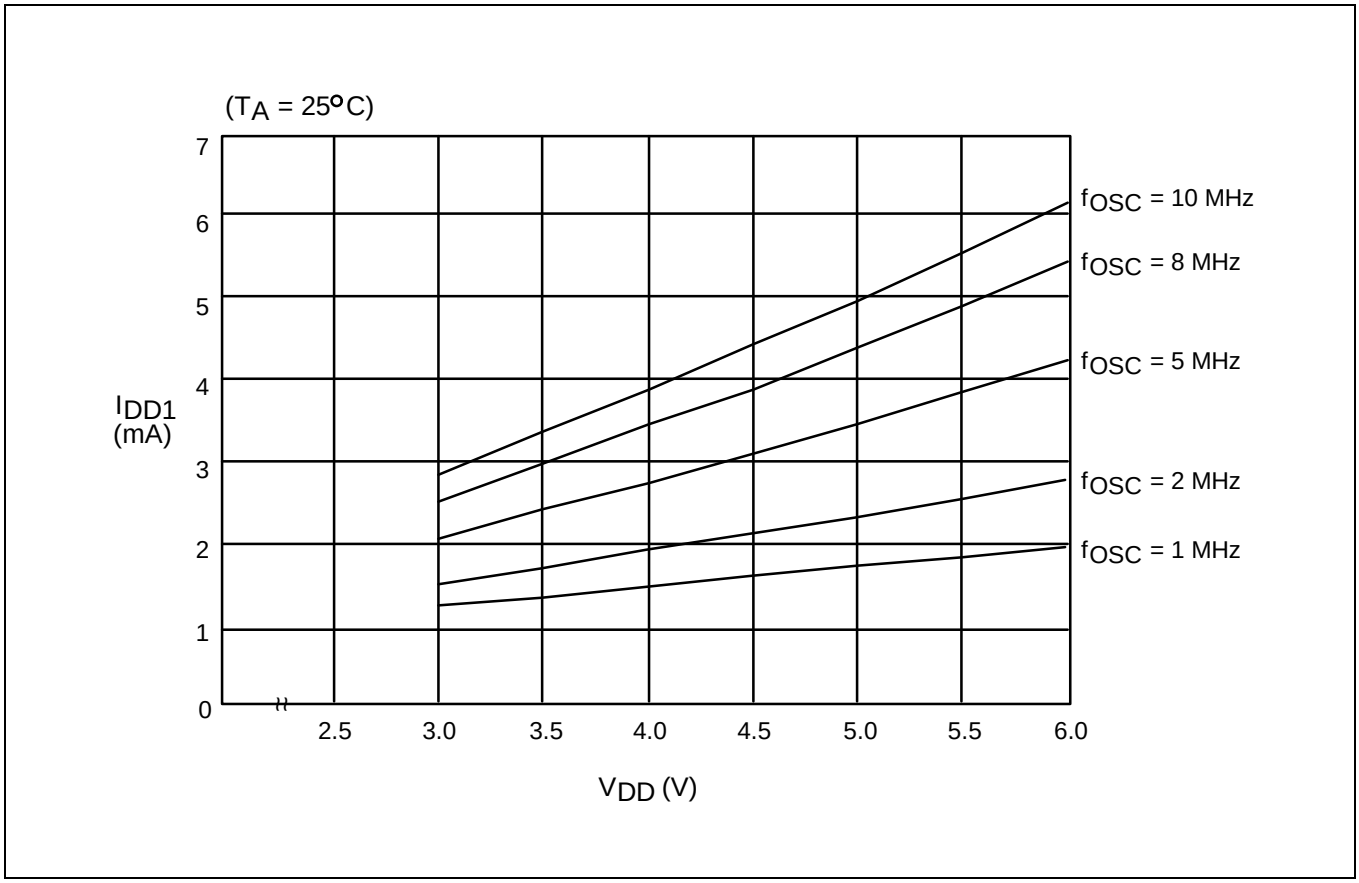


Figure 12-8. I_{DD1} vs. V_{DD}

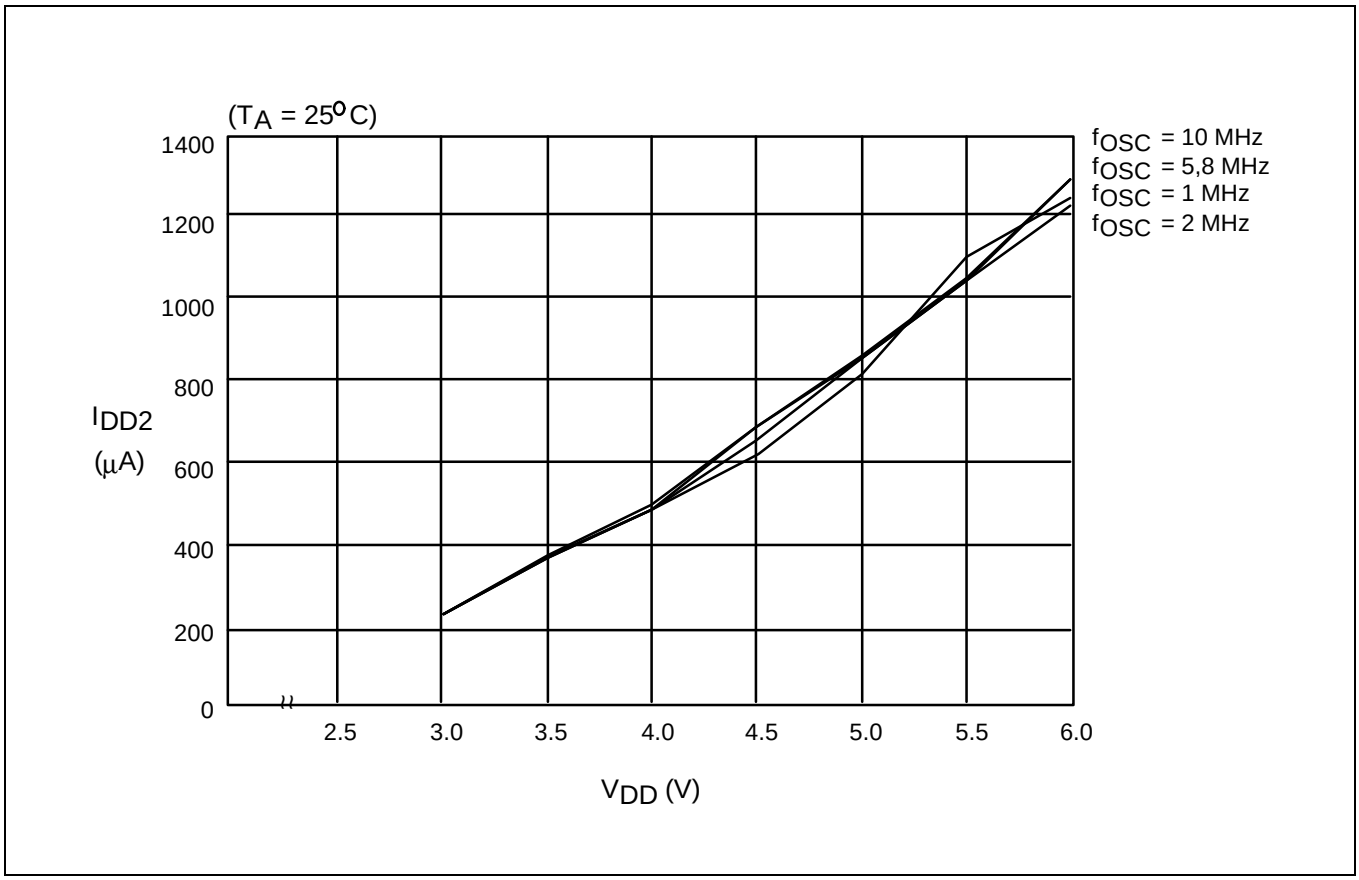


Figure 12-9. I_{DD2} vs. V_{DD}

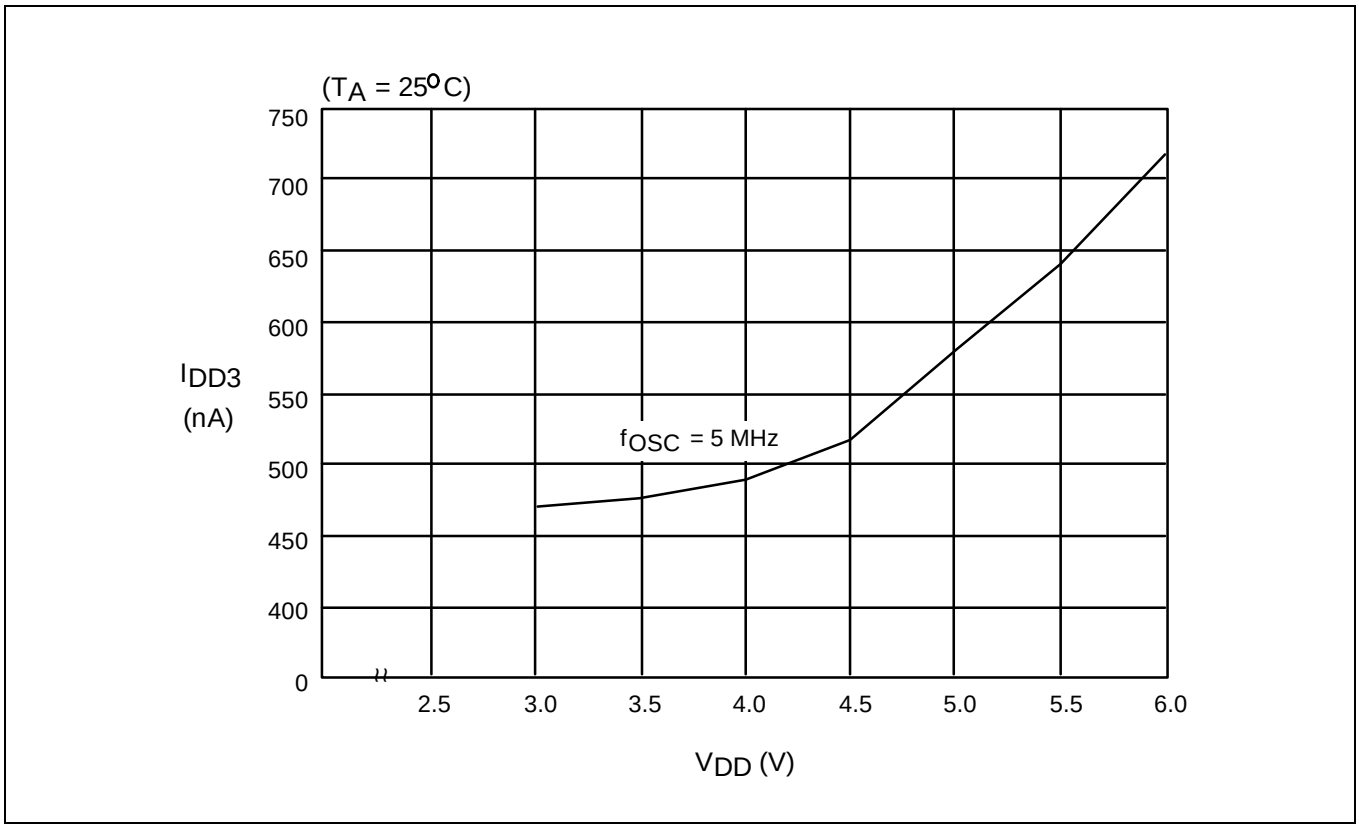


Figure 12-10. I_{DD3} vs. V_{DD}

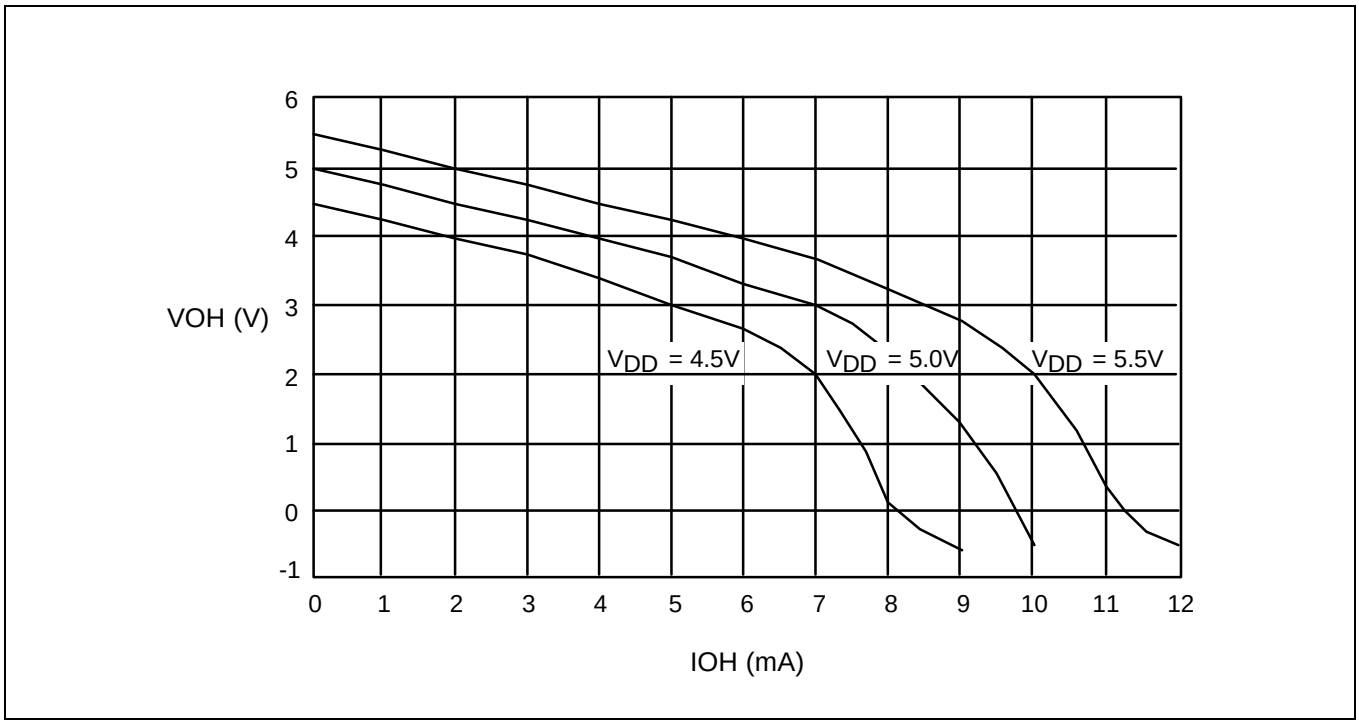


Figure 12-11. I_{OH} vs. V_{OH}

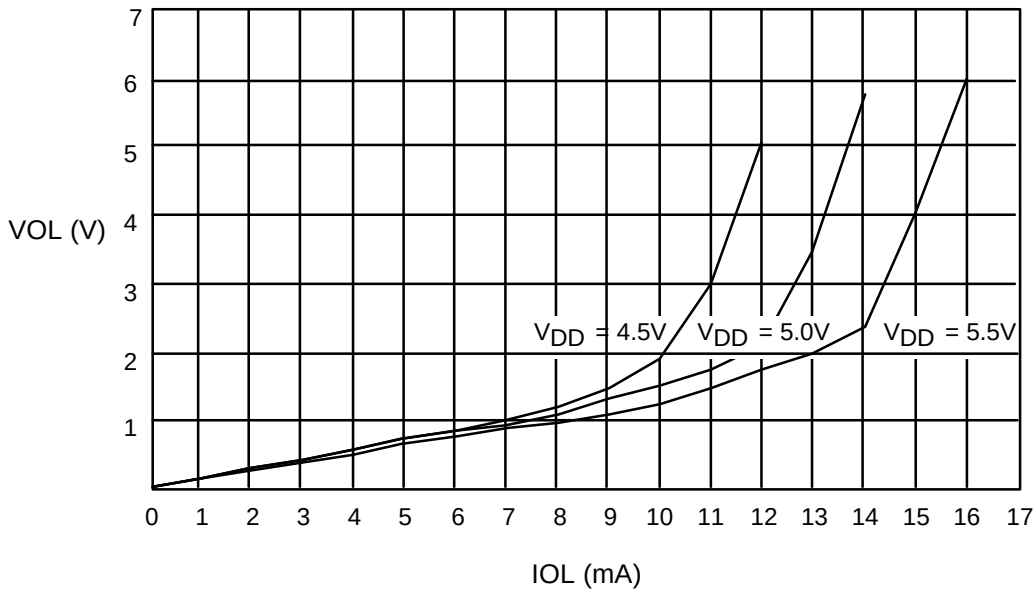


Figure 12-12. V_{OL} vs. I_{OL} (Port 0, 1, 2, and 4)

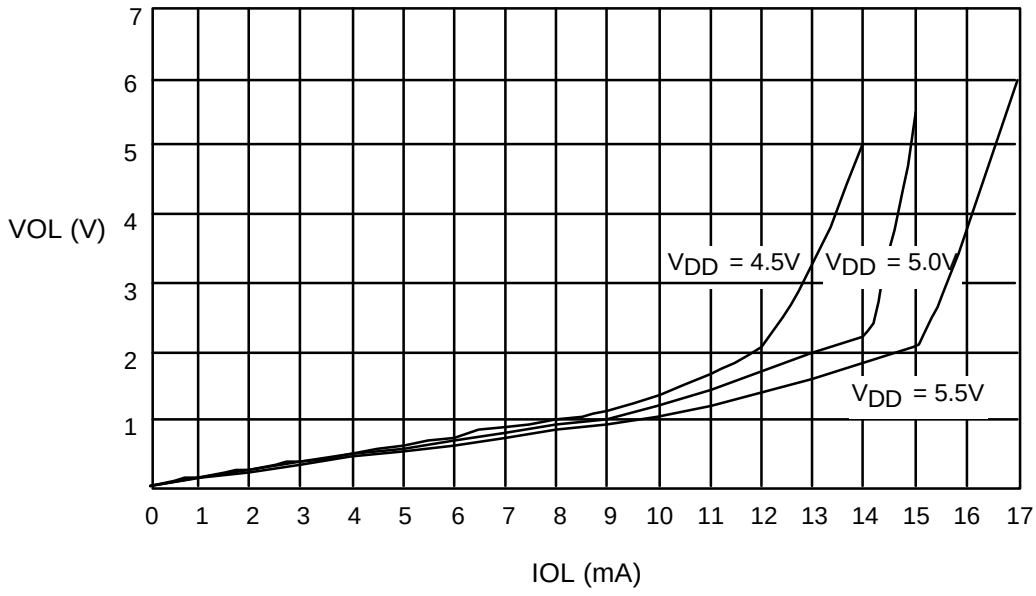
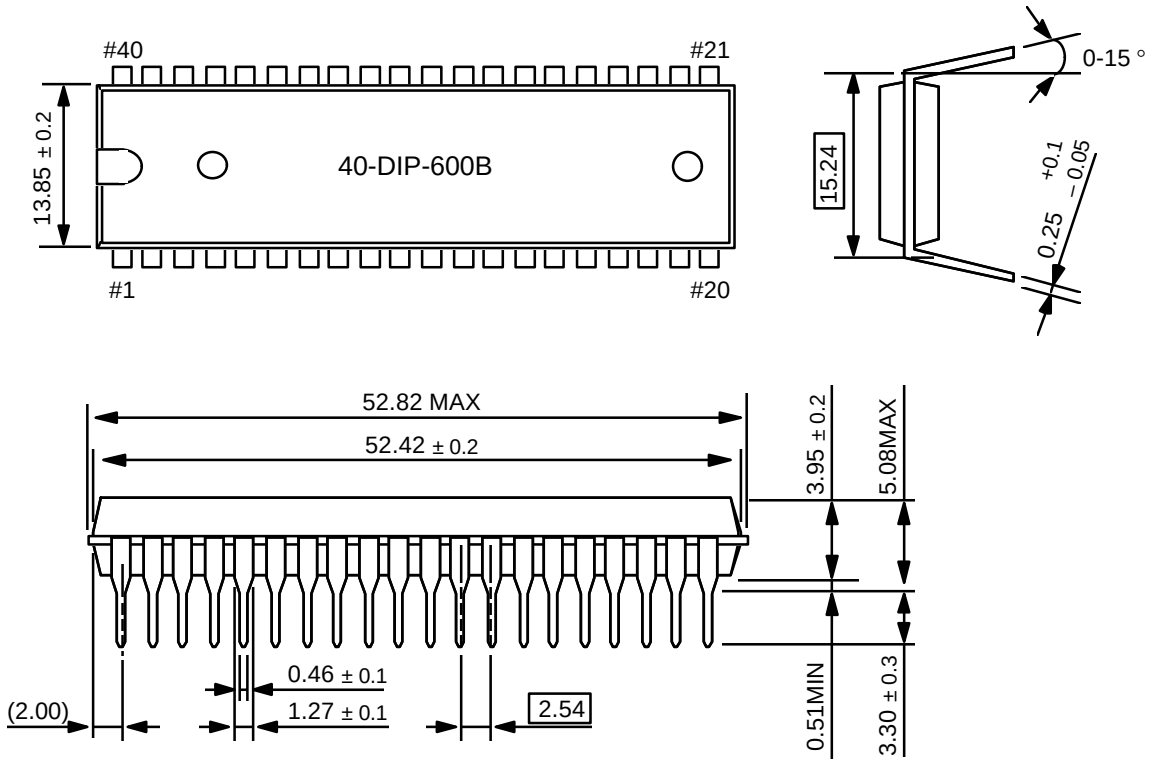


Figure 12-13. V_{OL} vs. I_{OL} (Port 3)

13 MECHANICAL DATA

OVERVIEW

The S3C9004/P9004/C9014/P9014 is currently available in a 40-pin DIP package.



NOTE: Dimensions are in millimeters.

Figure 13-1. 40-Pin DIP Package Mechanical Data (40-DIP-600B)

NOTES