1G- 128Mx64 DDR SDRAM UNBUFFERED

FEATURES

- Clock speeds of 100MHz and 133MHz
- Double-data-rate architecture
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2,5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect
- Power Supply: 2.5V ± 0.20V
- JEDEC standard 184 pin DIMM package

DESCRIPTION

The W3EG64129S is a 124Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM component. The module consists of sixteen 128Mx4 DDR SDRAMs in 66 pin TSOP package mounted on a 184 Pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lenths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change without notice.

OPERATING FREQUENCIES

	DDR266 @CL=2	DDR266 @CL=2.5	DDR200 @CL=2
Clock Speed	133MHz	133MHz	100MHz
CL-t_{RCD}-t_{RP}	2-2-2	2.5-3-3	2-2-2

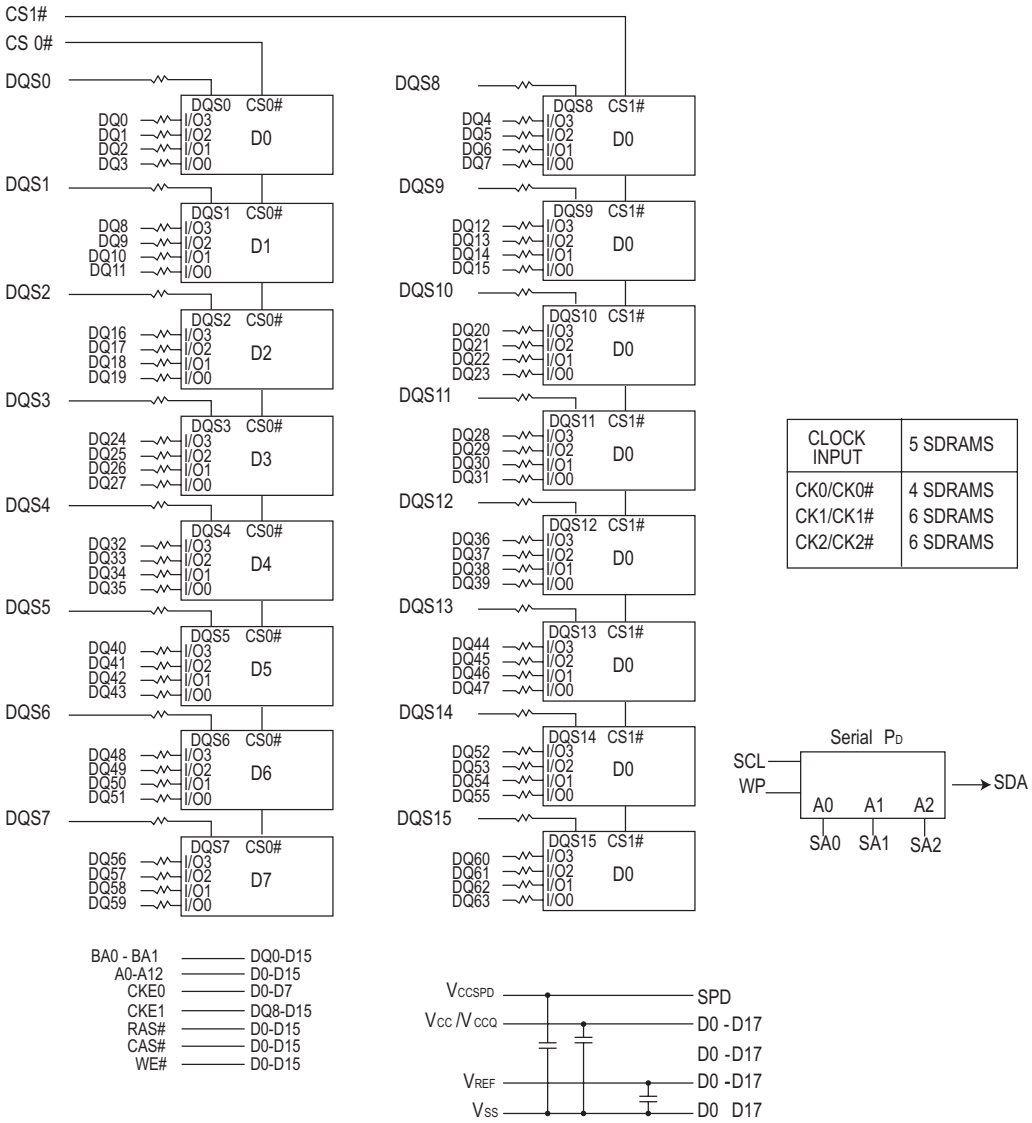
PIN CONFIGURATION

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V_{REF}	47	NC	93	V_{SS}	139	V_{SS}
2	DQ0	48	A0	94	DQ4	140	NC
3	V_{SS}	49	NC	95	DQ5	141	A10
4	DQ1	50	V_{SS}	96	V_{CCQ}	142	NC
5	DQS0	51	NC	97	DQS9	143	V_{CCQ}
6	DQ2	52	BA1	98	DQ6	144	NC
7	V_{CC}	53	DQ32	99	DQ7	145	V_{SS}
8	DQ3	54	V_{CCQ}	100	V_{SS}	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	V_{CC}
11	V_{SS}	57	DQ34	103	NC	149	DQS13
12	DQ8	56	V_{SS}	104	V_{CCQ}	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	V_{SS}
15	V_{CCQ}	61	DQ40	107	DQS10	153	DQ44
16	CK1	62	V_{CCQ}	108	V_{CC}	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	V_{SS}	64	DQ41	110	DQ15	156	V_{CCQ}
19	DQ10	65	CAS#	111	CKE1	157	CS0#
20	DQ11	66	V_{SS}	112	V_{CCQ}	158	CS1#
21	CKE0	67	DQS5	113	NC	159	DQS14
22	V_{CCQ}	68	DQ42	114	DQ20	160	V_{SS}
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	V_{CC}	116	V_{SS}	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	V_{SS}	72	DQ48	118	A11	164	V_{CCQ}
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	V_{SS}	120	V_{CC}	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	V_{CCQ}	76	CK2	122	A8	168	V_{CC}
31	DQ19	77	V_{CCQ}	123	DQ23	169	DQS15
32	A5	78	DQS6	124	V_{SS}	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	V_{SS}	80	DQ51	126	DQ28	172	V_{CCQ}
35	DQ25	81	V_{SS}	127	DQ29	173	NC
36	DQS3	82	V_{CCID}	128	V_{CCQ}	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	V_{CC}	84	DQ57	130	A3	176	V_{SS}
39	DQ26	85	V_{CC}	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	V_{SS}	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	V_{SS}	88	DQ59	134	NC	180	V_{CCQ}
43	A1	89	V_{SS}	135	NC	181	SA0
44	NC	90	WP	136	V_{CCQ}	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	V_{CC}	92	SCL	138	CK0#	184	V_{CCSPD}

PIN NAMES

A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS16	Data Strobe Input/Output
CK0, CK1, CK2	Clock Input
CK0#. CK1#, CK2#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
V_{CC}	Power Supply (2.5V)
V_{CCQ}	Power Supply for DQS (2.5V)
V_{SS}	Ground
V_{REF}	Power Supply for Reference
V_{CCSPD}	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
V_{CCID}	V_{CC} Indentification Flag
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



CLOCK INPUT	5 SDRAMS
CK0/CK0#	4 SDRAMS
CK1/CK1#	6 SDRAMS
CK2/CK2#	6 SDRAMS

Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS resistors: 22 Ohms.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-1.0 to 3.6	V
Storage Temperature	T_{STG}	-55 to +150	°C
Power Dissipation	P_D	16	W
Short Circuit Current	I_{OS}	50	mA

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC CHARACTERISTICS

$0°C \leq T_A \leq 70°C$, $V_{CC} = 2.5V \pm 0.2V$

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	2.3	2.7	V
Supply Voltage	V_{CCQ}	2.3	2.7	V
Reference Voltage	V_{REF}	1.15	1.35	V
Termination Voltage	V_{TT}	1.15	1.35	V
Input High Voltage	V_{IH}	V_{REF} + 0.15	V_{CCQ} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	V_{REF} -0.15	V
Output High Voltage	V_{OH}	V_{TT} + 0.76	—	V
Output Low Voltage	V_{OL}	—	V_{TT}-0.76	V

CAPACITANCE

$T_A = 25°C$. f = 1MHz, $V_{CC} = 2.5V$, $V_{REF} = 1.4V \pm 200mV$

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A11)	C_{IN1}	53	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	53	pF
Input Capacitance (CKE0, CKE1)	C_{IN3}	29	pF
Input Capacitance (CK0-2,CK0-2#)	C_{IN4}	18	pF
Input Capacitance (CS0#, CS1#)	C_{IN5}	29	pF
Input Capacitance (DQM0-DQM8)	C_{IN6}	8	pF
Input Capacitance (BA0-BA1)	C_{IN7}	53	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C_{OUT}	8	pF

I_{DD} SPECIFICATIONS AND TEST CONDITIONS

Recommended operating conditions, 0°C ≤ T_A ≤ 70°C, V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V
Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR266@CL=2 Max	DDR266@CL=2.5 Max	DDR200@CL=2 Max	Units
Operating Current	I_{DD0}	One device bank; Active - Precharge; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	2840	2840	2840	mA
Operating Current	I_{DD1}	One device bank; Active-Read-Precharge Burst = 2; t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle.	3040	3040	3040	mA
Precharge Power-Down Standby Current	I_{DD2P}	All device banks idle; Power-down mode; t_{CK}=t_{CK} (MIN); CKE=(low)	95	95	95	rnA
Idle Standby Current	I_{DD2F}	CS# = High; All device banks idle; t_{CK}=t_{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS and DM.	800	800	800	mA
Active Power-Down Standby Current	I_{DD3P}	One device bank active; Power-Down mode; t_{CK} (MIN); CKE=(low)	800	800	800	mA
Active Standby Current	I_{DD3N}	CS# = High; CKE = High; One device bank; Active-Precharge; t_{RC}=t_{RAS} (MAX); t_{CK}=t_{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	1520	1520	1520	mA
Operating Current	I_{DD4R}	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; T_{CK}= T_{CK} (MIN); I_{OUT} = 0mA.	3520	3520	3520	mA
Operating Current	I_{DD4W}	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK} (MIN); DQ,DM and DQS inputs changing once per clock cycle.	4000	4000	4000	rnA
Auto Refresh Current	I_{DD5}	t_{RC} = t_{RC} (MIN)	4960	4960	4960	mA
Self Refresh Current	I_{DD6}	CKE ≤ 0.2V	80	80	80	mA
Operating Current	I_{DD7A}	Four bank interleaving Reads (BL=4) with auto precharge with t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	7680	7680	7680	mA

DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RCD}=2*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL=2, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout=0mA
4. Timing Patterns :
   - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}
     Read with Autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
   - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL2=2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=2*t_{CK}
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend:

A = Activate, R = Read, W = Write, P = Precharge, N = NOP

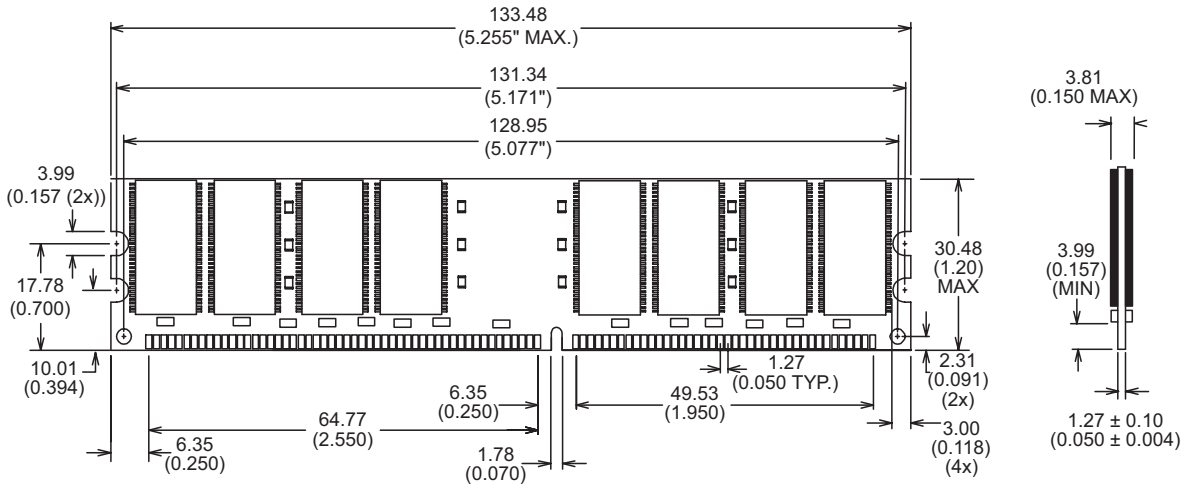
A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3

ORDERING INFORMATION FOR D3

Part Number	Speed	CAS Latency	t_{RCD}	t_{RP}	Height*
W3EG64129S262D3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG64129S265D3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")
W3EG64129S202D3	100MHz/200Mb/s	2	2	2	30.48 (1.20")

PACKAGE DIMENSIONS FOR D3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

Document Title

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Revision History

Rev #	History	Release Date	Status
Rev A	Created Datasheet	9-23-02	Advanced
Rev 0	0.1 Updated CAP and I_{DD} specs. 0.2 Removed "ED" from part marking 0.3 Moved from Advanced to Preliminary	6-04	Primary