Revision History

*** Rev. 0.95**
Date : 2001.07.23
1. Page2, 7, 8, 10, 12 : Add 2D RIMM part

Overview

The Rambus® RIMM™ module is a general purpose high-performance memory subsystem suitable for use in a broad range of applications including computer memory, personal computers, workstations, and other applications where high bandwidth and low latency are required.

The Rambus RIMM module consist of 256/288Mb Direct Rambus DRAM devices. These are extremely high-speed CMOS DRAMs organized as 16M words by 16/18 bits. The use of Rambus Signaling Level (RSL) technology permits 600MHz ,711MHz or 800MHz transfer rates while using conventional system and board design technologies. RDRAM devices are capable of sustained data transfers at 1.25 ns per two bytes (10ns per 16 bytes).

The RDRAM architecture enables the highest sustained bandwidth for multiple, simultaneous randomly addressed memory transactions. The separate control and data buses with independent row and column control yield over 95% bus efficiency. The Direct RDRAM's 32-banks architecture supports up to four simultaneous transactions per device.

Features

- High speed 800,711 and 600 MHz RDRAM storage
- 184 edge connector pads with 1 mm pad spacing
- Maximum module PCB size: 133.5mm x 34.93mm x 1.37mm(5.21” x 1.375” x 0.05”)
- Gold plated edge connector pad contacts
- Serial Presence Detect(SPD) support
- Operates from a 2.5 volt supply (±5%)
- Powerdown self refresh modes
- µBGA Package (92 balls)
- Separate Row and Column buses for higher efficiency

Key Timing Parameters/Part Numbers

The following table lists the frequency and latency bins available from RIMM modules.

Table 1: Part Number by Frequency and Latency

Organization	I/O Freq. MHz	t rac (Row Access Time) ns	Part Number
32M x 16/18	600	53	HYMR23216(18)H-653
32M x 16/18	711	45	HYMR23216(18)H-745
32M x 16/18	800	45	HYMR23216(18)H-845
32M x 16/18	800	40	HYMR23216(18)H-840
64M x 16/18	600	53	HYMR26416(18)H-653
64M x 16/18	711	45	HYMR26416(18)H-745
64M x 16/18	800	45	HYMR26416(18)H-845
64M x 16/18	800	40	HYMR26416(18)H-840
128M x 16/18	600	53	HYMR212816(18)H-653
128M x 16/18	711	45	HYMR212816(18)H-745
128M x 16/18	800	45	HYMR212816(18)H-845
128M x 16/18	800	40	HYMR212816(18)H-840
256M x 16/18	600	53	HYMR225616(18)H-653
256M x 16/18	711	45	HYMR225616(18)H-745
256M x 16/18	800	45	HYMR225616(18)H-845
256M x 16/18	800	40	HYMR225616(18)H-840

Form Factor

The Rambus RIMM modules are offered in a 184-pad 1mm edge connector pad pitch from factor suitable for either 184 or 168 contact RIMM connectors. The RIMM module is suitable for desktop and other system applications. Figure 1 below, shows an eight device Rambus RIMM module without heat spreader.

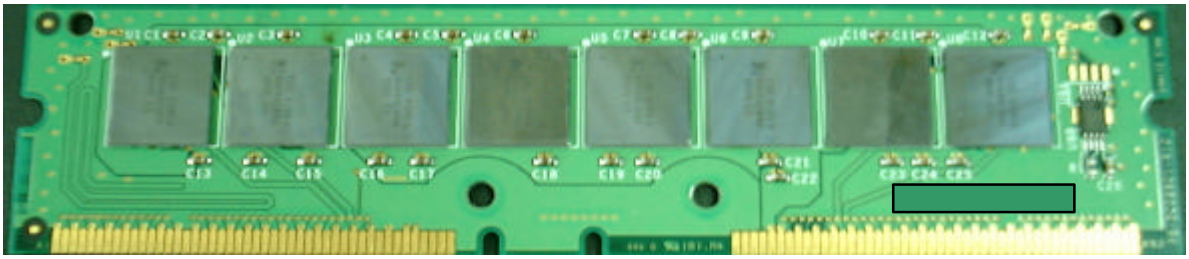


Figure 1: Rambus RIMM Module without heat spreader

Table 2: Module Pad Number and Signal Names

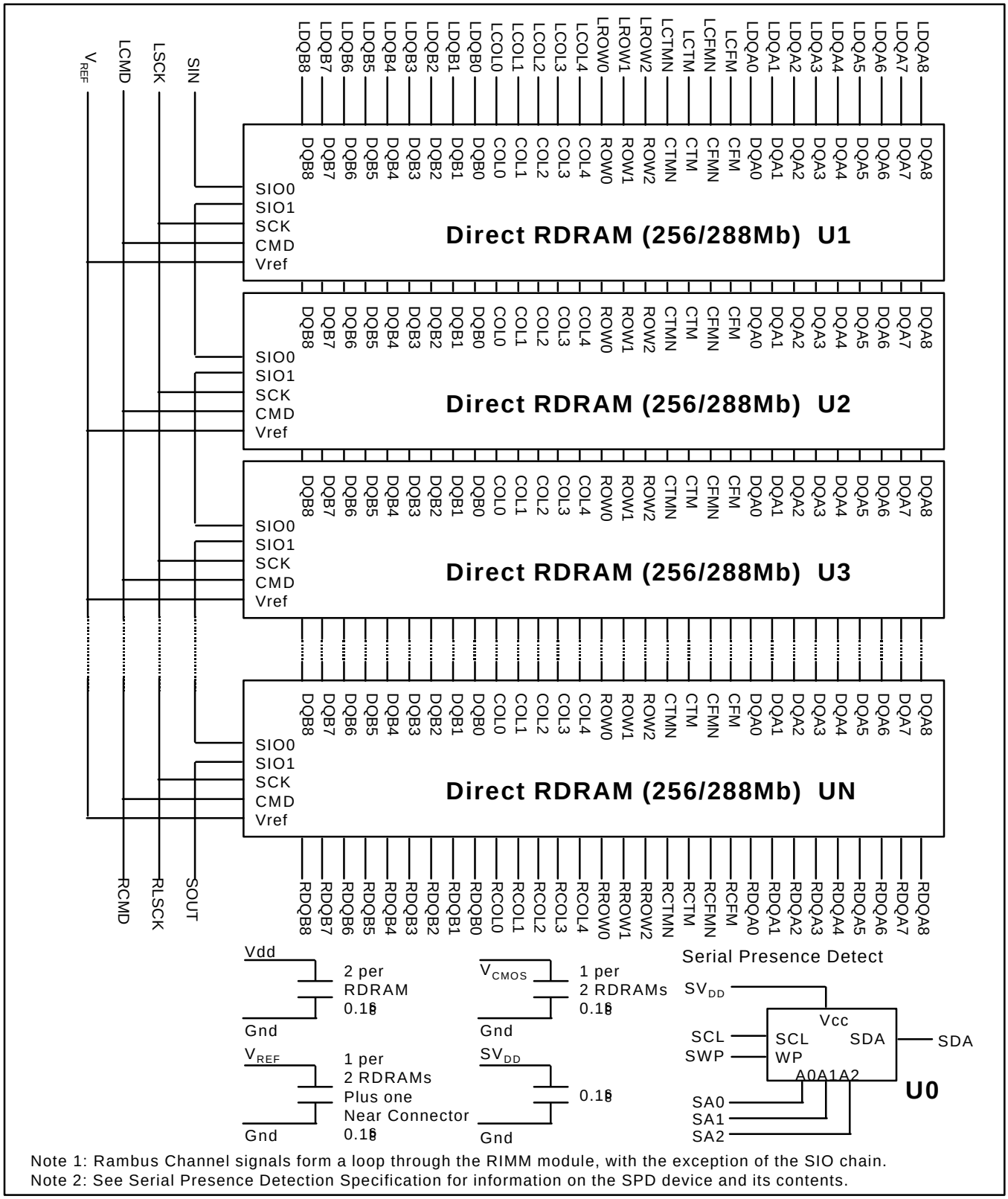
Pin	Pin Name	Pin	Pin Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTMN	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTM	B14	NC
A15	Gnd	B15	Gnd
A16	NC	B16	LROW2
A17	Gnd	B17	Gnd
A18	LROW1	B18	LROW0
A19	Gnd	B19	Gnd
A20	LCOL4	B20	LCOL3
A21	Gnd	B21	Gnd
A22	LCOL2	B22	LCOL1
A23	Gnd	B23	Gnd
A24	LCOL0	B24	LDQB0
A25	Gnd	B25	Gnd
A26	LDQB1	B26	LDQB2
A27	Gnd	B27	Gnd
A28	LDQB3	B28	LDQB4
A29	Gnd	B29	Gnd
A30	LDQB5	B30	LDQB6
A31	Gnd	B31	Gnd
A32	LDQB7	B32	LDQB8
A33	Gnd	B33	Gnd
A34	LSCK	B34	LCMD
A35	Vcmos	B35	Vcmos
A36	SOUT	B36	SIN
A37	Vcmos	B37	Vcmos
A38	NC	B38	NC
A39	Gnd	B39	Gnd
A40	NC	B40	NC
A41	Vdd	B41	Vdd
A42	Vdd	B42	Vdd
A43	NC	B43	NC
A44	NC	B44	NC
A45	NC	B45	NC
A46	NC	B46	NC

Pin	Pin Name	Pin	Pin Name
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	Vref	B51	Vref
A52	Gnd	B52	Gnd
A53	SCL	B53	SA0
A54	Vdd	B54	Vdd
A55	SDA	B55	SA1
A56	SVdd	B56	SVdd
A57	SWP	B57	SA2
A58	Vdd	B58	Vdd
A59	RSCK	B59	RCMD
A60	Gnd	B60	Gnd
A61	RDQB7	B61	RDQB8
A62	Gnd	B62	Gnd
A63	RDQB5	B63	RDQB6
A64	Gnd	B64	Gnd
A65	RDQB3	B65	RDQB4
A66	Gnd	B66	Gnd
A67	RDQB1	B67	RDQB2
A68	Gnd	B68	Gnd
A69	RCOL0	B69	RDQB0
A70	Gnd	B70	Gnd
A71	RCOL2	B71	RCOL1
A72	Gnd	B72	Gnd
A73	RCOL4	B73	RCOL3
A74	Gnd	B74	Gnd
A75	RROW1	B75	RROW0
A76	Gnd	B76	Gnd
A77	NC	B77	RROW2
A78	Gnd	B78	Gnd
A79	RCTM	B79	NC
A80	Gnd	B80	Gnd
A81	RCTMN	B81	RCFMN
A82	Gnd	B82	Gnd
A83	RDQA0	B83	RCFM
A84	Gnd	B84	Gnd
A85	RDQA2	B85	RDQA1
A86	Gnd	B86	Gnd
A87	RDQA4	B87	RDQA3
A88	Gnd	B88	Gnd
A89	RDQA6	B89	RDQA5
A90	Gnd	B90	Gnd
A91	RDQA8	B91	RDQA7
A92	Gnd	B92	Gnd

Table 3: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, A82, A84, A86, A88, A90, A92, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B39, B52, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80, B82, B84, B86, B88, B90, B92			Ground reference for RDRAM core and interface. 72 PCB connector pads.
LCFM	B10	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B34	I	V_{CMOS}	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4.. LCOL0	A20, B20, A22, B22, A24	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A14	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A12	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8.. LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on x16 RDRAM devices.
LDQB8.. LDQB0	B32, A32, B30, A30, B28, A28, B26, A26, B24	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on x16 RDRAM devices.
LROW2.. LROW0	B16, A18, B18	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A34	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A16, B14, A38, B38, A40, B40, A77, B79			These pads are not connected. These 8 connector pads are reserved for future use.
NC	A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50			These pads are not connected. These 16connector pads art reserved for future use. The 168 contact RIMM connector does not connect to these PCB pads.
RCFM	B83	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	B81	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.

Signal	Module Connector Pads	I/O	Type	Description
RCMD	B59	I	V_{CMOS}	Serial Command Input used to read from and write to the control registers. Also used for power management.
RCOL4.. RCOL0	A73, B73, A71, B71, A69	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	A79	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	A81	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8.. RDQA0	A91, B91, A89, B89, A87, B87, A85, B85, A83	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on x16 RDRAM devices.
RDQB8.. RDQB0	B61, A61, B63, A63, B65, A65, B67, A67, B69	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on x16 RDRAM devices.
RROW2.. RROW0	B77, A75, B75	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A59	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B53	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	B55	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	B57	I	SV_{DD}	Serial Presence Detect Address 2.
SCL	A53	I	SV_{DD}	Serial Presence Detect Clock.
SDA	A55	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O)
SIN	B36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{DD}	A56, B56			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	A57	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A35, B35, A37, B37			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A41, A42, A54, A58, B41, B42, B54, B58	I		Supply voltage for the RDRAM core and interface logic.
Vref	A51, B51			Logic threshold reference voltage for RSL signals.



Note 1: Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.
Note 2: See Serial Presence Detection Specification for information on the SPD device and its contents.

Figure 2: RIMM Module Functional Diagram

Absolute Maximum Ratings

Signal	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to Gnd	- 0.3	V DD + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V DD + 1.0	V
T_{STORE}	Storage temperature	- 50	100	ºC
T_{PLATE}	Plate temperature	-	100	ºC

DC Recommended Electrical Conditions

Signal	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers: CMOS I/O power supply at pad for 1.8V controllers:	2.5 - 0.13 1.8 - 0.1	2.5 + 0.25 1.8 + 0.2	V V
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{SPD}	Serial Presence Detector - Positive power supply	2.2	3.6	V
V_{IL}	RSL input low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{IH}	RSL input high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage	- 0.3	$0.5V_{CMOS}$ - 0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	$0.5V_{CMOS}$ + 0.25	V_{CMOS} + 0.3	V
$V_{OL,CMOS}$	CMOS output low voltage @ $I_{OL,CMOS}$ = 1mA		0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = -0.25mA	V_{CMOS} - 0.3		V
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	µA
$I_{SCK,CMD}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	µA
$I_{SIN,SOUT}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10.0	10.0	µA

a. The tale below shows the number of 256Mb or 288Mb RDRAM devices contained in a RIMM module of listed memory storage capacity

RIMM Module Capacity:	512/576MB	384/432MB	256/288MB	128/144MB	64/72MB
Number of 256Mb or 288Mb RDRAM devices:	16	12	8	4	2

RIMM Module Current Profile

I_{DD}	RIMM Module Capacity: No. of 256/288Mb RDRAMs:		512/576MB 16	384/423MB 12	256/288MB 8	128/144MB 4	64/72MB 2	Unit
	RIMM Module power conditions[a]	Freq.	Max	Max	Max	Max	Max	
I_{DD1}	One RDRAM in Read[b], balance in NAP mode	800	798	782	767	751	742	mA
		711	746	730	714	698	679	
		600	641	625	609	593	584	
I_{DD2}	One RDRAM in Read[b], balance in Standby mode	800	2860	2340	1820	1300	1040	mA
		711	2667	2187	1707	1227	987	
		600	2406	1996	1526	1086	866	
I_{DD3}	One RDRAM in Read[b], balance in Active mode	800	3100	2460	1820	1180	860	mA
		711	2900	2300	1700	1100	800	
		600	2350	1870	1390	910	670	
I_{DD4}	One RDRAM in Write[b], balance in NAP mode	800	956	940	924	908	899	mA
		711	851	835	819	803	792	
		600	746	730	714	698	689	
I_{DD5}	One RDRAM in Write[b], balance in Standby mode	800	2868	2303	1738	1174	892	mA
		711	2800	2240	1680	1120	840	
		600	2262	1818	1375	932	711	
I_{DD6}	One RDRAM in Write[b], balance in Active mode	800	3055	2535	2015	1495	1235	mA
		711	2800	2320	1840	1360	1120	
		600	2544	2104	1664	1224	1004	

a. Actual Power will depend on individual RDRAM component specifications, memory controller and usage patterns. Please refer to specific RIMM module vendor data sheets for additional information.
b. I/O current is a function of the % of 1s, to add I/O power for 50% 1s for a x16 need to add 257mA or 290mA for x18 ECC modu le for the following : V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V and V_{DIL} = V_{REF} - 0.5V.

AC Electrical Specifications

Symbol	Parameter and Condition	Min	Typ	Max	Unit
Z_L	Module Impedance of RSL Signals	25.2	28	30.8	Ω
$Z_{UL\text{-}CMOS}$	Module Impedance of SCK and CMD signals	23.8	28	32.2	Ω
T_{PD}	Average clock delay form finger to finger of all RSL clock nets (CTMN, CFM, and CFMN)	-		See Table[a]	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD}[a,b] for 4, 6, 8, and 12 device modules	-21		21	ps
	Propagation delay variation of RSL signals with respect to T_{PD}[a,b] for 16 device modules	-24		24	ps
$\Delta T_{PD\text{-}CMOS}$	Propagation delay variation of SCK signal with respect to an average clock delay[a]	-250		250	ps
$\Delta T_{PD\text{-}SCK,CMD}$	Propagation delay variation of CMD signal with respect to SCK signal	-200		200	ps
V_{α}/V_{IN}	Attenuation Limit			See Table[a]	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time 20%-80%)			See Table[a]	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time 20%-80%)			See Table[a]	%

a. Tpd or Average clock delay is defined as the average delay from finger of all RSL clock nets(CTM, CTMN, CFM, and CFMN)

b. If the RIMM module meets the following specification, then it is compliant to the specification. If the RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔT_{PD} Specification" table

Adjusted ΔT_{PD} Specification

Symbol	Parameter and Conditions	Adjusted Min/Max	Absolute Min/Max		Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} for 4,6 and 8 device modules	+/-[17+(18*N* ΔZ0)][a]	-30	30	ns
	Propagation delay variation of RSL signals with respect to T_{PD} for 12 device modules	+/-[20+(18*N* ΔZ0)][a]	-40	40	ps
	Propagation delay variation of RSL signals with respect to T_{PD} for 16 device modules	+/-[24+(18*N* ΔZ0)][a]	-50	50	ps

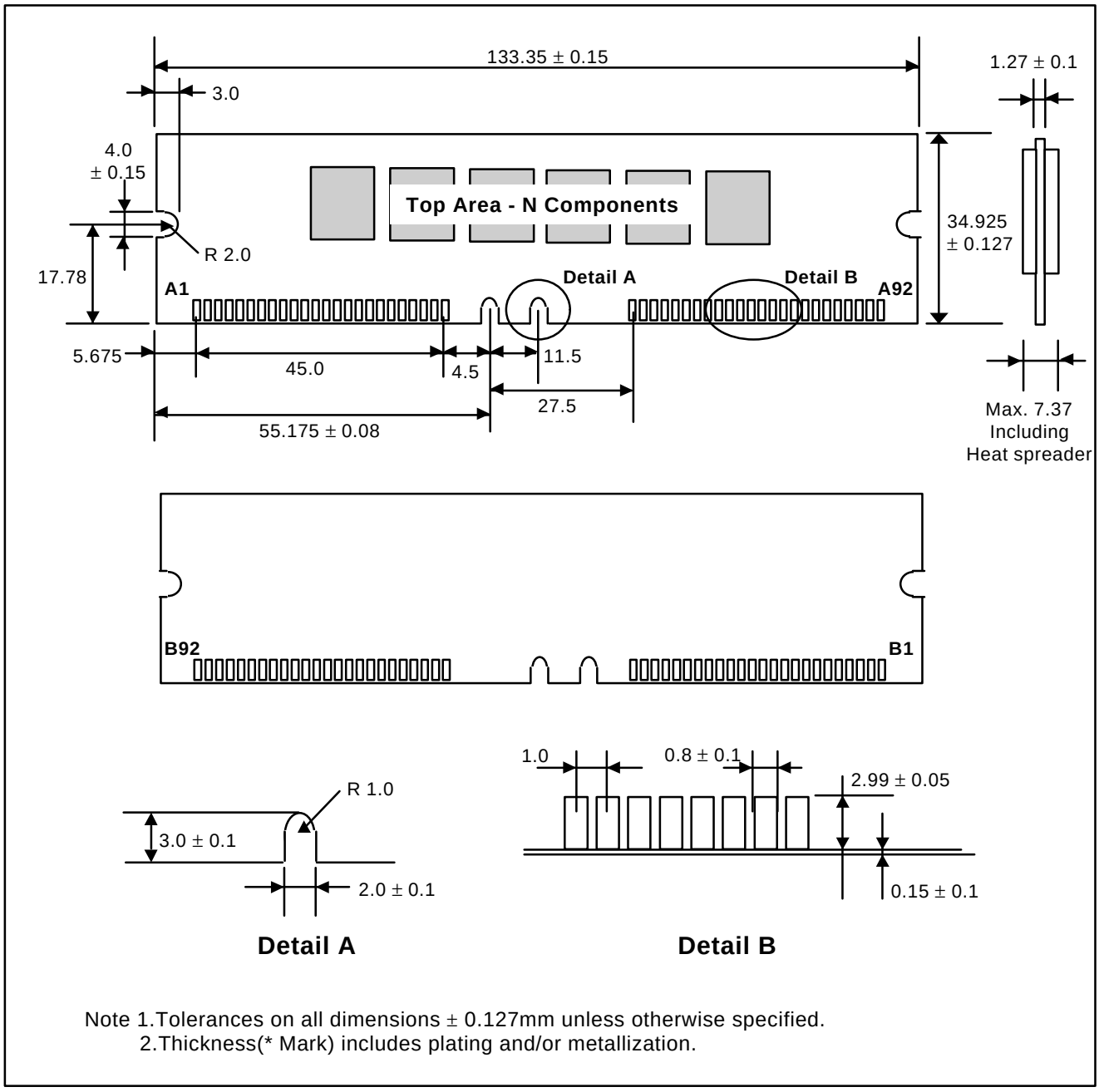
a. Where : N =Number of RDRAM devices installed on the RIMM module
ΔZ0 = delta Z0% = (max Z0 - min Z0)/(min Z0)
(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

AC Electrical Specifications for RIMM Modules

Symbol	RIMM Module Capacity: No. of 256/288Mb RDRAMs:	512/576MB 16	384/432MB 12	256/288MB 8	128/144MB 4	64/72MB 2	Unit
	Parameter and Condition for -800, -711 & -600 RIMM Module	**Max**	**Max**	**Max**	**Max**	**Max**	
T_{PD}	Propagation Delay, all RSL signals	2.11	1.76	1.56	1.28	1.28	ns
V_{α} / V_{IN}	Attenuation Limit -800, -711	25.0	20.0	16.0	12.0	12.0	%
	Attenuation Limit -600	18.5	15.5	12.5	10.5	10.5	%
V_{XF} / V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%) -800, -711, -600	8.0	6.0	4.0	2.0	2.0	%
V_{XB} / V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%) -800, -711, -600	2.5	2.3	2.0	1.5	1.5	%
R_{DC}	DC Resistance Limit -800, -711, -600	1.2	1.1	0.8	0.6	0.6	Ω

Physical Dimensions

The following defines the RIMM module dimensions. All units are in millimeters. The height of the module is 31.75mm.



Note 1.Tolerances on all dimensions ± 0.127mm unless otherwise specified.
2.Thickness(* Mark) includes plating and/or metallization.

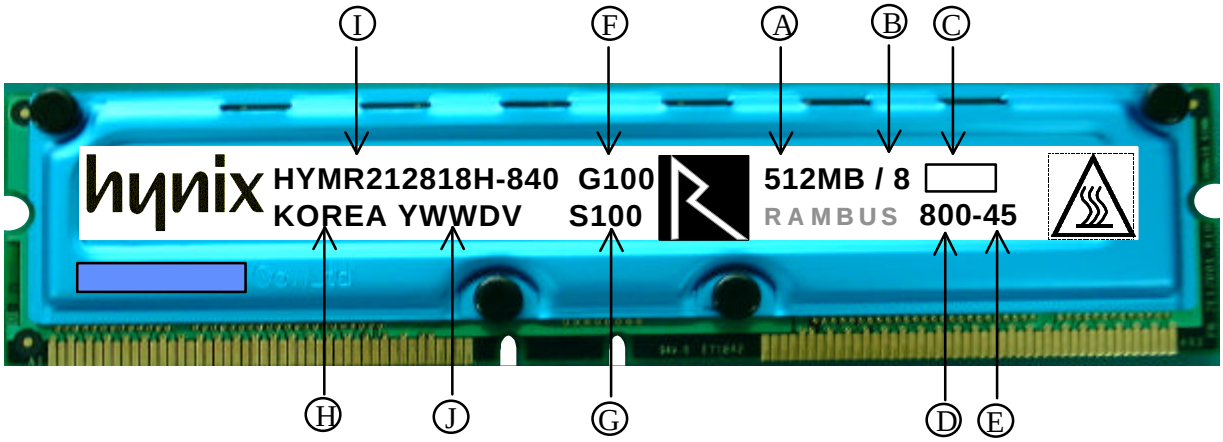
Figure 3: RIMM Module PCB Physical Description

Module Weight

The maximum RIMM Module weight is 75gm(2.625oz) with a center of mass 35mm (1.378 in.) upwards from bottom edge.

Standard RIMM Module Marking

The RIMM modules available from RIMM module manufacturers will be marked per Figure 4 below. This industry standard marking will help OEMs and users identify the Rambus RIMM modules for use in specific system application. This marking also assists OEMs or users to specify and verify if the correct RIMM



	Label Field	Description	Marked Text	Unit
A	Module Memory capacity	Number of 8-bit or 9-bit Mbytes of RDRAM storage in RIMM module	512MB, 384MB 256MB,128MB,64MB	MBytes
B	Number of DRDRAMs	Number of RDRAM devices contained in the RIMM module	/16, /12, /8, /4, /2	RDRAM devices
C	ECC support	Indicates whether the RIMM module supports 8-bit (no ECC) or 9-bit (ECC) Bytes	Blank = 8-bit Byte ECC = 9-bit Byte	
D	Memory Speed	Data transfer speed for RDRAM RIMM module	800, 711, 600	MHz
E	t_{RAC}	Row Access Time (Optional field)	-40, -45, -50, -53 or blank	ns
F	Gerber Version	PCB Gerber file revision used on RIMM Module (Optional field)	Rev 1.00 = G100 or blank	
G	SPD Version	SPD Code Version (Optional field)	Rev 1.00 = S100 or blank	
H	Country	Country Area	Korea	
I	Vendor	Hynix specific RIMM module Information	Product Part No	
J	Vendor	Hynix specific Date code, Ass'y Vender	YWWDV	

Figure 4: Standard RIMM Module Marking

SPD Specification
based on 256/288Mb RDRAM

Version 1.1
July 2001

Revision History

Revision 1.1 (July 2001)

- Added 2D Product.
  - Added 2D items at Byte75, 76, 77 regarding Part Number
  - Added 2D items at Byte99, 101, 102 regarding device number
  - Added 2D checksum data.

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIPTION	FUNCTION				Hex VALUE				NOTE
		-840	-845	-745	-653	-840	-845	-745	-653	
BYTE0	SPD Revision Level	SPD Revision 1.0				02h				
BYTE1	Total # of Bytes in the SPD	256Bytes				08h				
BYTE2	Device Type	Direct RDRAM				01h				
BYTE3	Module Type	RIMM				01h				
BYTE4	Row Address bits[0:3], Column Address bits[0:3]	9bits, 7bits				97h				
BYTE5	Bank Address bits and Type	32Banks (5bank bits)				C5h				
BYTE6	Refresh Bank bits	32 Refresh Bank Sets				05h				
BYTE7	Refresh Reriod (tREF)	32ms				20h				
BYTE8	Protocol Version	Protocol Version 1				02h				
BYTE9	Miscellaneous Device Configuration Field	DQS=1.5, no-LP, S28, S3				05h				
BYTE10	Minimum Precharge to RAS time(tRP-R,Min)	8cycles				08h				
BYTE11	Minimum RAS to Precharge time(tRAS-R,Min)	20cycles				14h				
BYTE12	Minimum RAS to CAS time(tRCD-R,Min)	8cycles	10cycles	8cycles	8cycles	08h	0Ah	08h	08h	
BYTE13	Minimum RAS to RAS time(tRR-R,Min)	8cycles				08h				
BYTE14	Minimum Precharge to Precharge time(tPP-R,Min)	8cycles				08h				
BYTE15	Min tCYCLE for RangeA	2.50ns		2.80ns	3.33ns	13h		15h	1Ah	
BYTE16	Max tCYCLE for RangeA	3.83ns				1Eh				
BYTE17	tCDLY Range for RangeA	5tCYCLE ~ 9tCYCLE				59h				
BYTE18	tCLS and tCAS Range for RangeA	2tCYCLE for tCLS & tCAS				AAh				
BYTE19	Min tCYCLE for RangeB	Reserved				00h				
BYTE20	Max tCYCLE for Range**B**	Reserved				00h				
BYTE21	tCDLY Range for RangeB	Reserved				00h				
BYTE22	tCLS and tCAS Range for RangeB	Reserved				00h				
BYTE23	Min tCYCLE for RangeC	Reserved				00h				
BYTE24	Max tCYCLE for Range**C**	Reserved				00h				
BYTE25	tCDLY Range for RangeC	Reserved				00h				
BYTE26	tCLS and tCAS Range for RangeC	Reserved				00h				
BYTE27	Min tCYCLE for RangeD	Reserved				00h				
BYTE28	Max tCYCLE for Range**D**	Reserved				00h				
BYTE29	tCDLY Range for RangeD	Reserved				00h				
BYTE30	tCLS and tCAS Range for RangeD	Reserved				00h				
BYTE31	Power Down Exit Max. time, PhaseA(tPD-NXA,Max)	4us				04h				
BYTE32	Power Down Exit Max. time, PhaseB(tPD-NXB,Max)	9000tCYCLE				8Dh				
BYTE33	Nap Exit Max.time, PhaseA(tNAPXA,Max)	50ns				32h				
BYTE34	Nap Exit Max.time, PhaseB(tNAPXB,Max)	40ns				28h				
BYTE35	fMIN[11:8], fMAX[11:8]	261MHz, 400MHz		261MHz, 357MHz	261MHz, 300MHz	11h				
BYTE36	fMIN[7:0]	261MHz				05h				
BYTE37	fMAX[7:0]	400MHz		357MHz	300MHz	90h		65h	2Ch	
BYTE38	ODF Mapping	Reserved				00h				
BYTE39	Max time between Current Control(tCCTRL,Max)	100ms				64h				
BYTE40	Max time between Temp. Calibration(tTEMP,Max)	100ms				64h				
BYTE41	Max time between Temp. Calibration Enable and Command (tTCEN,Min)	150tCYCLE				96h				
BYTE42	Maximum RAS to Precharge time(tRAS-R,Max)	64us				40h				
BYTE43	Maximum time that a Device can stay in Nap Mode (tNLIMIT,Max)	10us				0Ah				

Continued

BYTE NUMBER	FUNCTION DESCRIPTION	Option	FUNCTION				Hex VALUE				NOTE
			-840	-845	-745	-653	-840	-845	-745	-653	
BYTE44	ACTREFPT[3:0], PCHREFPT[3:0]		6tCYCLE, 6tCYCLE				66h				
BYTE45	CPCHREFPT_DC[3:0], RDREFPT_DC[3:0]		5tCYCLE, 5tCYCLE				55h				
BYTE46	RETREFPT_DC[3:0], WRREFPT_DC[3:0]		5tCYCLE, 13tCYCLE				5Dh				
BYTE47~49	Reserved		-				00h				
BYTE50	fRAS[11:8]		400MHz		357MHz	300MHz	01h				
BYTE51	fRAS[7:0]						90h		65h	2Ch	
BYTE52	PMAX,HI,PMAX,LO,Tj		0,0,100℃				24h				
BYTE53	HeatSpreader, thermal sensor, Tplate		1,0,100℃				A4h				
BYTE54	PSTBY,HI		130mA		120mA	110mA	82h		78h	6Eh	
BYTE55	PACTI,HI		200mA		190mA	180mA	64h		5Fh	5Ah	
BYTE56	PACTRW,HI		750mA		700mA	650mA	5Eh		58h	4Bh	
BYTE57	PSTBY,LO		TBD		TBD	TBD	00h		00h	00h	
BYTE58	PACTI,LO		TBD		TBD	TBD	00h		00h	00h	
BYTE59	PACTRW,HI		TBD		TBD	TBD	00h		00h	00h	
BYTE60	PNAP		4.2mA				21h				
BYTE61	PRESA(Reserved for a future thermal parameter)		Reserved				00h				
BYTE62	PRESB(Reserved for a future thermal parameter)		Reserved				00h				
BYTE63	Checksum for bytes 0 ~ 62		-				0Bh	0Dh	A2h	19h	
BYTE64	Module Manufacturer ID Code		Hynix				ADh				
BYTE65~71	..... Module Manufacturer ID Code		Hynix				00h				
BYTE72	Module Manufacturing Location		Hynix (Korea Area) HSA (United States Area) HSE (Europe Area) HSJ (Japan Area) Asia Area				0*h 1*h 2*h 3*h 4*h				1
BYTE73	Module Part Number (Component)		R (Rambus)				52h				2,3
BYTE74	Module Part Number (256/288Mb based)		2				32h				2,3
BYTE75	Module Part Number (Memory Width)	2D	Blank				20h				2,3
		4D	Blank				20h				
		8D	1				31h				
		12D	1				31h				
		16D	2				32h				
BYTE76	... Module Part Number (Memory Width)	2D	3				33h				2,3
		4D	6				36h				
		8D	2				32h				
		12D	9				39h				
		16D	5				35h				
BYTE77	..... Module Part Number (Memory Width)	2D	3				32h				2,3
		4D	4				34h				
		8D	8				38h				
		12D	2				32h				
		16D	6				36h				

Continued

BYTE NUMBER	FUNCTION DESCRIPTION	Option	FUNCTION				Hex VALUE				NOTE
			-840	-845	-745	-653	-840	-845	-745	-653	
BYTE78	Module Part Number (Data Width)	16bits	1				31h				2,3
		18bits	1				31h				
BYTE79	..... Module Part Number (Data Width)	16bits	6				36h				2,3
		18bits	8				38h				
BYTE80	Module Part Number (Manufacturing Site)		H				48h				2,3
BYTE81	Module Part Number (Hyphent)		-(Hyphen)				2Dh				2,3
BYTE82	Module Part Number (tRAC & Speed)		8	8	7	6	38h	38h	37h	36h	2,3
BYTE83	Module Part Number (tRAC & Speed)		4	4	4	5	34h	34h	34h	35h	2,3
BYTE84	Module Part Number (tRAC & Speed)		0	5	5	3	30h	35h	35h	33h	2,3
BYTE85 ~90	Module Part Number		Blank				20h				2,3
BYTE91~ 92	Module Revision Code		-				-				
BYTE93	Module Manufacturing Year		-				-				
BYTE94	Module Manufacturing Week		-				-				
BYTE95 ~98	Module Serial Number		-				-				
BYTE99	Number of Devices on module	2D	2				02h				
		4D	4				04h				
		8D	8				08h				
		12D	12				0Ch				
		16D	16				10h				
BYTE100	Module Data Width	16bits	16				10h				
		18bits	18				12h				
BYTE101	Device Enalbes	2D	All 2Devices				03h				
		4D	All 4Devices				0Fh				
		8D	All 8Devices				FFh				
		12D	All 12Devices				FFh				
		16D	All 16Devices				FFh				
BYTE102	..... Device Enalbes	2D	All 2Devices				00h				
		4D	All 4Devices				00h				
		8D	All 8Devices				00h				
		12D	All 12Devices				0Fh				
		16D	All 16Devices				FFh				
BYTE103 ~104	..... Device Enalbes		-				00h				
BYTE105	Module Vdd, Module Voltage Interface Level		2.5Vdd,1.8Vterm				10h				
BYTE106	Module Vdd Tolerance		5% DC, 2% AC				52h				
BYTE107 ~113	Reserved		-				00h				
BYTE114	CDLY0/1 for tCDLY=3		-				00h				
BYTE115	CDLY0/1 for tCDLY=4		2/0				20h				
BYTE116	CDLY0/1 for tCDLY=5		3/0				30h				
BYTE117	CDLY0/1 for tCDLY=6		3/1				31h				
BYTE118	CDLY0/1 for tCDLY=7		3/2				32h				
BYTE119	CDLY0/1 for tCDLY=8		4/2				42h				

Continued

BYTE NUMBER	FUNCTION DESCRIPTION	Option		FUNCTION				Hex VALUE				NOTE
				-840	-845	-745	-653	-840	-845	-745	-653	
BYTE120	CDLY0/1 for tCDLY=9			5/2				52h				
BYTE121	CDLY0/1 for tCDLY=10			-				00h				
BYTE122	CDLY0/1 for tCDLY=11			-				00h				
BYTE123	CDLY0/1 for tCDLY=12			-				00h				
BYTE124	CDLY0/1 for tCDLY=13			-				00h				
BYTE125	CDLY0/1 for tCDLY=14			-				00h				
BYTE126	CDLY0/1 for tCDLY=15			-				00h				
BYTE127	Checksum for bytes 99 - 126	16bits	2D	2				BEh				
			4D	4				CCh				
			8D	8				C0h				
			12D	12				D3h				
			16D	16				C7h				
		18bits	2D	2				C0h				
			4D	4				CEh				
			8D	8				C2h				
			12D	12				D5h				
			16D	16				C9h				
BYTE128 +	Open for Customer use			-				Undefined				

Note :
1. Refer to Hynix Web Site.
2. ASCII adopted
3. Basically Hynix writes Part No. except for 'HYM' in Byte 73~90 to use the limited 18 bytes from byte 73 to byte 90