M58LW128H

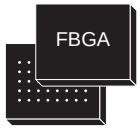
128 Mbit (8Mb x16, Uniform Block, Burst) 3V Supply Flash Memory

PRODUCT PREVIEW

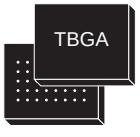
FEATURES SUMMARY

- WIDE x16 DATA BUS for HIGH BANDWIDTH
- SUPPLY VOLTAGE
  - V_{DD} = 2.7 to 3.6V core supply voltage for Program, Erase and Read operations
  - V_{DDQ} = 1.8 to V_{DD} for I/O Buffers
- SYNCHRONOUS/ASYNCHRONOUS READ
  - Synchronous Burst Read
  - Asynchronous Random Read
  - Asynchronous Address Latch Controlled Read
  - Page Read
- ACCESS TIME
  - 8 or 16 Word Synchronous Burst Mode up to 66MHz
  - 8 Word Asynchronous Page Mode 115/25ns
  - Random Read 115ns
- PROGRAMMING TIME
  - 32 Word Write Buffer
  - 12µs Word effective programming time
- 128 UNIFORM 64 KWord MEMORY BLOCKS
- BLOCK PROTECTION
  - All blocks protected at Power up
  - Blocks can be protected individually and instantly
  - $\overline{WP}$ for Block Lock-Down
- SECURITY
  - V_{PEN} Enabled Data Protection
  - 2 Kbit Protection Register with 64 bit Unique Code in OTP Area
- PROGRAM and ERASE SUSPEND
- PROGRAMMABLE WAIT SIGNAL
- COMMON FLASH INTERFACE
- 100,000 PROGRAM/ERASE CYCLES per BLOCK

Figure 1. Packages



VFBGA56 (ZB)
11 x 9mm



TBGA64 (ZA)
10 x 13mm

- ELECTRONIC SIGNATURE
  - Manufacturer Code: 0020h
  - Device Code M58LW128H: 8802h

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SUMMARY DESCRIPTION

M58LW128H is a 128 Mbit (8Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7V to 3.6V) core supply. On power-up the memory defaults to Read mode with an asynchronous bus where it can be read in the same way as a non-burst Flash memory.

The memory is divided into 128 blocks of 1Mbit that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for asynchronous read. In asynchronous read mode an Address Latch input can be used to latch addresses in Latch Controlled mode. In synchronous burst read mode, data is output on each clock cycle at frequencies of up to 66MHz.

The Write Buffer allows the microprocessor to program from 1 to 32 Words in parallel, both speeding up the programming and freeing up the microprocessor to perform other work. A Word Program command is available to program a single Word.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

The M58LW128H features an instant, individual block protection scheme that allows any block to be protected or unprotected with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be protected and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are protected at Power- Up.

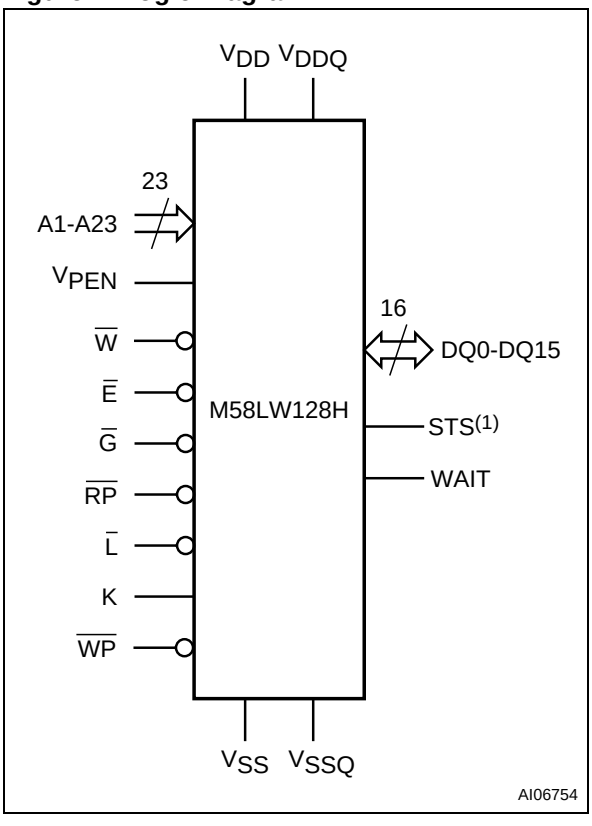
The device includes a Protection Register and two Protection Register locks to increase the protection of a system's design. The Protection Register is divided into seventeen 128-bit sub-registers: the first sub-register consists of a 64 bit segment containing a unique device number written by ST, and a 64-bit segment One-Time-Programmable (OTP) by the user. The other 16 sub-registers are all OTP and available for the user to program. The user programmable segment and sub-registers can be permanently protected. The Protection Register locks can be permanently protected by the user. Figure 8, shows the Protection Register Locks and Protection Register Memory Map.

The Reset/Power-Down pin is used to apply a Hardware Reset to the memory and to set the device in power-down mode.

The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes: Ready/Busy mode where a static signal indicates the status of the P/E.C, and Status mode where a pulsing signal indicates the end of a Program or Block Erase operation. In Status mode it can be used as a system interrupt signal, useful for saving CPU time.

The memory is available in VFBGA56 (11 x 9mm, 0.75mm pitch) and TBGA64 (10 x 13mm, 1mm pitch) packages.

Figure 2. Logic Diagram



Note: 1. The STS pin is available in TBGA64 packages only and not in VFBGA56 packages. See Figures 3 and 4.

Table 1. Signal Names

A1-A23	Address inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
K	Clock
$\overline{L}$	Latch Enable
WAIT	Wait
STS(1)	Status/(Ready/Busy)
$\overline{RP}$	Reset/Power-Down
V_{PEN}	Program/Erase Enable
$\overline{W}$	Write Enable
$\overline{WP}$	Write Protect
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
NC	Not Connected Internally

Note: 1. The STS pin is available in TBGA64 packages only and not in VFBGA56 packages. See Figures 3 and 4.

Figure 3. TBGA64 Connections (Top view through package)

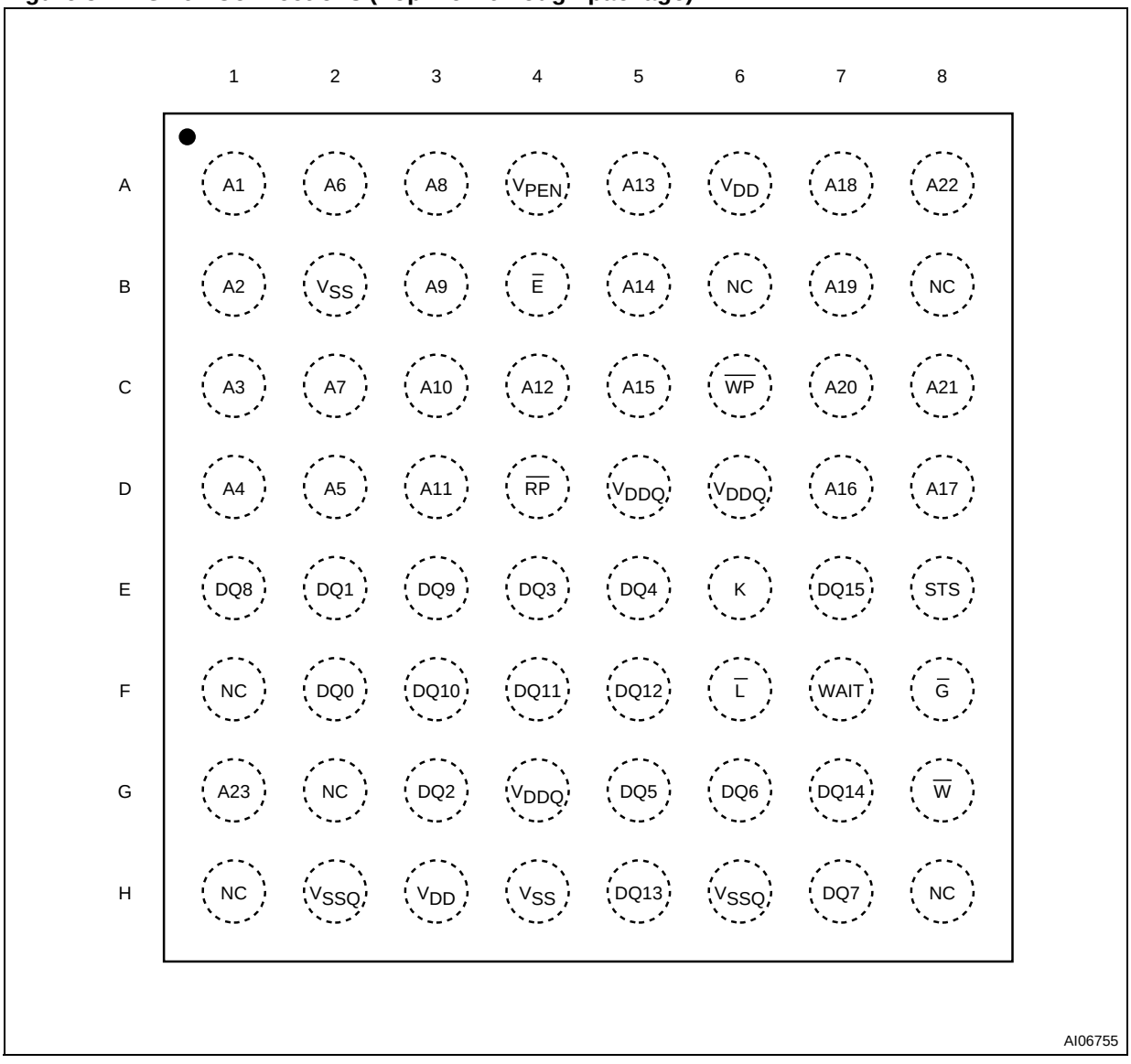


Figure 4. VFBGA56 Connections (Top view through package)

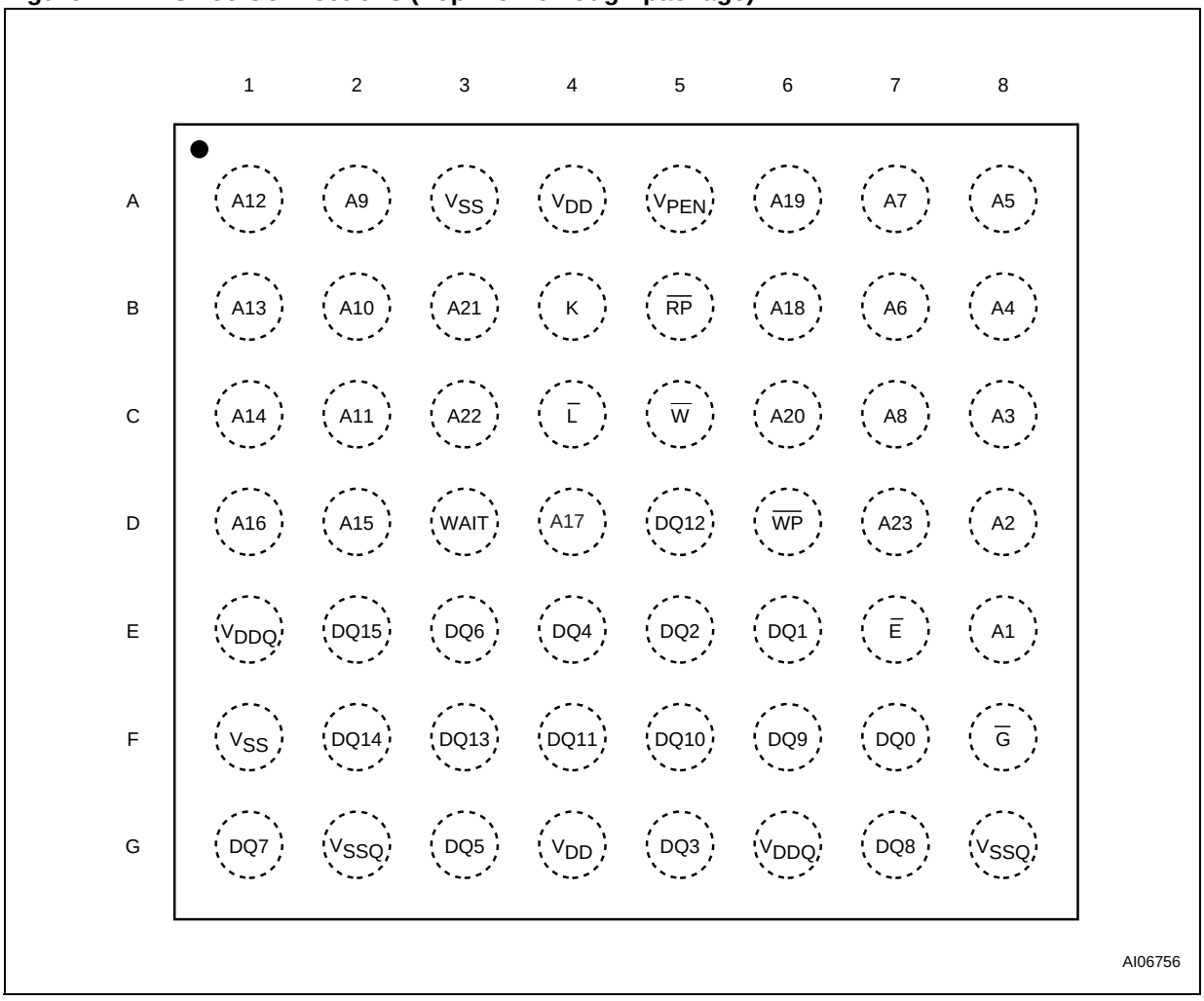
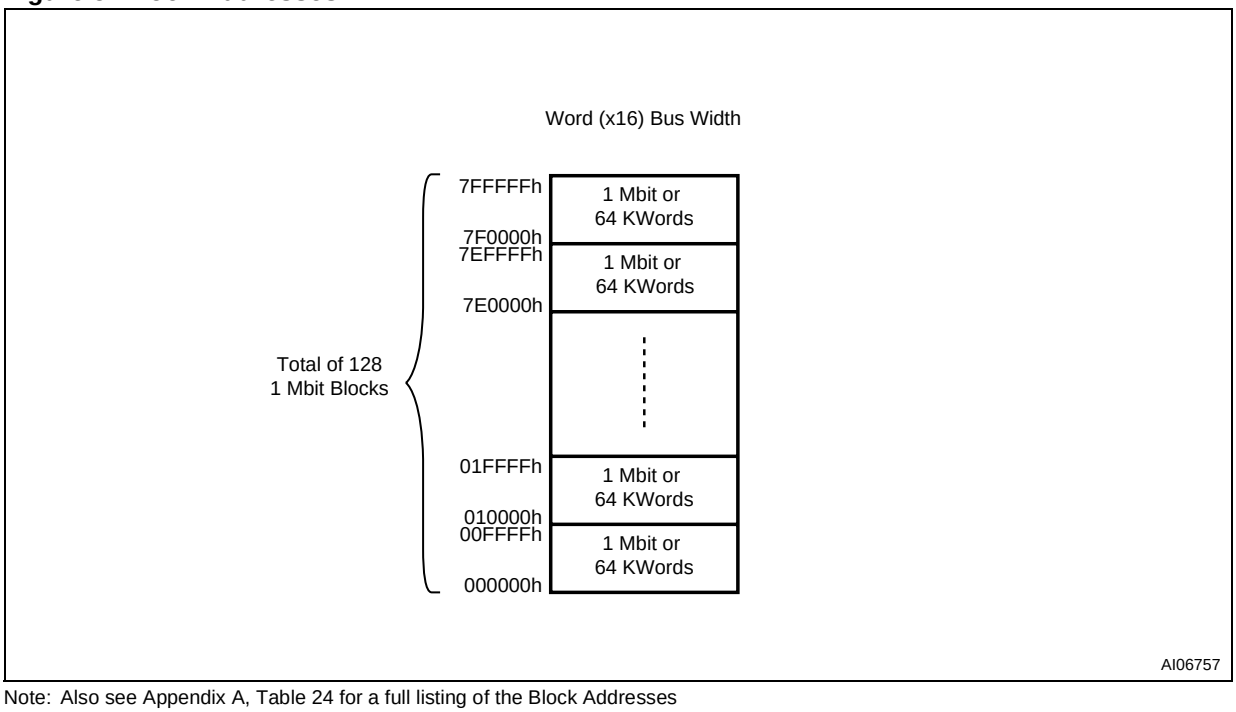


Figure 5. Block Addresses



Note: Also see Appendix A, Table 24 for a full listing of the Block Addresses

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A1-A23). The Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data to. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. Chip Enable and Latch Enable must be low when selecting the addresses.

The address latch is transparent when Latch Enable is low, V_{IL}. The address is internally latched in an Erase or Program operation.

Data Inputs/Outputs (DQ0-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both low, V_{IL}, the data bus outputs data from the memory array, the Electronic Signature, the Block Protection status, the CFI Information or the contents of the Status Register. The data bus is high impedance when the chip is deselected, Output Enable is high, V_{IH}, or the Reset/Power-Down signal is low, V_{IL}. When the Program/Erase Controller is active the Ready/Busy status is given on DQ7.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the Standby level, I_{DD1}.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation. When Output Enable, $\overline{G}$, is at V_{IH} the outputs are high impedance. Output Enable, $\overline{G}$, can be used to inhibit the data output during a burst read operation.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable.

Write Protect ($\overline{WP}$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the Locked-Down blocks can be protected or unprotected.

Reset/Power-Down ($\overline{RP}$). The Reset/Power-Down pin provides a Hardware Reset of the memory.

A Hardware Reset is achieved by holding Reset/Power-Down Low, V_{IL}, for at least t_{PLPH}. When Reset/Power-Down is Low, V_{IL}, the Status Register information is cleared, all blocks are locked down, the Configuration Register is reset and the power consumption is reduced to its power-down level. The device is deselected and outputs are high impedance.

After Reset/Power-Down goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHQV}.

If Reset/Power-Down goes low, V_{IL}, during an erase or program operation, the operation is aborted and the data may be corrupted. In this case the Status/(Ready/Busy) pin stays low, V_{IL}, for a maximum timing of t_{PLSZ}, until the completion of the internal reset operations. Note that the Status/(Ready/Busy) pin does not fall during a reset (refer to Status/(Ready/Busy) section for more details).

Latch Enable (L). The Bus Interface is configured to latch the Address Inputs on the rising edge of Latch Enable, L. In synchronous bus operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL} or on the rising of Latch Enable, whichever occurs first. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL}, the latch is transparent.

Clock (K). The Clock, K, is used to synchronize the memory with the external bus during synchronous read operations. The Clock can be configured to have an active rising or falling edge. Bus signals are latched on the active edge of the Clock during synchronous bus operations. In Synchronous Burst Read mode the address is latched on the first active clock edge when Latch Enable is low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

During asynchronous bus operations the Clock is not used.

WAIT (WAIT). Wait is an output signal used during Synchronous Burst read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH} or Reset is at V_{IL}.

Status/(Ready/Busy) (STS). The STS signal exists in the TBGA64 package only (not available in the VFBGA56 package). It is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes:

- Ready/Busy - the pin is Low, V_{OL}, during program and erase operations and high impedance when the memory is ready for any read, program or erase operation.
- Status - the pin gives a pulsing signal to indicate the end or the suspension of a program or Block Erase operation.

After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured for Status mode using the Configure STS command.

When the Program/Erase Controller is idle, or suspended, STS can float High through a pull-up resistor. The use of an open-drain output allows the STS pins from several memories to be connected to a single pull-up resistor (a Low will indicate that one, or more, of the memories is busy).

STS is not Low during a reset unless the reset was applied when the Program/Erase controller was active. The Status/(Ready/Busy) pin can rise before Reset/Power-Down rises.

Program/Erase Enable (V_{PEN}). The Program/Erase Enable input, $V_{PEN,}$ is used to protect all blocks, preventing program and erase operations from affecting their data.

Program/Erase Enable must be kept High during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid any condition that would result in data corruption.

V_{SS} Ground. Ground, $V_{SS,}$ is the reference for the core power supply. It must be connected to the system ground.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 10, AC Measurement Load Circuit.

BUS OPERATIONS

There are six standard bus operations that control the device. These are Address Latch, Bus Read, Bus Write, Output Disable, Power-Down and Standby. See Table 2, Bus Operations, for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect Bus Write operations.

Address Latch. Address latch operations input valid addresses.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Address Latch.

Bus Read. Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the Common Flash Interface and the Block Protection Status.

A valid bus operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable, Output Enable and Latch Enable and keeping Write Enable High, V_{IH}. According to the Synchronous or Asynchronous Read mode selected, and to the data to be output, the WAIT signal will be either Valid or Driven (see Table 2 for details).

The data read depends on the previous command written to the memory (see Command Interface section). See Figures 11, 12, 13, 14, 15 and 16 Read AC Waveforms, and Tables 17 and 18 Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write Commands to the memory or latch addresses and input data to be programmed.

A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the Bus Write operation.

See Figures 17, 18 and 19, Write AC Waveforms, and Table 19, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are high impedance when the Output Enable is at V_{IH}.

Power-Down. The memory is in Power-Down mode when Reset/Power-Down, $\overline{RP}$, is Low. The power consumption is reduced to the Power-Down level, I_{DD2}, and the outputs are high impedance, independent of Chip Enable, Output Enable or Write Enable.

Standby. Standby disables most of the internal circuitry, allowing a substantial reduction of the current consumption. The memory is in standby when Chip Enable is at V_{IH}. The power consumption is reduced to the standby level I_{DD1} and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs.

If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

Table 2. Bus Operations

Operation		$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$\overline{L}$	WAIT	A1-A23	DQ0-DQ15
Address Latch		V_{IL}	X	V_{IH}	V_{IH}	V_{IL}	Driven	Address	Data Output or Hi-Z(2)
Bus Read	Synchronous Read: Memory Array	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Valid	Address	Data Output
	Asynchronous Read, Synchronous Read: Status Register, CFI, Electronic Signature, Block Protection Status	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Driven	Address	Data Output
Bus Write		V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	Driven	Address	Data Input
Output Disable		V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Driven	X	High Z
Power-Down		X	X	X	V_{IL}	X	High Z	X	High Z
Standby		V_{IH}	X	X	V_{IH}	X	High Z	X	High Z

Note: 1. X = Don't Care V_{IL} or V_{IH}.
2. Depends on $\overline{G}$

READ MODES

Read operations can be performed in two different ways depending on the settings in the Configuration Register. If the clock signal is 'don't care' for the data output, the read operation is asynchronous; if the data output is synchronized with clock, the read operation is synchronous.

The read mode and format of the data output are determined by the Configuration Register. (See Configuration Register section for details).

On Power-up or after a Hardware Reset the memory defaults to Asynchronous Read mode.

Asynchronous Read Modes

In Asynchronous Read operations the clock signal is 'don't care'. The device outputs the data corresponding to the address latched, that is the memory array, Status Register, Common Flash Interface, Electronic Signature or Block Protection Status depending on the command issued. CR15 in the Configuration Register must be set to '1' for asynchronous operations.

Asynchronous Read operations can be performed in three different ways, Asynchronous Latch Controlled Read, Asynchronous Random Read and Asynchronous Page Read.

Asynchronous Latch Controlled Read. In Asynchronous Latch Controlled Read operations read the address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Address Latch. Once latched, the Address Inputs can change. Set Output Enable Low, V_{IL}, to read the data on the Data Inputs/Outputs; see Figure 12, Single Asynchronous Latch Controlled Read AC Waveforms and Table 17, Asynchronous Read AC Characteristics, for details on when the output becomes valid.

See Figure 12, Single Asynchronous Latch Controlled Read AC Waveforms, and Table 17, Asynchronous Read AC Characteristics, for details.

Asynchronous Random Read. As the Latch Enable input is transparent when set Low, V_{IL}, Asynchronous Random Read operations can be performed by holding Latch Enable Low, V_{IL} throughout the bus operation.

See Figure 11, Single Asynchronous Random Read AC Waveforms, and Table 17, Asynchronous Read AC Characteristics, for details.

Asynchronous Page Read. In Asynchronous Page Read mode a Page of data is internally read and stored in a Page Buffer. Each memory page is 8 Words and has the same A4-A23, only A1-A3 may change.

The first read operation within the Page has the normal access time (t_{AVQV}), subsequent reads within the same Page have much shorter access times (t_{AVQV1}). If the Page changes then the normal, longer timings apply again.

See Figures 13, Asynchronous Page Read AC Waveforms, and Table 17, Asynchronous Read AC Characteristics, for details.

Synchronous Read Modes

In Synchronous Read mode the data output is synchronized with the clock. CR15 in the Configuration Register must be set to '0' for synchronous operations.

Synchronous Burst Read. In Synchronous Burst Read mode the data is output in bursts synchronized with the clock.

Synchronous Burst Read mode can only be used to read the memory array. For other read operations, such as Read Status Register, Read CFI, Read Electronic Signature and Block Protection Status, Single Synchronous Read or Asynchronous Read must be used.

In Synchronous Burst Read mode the flow of the data output depends on parameters that are configured in the Configuration Register.

A valid Synchronous Burst Read operation begins when the address is set on the Address Inputs, Write Enable is High, V_{IH}, and Chip Enable and Latch Enable are Low, V_{IL}, during the active edge of the Clock. The address is latched on the first active clock edge when Latch Enable is low, or on the rising edge of Latch Enable, whichever occurs first. The data becomes available for output after the X-latency specified in the Burst Control Register has expired. The output buffers are activated by setting Output Enable Low, V_{IL}. See Figures 6 and 7 for examples of Synchronous Burst Read operations.

The number of Words to be output during a Synchronous Burst Read operation can be configured as 8 Words, 16 Words. Only sequential burst is available.

See Table 18, Synchronous Read AC Characteristics and Figures 14 and 15, Synchronous Burst Read AC Waveform for details.

Single Synchronous Read. Single Synchronous Read operations are similar to Synchronous Burst Read operations except that only the first data output after the X latency is valid. Single Synchronous Reads are used to read the Status Register, CFI, Electronic Signature and Block Protection Status.

CONFIGURATION REGISTER

The Configuration Register is used to configure the type of bus access that the memory will perform. The Configuration Register bits are described in Table 3. They specify the selection of the burst length, burst type, burst latencies and the read operation. See figures 6 and 7 for examples of Synchronous Burst Read configurations.

The Configuration Register is set through the Command Interface and will retain its information until it is re-configured, the device is reset, or the device goes into Reset/Power-Down mode. The Configuration Register is read using the Read Electronic Signature Command at address 05h.

Read Select Bit (CR15). The Read Select bit, CR15, is used to switch between asynchronous and synchronous read operations. When the Read Select bit is set to '1', read operations are asynchronous; when the Read Select bit is set to '0', read operations are synchronous.

On reset or power-up the Read Select bit is set to '1' for asynchronous access.

Latency Bits (CR14-CR11). The X-Latency bits are used during Synchronous read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the Latency bits can only assume the values in Table 3, Configuration Register.

Wait Polarity Bit (CR10). In Synchronous Burst mode, the Wait signal indicates whether the output data are valid or a WAIT state must be inserted. The Wait Polarity bit is used to set the polarity of the WAIT signal. When the Wait Polarity bit is set to '0', the WAIT signal is active Low. When the Wait Polarity bit is set to '1' the Wait signal is active High (default).

Data Output Configuration Bit (CR9). The Data Output Configuration bit determines whether the output remains valid for one or two clock cycle(s). When the Data Output Configuration bit is '0' the output data is valid for one clock cycle, when the Data Output Configuration bit is '1' the output data is valid for two clock cycles (default).

The Data Output Configuration depends on the condition:

- $t_{KHKH} > t_{KHQV} + t_{QVK\_CPU}$

where t_{KHKH} is the clock period, t_{QVK_CPU} is the data setup time required by the system CPU and t_{KHQV} is the clock to data valid time. If this condition is not satisfied, the Data Output Configuration bit should be set to '1' (two clock cycles). Refer to Figure 6, X-Latency and Data Output Configuration Example.

Wait Configuration Bit (CR8). In Burst mode the Wait Configuration bit controls the timing of the Wait output pin, WAIT. When WAIT is asserted, Data is Not Valid and when WAIT is de-asserted, Data is Valid. When the Wait Configuration bit is '0' the WAIT output pin is de-asserted with Valid Data. When the Wait Configuration bit is '1' (default) the WAIT output pin is de-asserted one clock cycle before Valid Data if Data Output Configuration bit (CR9) is '0', or two clock cycle before Valid Data if CR9 bit is '1'.

Burst Type Bit (CR7). The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is '0' the memory outputs from interleaved addresses; when the Burst Type bit is '1' the memory outputs from sequential addresses. Only sequential Burst Type is supported. See Table 4, Burst Type Definition, for the sequence of addresses output from a given starting address in the 8 and 16 burst length mode (CR2-CR0).

Valid Clock Edge Bit (CR6). The Valid Clock Edge bit, CR6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is '0' the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is '1' the rising edge of the Clock is active.

Burst Length Bit (CR2-CR0). The Burst Length bits set the maximum number of Words that can be output during a Synchronous Burst Read operation.

Table 3, Configuration Register gives the valid combinations of the Burst Length bits that the memory accepts; Tables 4, Burst Type Definition, give the sequence of addresses output from a given starting address for each length.

CR5, CR4 and CR3 are reserved for future use.

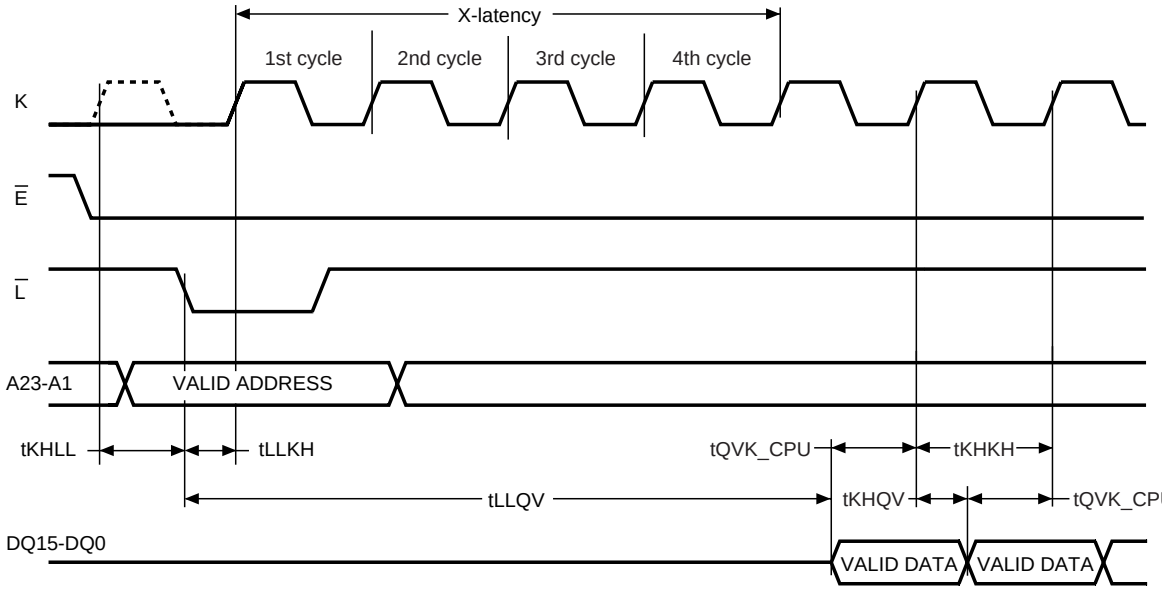
Table 3. Configuration Register

Address Bit	Mnemonic	Bit Name	Reset Value	Value	Description
16	CR15	Read Select	1	0	Synchronous Burst Read
				1	Asynchronous Read (default at power-up)
15 to 12	CR14-CR11	X-Latency	XXX	0000-0001	Reserved
				0010	X-Latency = 2
				0011	X-Latency = 3
				0100	X-Latency = 4
				0101	X-Latency = 5
				0110	X-Latency = 6
				0111	X-Latency = 7
				1000	X-Latency = 8
				1001	X-Latency = 9
				1010	X-Latency = 10
				1011-1111	Reserved
11	CR10	Wait Polarity	X	0	WAIT signal is active Low
				1	WAIT signal is active High (Default)
10	CR9	Data Output Configuration	X	0	Data is valid for one clock cycle
				1	Data is valid for two clock cycles
9	CR8	Wait Configuration	X	0	WAIT is de-asserted with Valid Data
				1	WAIT is de-asserted one clock before Valid Data (default)
8	CR7	Burst Type	X	0	Interleaved (Not Supported)
				1	Sequential (Default)
7	CR6	Valid Clock Edge	X	0	Falling Clock edge
				1	Rising Clock edge
6 to 4	CR5-CR3	Reserved			
3 to 1	CR2-CR0	Burst Length	XXX	001	Reserved
				010	8 Words
				011	16 Words
				111	Reserved

Table 4. Burst Type Definition

Starting Address	x8 Sequential	x16 Sequential
0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15
1	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0
2	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1
3	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2
4	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3
5	5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4
6	6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5
7	7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6
...	–	...
14	–	14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13
15	–	15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14
...	–	–

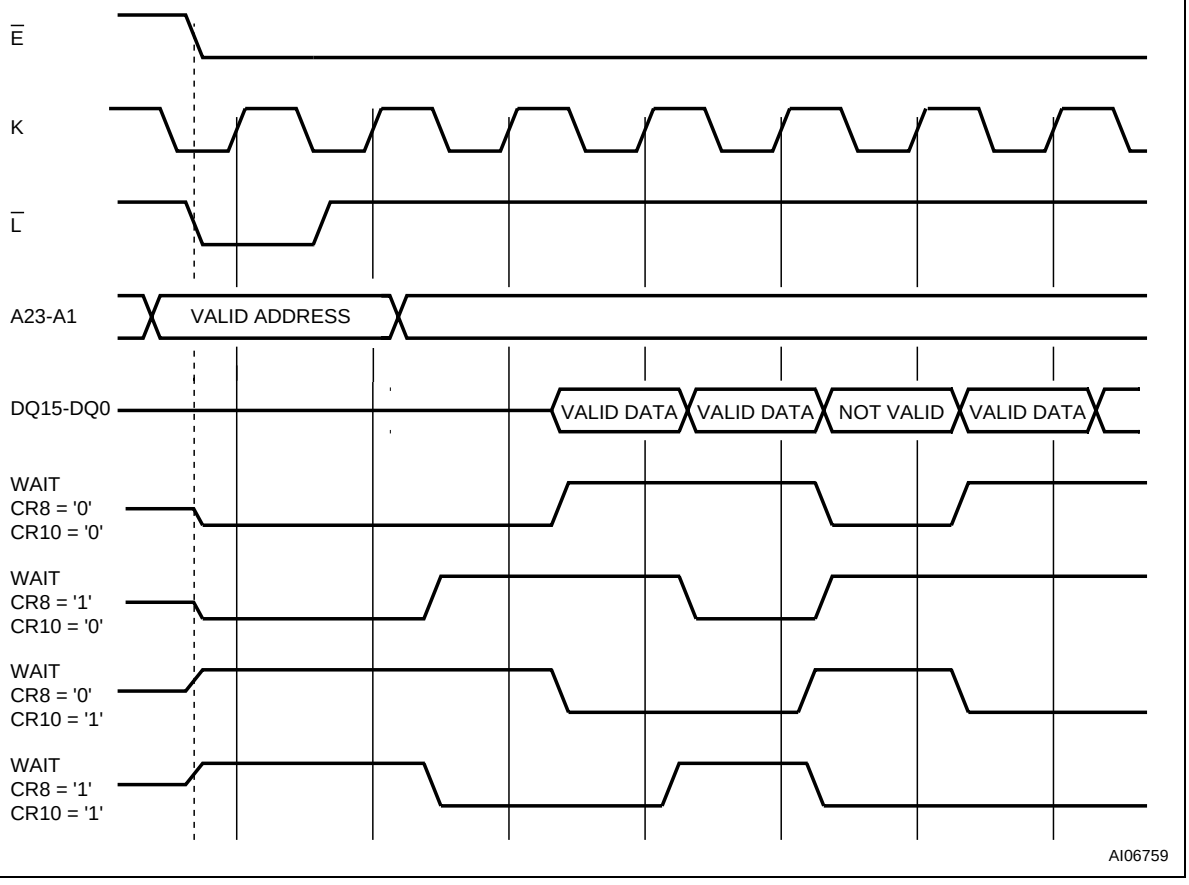
Figure 6. X-Latency and Data Output Configuration Example



Note. Settings shown: X-latency = 4, Data Output held for one clock cycle

AI06758

Figure 7. Wait Configuration Example



COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. The Commands and their codes are summarized in Tables 5, 6 and 7. Refer to these Tables in conjunction with the text descriptions below.

After power-up or a Reset operation the memory enters Read mode.

Synchronous Read operations and Latch Controlled Read operations can only be used to read the memory array. The Electronic Signature, CFI or Status Register will be read in asynchronous mode or single synchronous burst mode. Once the memory returns to Read Memory Array mode the bus will resume the setting in the Configuration Register automatically.

Table 5. Command Codes

Hex Code	Command
01h	Block Protect Confirm
03h	Set Configuration Register Confirm
10h	Alternative Word Program Setup
20h	Block Erase Setup
2Fh	Block Lock-Down Confirm
40h	Word Program Setup
50h	Clear Status Register
60h	Block Protect Setup, Block Unprotect Setup, Block Lock Down Setup and Set Configuration Register Setup
70h	Read Status Register
80h	Buffer Enhanced Factory Program Setup
90h	Read Electronic Signature
98h	Read Query
B0h	Program/Erase Suspend
B8h	Configure STS
C0h	Protection Register Program
D0h	Program/Erase Resume, Block Erase Confirm, Block Unprotect Confirm or Write to Buffer and Program Confirm, Buffer Enhanced Factory Program Confirm
E8h	Write to Buffer and Program
FFh	Read Memory Array

Read Memory Array Command

The Read Memory Array command returns the memory to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. In Read mode Bus Read operations access the memory array.

While the Program/Erase Controller is executing a Program, Erase, Block Protect, Block Unprotect or Block Lock-Down command the memory will not accept the Read Memory Array command until the operation completes.

Read Electronic Signature Command

The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code, the Block Protection Status, the Configuration Register and the Protection Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code, the Device Code, the Block Protection Status, the Configuration Register or the Protection Register until another command is issued. Refer to Table 9, Read Electronic Signature and Figure 8, Protection Register Locks and Protection Register Memory Map, for information on the addresses.

Read Query Command

The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Tables 25, 26, 27, 28, 29 and 30 for details on the information contained in the Common Flash Interface (CFI) memory area.

Read Status Register Command

The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued.

The Status Register information is present on the output data bus (DQ0-DQ7) when both Chip Enable and Output Enable are low, V_{IL}.

See the section on the Status Register and Table 12 for details on the definitions of the Status Register bits.

Clear Status Register Command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register

to '0'. One Bus Write is required to issue the Clear Status Register command.

The bits in the Status Register are sticky and do not automatically return to '0' when a new command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new command.

Block Erase Command

The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Erase times are given in Table 10.

See Appendix C, Figure 26, Block Erase Flowchart and Pseudo Code, for a suggested flowchart on using the Block Erase command.

Word Program Command

The Word Program command is used to program a single word in the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Word Program command, the second write cycle latches the address and data to be programmed in the internal state machine and starts the Program/Erase Controller.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

Write to Buffer and Program Command

The Write to Buffer and Program Command makes use of the device's 32-Word Write Buffer to speed up programming. Up to 32 Words can be loaded into the Write Buffer. The Write to Buffer and Program command dramatically reduces in-system programming time compared to the standard non-buffered Program command.

Up to 32 Words can be loaded into the Write Buffer and programmed into the memory. For best performance the 32 Words must be aligned (same A6-A23), otherwise double program time is required.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program Command. Issue the set up command with the selected memory Block Address where the program operation should occur (any address in the block where the values will be programmed can be used). Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the same block address along with the value N on the Data Inputs/Output, where N+1 is the number of Words to be programmed.
3. Use N+1 Bus Write operations to load the address and data for each Word into the Write Buffer. The address must be between Start Address and Start Address plus N, where Start Address is the first word address.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

If one address of the data pasts the block boundaries or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array. The Status Register should be cleared before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

See Appendix C, Figure 23, Write to Buffer and Program Flowchart and Pseudo Code, for a suggested flowchart on using the Write to Buffer and Program command.

Buffer Enhanced Factory Program Command

The Buffer Enhanced Factory Program command has been specially developed to speed up programming in manufacturing environments where the programming time is critical.

It is used to program one or more Write Buffer(s) of 32 Words to a block. Once the device enters Buffer Enhanced Factory Program mode, the Write Buffer can be reloaded any number of times as long as the address remains within the same block. Only one block can be programmed at a time.

The use of the Buffer Enhanced Factory Program command requires certain operating conditions:

- V_{PEN} must be set to V_{PENH}
- V_{DD} must be within operating range

- Ambient temperature, T_A must be 25°C ± 5°C
- The targeted block must be unlocked
- The start address must be aligned with the start of a 32 Word buffer boundary
- The address must remain the Start Address throughout programming.

Dual operations are not supported during the Buffer Enhanced Factory Program operation and the command cannot be suspended.

The Buffer Enhanced Factory Program Command consists of three phases: the Setup Phase, the Program and Verify Phase, and the Exit Phase, Refer to Table 7, Factory Program Command and Figure 24, Buffer Enhanced Factory Program Flowchart.

Setup Phase. The Buffer Enhanced Factory Program command requires two Bus Write cycles to initiate the command.

- The first Bus Write cycle sets up the Buffer Enhanced Factory Program command.
- The second Bus Write cycle confirms the command.

After the confirm command is issued, read operations output the contents of the Status Register. The read Status Register command must not be issued as it will be interpreted as data to program.

The Status Register P/E.C. Bit SR7 should be read to check that the P/E.C. is ready to proceed to the next phase.

If an error is detected, SR4 goes high (set to '1') and the Buffer Enhanced Factory Program operation is terminated. See Status Register section for details on the error.

Program and Verify Phase. The Program and Verify Phase requires 32 Bus Write cycles to program the 32 Words to the Write Buffer. The data is stored sequentially, starting at the first address of the Write Buffer, until the Write Buffer is full (32 Words). To program less than 32 Words, the remaining data Words should be filled with FFFFh.

Three successive steps are required to issue and execute the Program and Verify Phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first Word to be programmed. The Status Register Bank Write Status bit SR0 should be read to check that the P/E.C. is ready for the next Word.
2. Each subsequent Word to be programmed is latched with a new Bus Write operation. The address must remain the Start Address as the P/E.C. increments the address location.If any address that is not in the same block as the Start Address is given, the Program and Verify Phase terminates. Status Register bit SR0 should be read between each Bus Write cycle to check that the P/E.C. is ready for the next Word.
3. Once the Write Buffer is full, the data is programmed sequentially to the memory array. After the program operation the device automatically verifies the data and reprograms if necessary.
   When the P/E.C. is busy no Bus Write operation can be performed.

The Program and Verify phase can be repeated, without re-issuing the command, to program additional 32 Word locations as long as the address remains in the same block.

4. Finally, after all Words, or the entire block have been programmed, write one Bus Write operation to any address outside the block containing the Start Address, to terminate Program and Verify Phase.

Status Register bit SR0 must be checked to determine whether the program operation is finished. The Status Register may be checked for errors at any time but it must be checked after the entire block has been programmed.

Exit Phase. Status Register P/E.C. bit SR7 set to '1' indicates that the device has exited the Buffer Enhanced Factory Program operation and returned to Read Status Register mode. A full Status Register check should be done to ensure that the block has been successfully programmed. See the section on the Status Register for more details.

For optimum performance the Buffer Enhanced Factory Program command should be limited to a maximum of 100 program/erase cycles per block. If this limit is exceeded the internal algorithm will continue to work properly but some degradation in performance is possible. Typical program times are given in Table 10.

See Appendix C, Figure 24, Buffer Enhanced Factory Program Flowchart and Pseudo Code, for a suggested flowchart on using the Buffer Enhanced Factory Program command.

Program/Erase Suspend Command

The Program/Erase Suspend command is used to pause a Word Program, Write to Buffer and program or erase operation. The command will only be accepted during a program or an erase operation. It can be issued at any time during an erase operation but will only be accepted during a Word Program or Write to Buffer and Program command if the Program/Erase Controller is running.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (SR7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/

Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once the Program/Erase Controller Status bit (SR7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (SR2) or the Erase Suspend Status bit (SR6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see Table 10.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Clear Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was erase then the Write to Buffer and Program, and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See Appendix C, Figure 25, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 27, Erase Suspend & Resume Flowchart and Pseudo Code, for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

Set Configuration Register Command.

The Set Configuration Register command is used to write a new value to the Configuration Register (see Table 3). Two Bus Write cycles are required to issue the Set Configuration Register command. Once the command is issued the memory returns to Read mode as if a Read Memory Array command had been issued.

The value for the Configuration Register is presented on A1-A16. CR0 is on A1, CR1 on A2, etc.; the other address bits are ignored.

Block Protect Command

The Block Protect command is used to protect a block by setting the Block Protection Status bit, thus preventing Program or Erase operations from changing the data in it. All blocks are protected at power-up or reset.

Two Bus Write cycles are required to issue the Block Protect command.

- The first bus cycle sets up the Block Protect command.
- The second Bus Write cycle latches the block address.

The protection status can be monitored for each block using the Read Electronic Signature command.

Once set, the Block Protection Status bit remains set until a hardware reset or power-down/power-up. It can be cleared by issuing a Block Unprotect command. Refer to the section, Block Protection, for a detailed explanation. See Appendix C, Figure 28, Protection Operations Flowchart and Pseudo Code, for a flowchart for using the Block Protect command.

Block Unprotect Command

The Block Unprotect command is used to unprotect a block, allowing the block to be programmed or erased.

Two Bus Write cycles are required to issue the Block Unprotect command.

- The first bus cycle sets up the Block Unprotect command.
- The second Bus Write cycle latches the block address.

The protection status can be monitored for each block using the Read Electronic Signature command. Table 11 shows the protection status after issuing a Block Unprotect command. Refer to the section, Block Protection, for a detailed explanation and Appendix C, Figure 28, Protection Operations Flowchart and Pseudo Code, for a flowchart for using the Block Unprotect command.

Block Lock-Down Command

A protected or unprotected block can be locked-down by issuing the Block Lock-Down command. A locked-down block cannot be programmed or erased, or have its protection status changed when $\overline{WP}$ is Low, V_{IL}. When $\overline{WP}$ is High, V_{IH}, the Lock-Down function is disabled and the protected blocks can be individually unprotected by the Block Unprotect command.

Two Bus Write cycles are required to issue the Block Lock-Down command.

- The first bus cycle sets up the Block Protect command.
- The second Bus Write cycle latches the block address.

The protection status can be monitored for each block using the Read Electronic Signature com-

mand. Locked-Down blocks revert to the protected (and not locked-down) state when the device is reset on power-down. Table 11 shows the Protection Status after issuing a Block Lock-Down command. Refer to the section, Block Protection, for a detailed explanation and Appendix C, Figure 28, Protection Operations Flowchart and Pseudo Code, for a flowchart for using the Lock-Down command.

Protection Register Program Command

The Protection Register Program command is used to Program the user segment of the Protection Register. The segment is programmed 16 bits at a time. Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The user-programmable segment can be locked by programming bit 1 of the Protection Register Lock location to '0'. Bit 0 of the Protection Register Lock location locks the factory programmed segment and is programmed to '0' in the factory. The locking of the Protection Register is not reversible, once the lock bits are programmed no further changes can be made to the values stored in the Protection Register, see Figure 8, Protection Register Memory Map. Attempting to program a previously protected Protection Register will result in a Status Register error.

The Protection Register Program cannot be suspended. See Appendix C, Figure 29, Protection Register Program Flowchart and Pseudo Code, for the flowchart for using the Protection Register Program command.

Configure STS Command

The Configure STS command is available only in parts offered in the TFBGA64 package. It is used to configure the Status/(Ready/Busy) pin. After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured in Status mode using the Configure STS command (refer to Status/(Ready/Busy) section for more details).

Two write cycles are required to issue the Configure STS command.

- The first bus cycle sets up the Configure STS command.
- The second specifies one of the four possible configurations (refer to Table 8, Configuration Codes):
  - Ready/Busy mode
  - Pulse on Erase suspended or complete
  - Pulse on Program suspended or complete
  - Pulse on Erase/ Program suspended or complete

The device will not accept the Configure STS command while the Program/Erase controller is busy or during Program/Erase Suspend. When STS pin is pulsing it remains Low for a typical time of 250ns. Any invalid Configuration Code will set an error in the Status Register.

Table 6. Standard Commands

Command	Cycles	Bus Operations											
		1st Cycle			2nd Cycle			Subsequent			Final		
		Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array	≥ 2	Write	X	FFh	Read	RA	RD						
Read Electronic Signature	≥ 2	Write	X	90h	Read	IDA(3)	IDD(3)						
Read Status Register	2	Write	X	70h	Read	X	SRD						
Read Query	≥ 2	Write	X	98h	Read	QA(4)	QD(4)						
Clear Status Register	1	Write	X	50h									
Block Erase	2	Write	X	20h	Write	BA	D0h						
Word Program	2	Write	X	40h 10h	Write	PA	PD						
Write to Buffer and Program	4 + N	Write	BA	E8h	Write	BA	N	Write	PA	PD	Write	X	D0h
Program/Erase Suspend	1	Write	X	B0h									
Program/Erase Resume	1	Write	X	D0h									
Set Configuration Register	2	Write	X	60h	Write	CR	03h						
Block Protect	2	Write	BA	60h	Write	BA	01h						
Block Unprotect	2	Write	BA	60h	Write	BA	D0h						
Block Lock-Down	2	Write	BA	60h	Write	BA	2Fh						
Protection Register Program	2	Write	X	C0h	Write	PRA	PRD						
Configure STS command	2	Write	X	B8h	Write	X	CC						

Note: 1. X Don't Care; RA Read Address, RD Read Data, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address, PD Program Data, QA Query Address, QD Query Data, BA Any address in the Block, CR Configuration Register value, CC Configuration Code, PRA Protection Register Address, PRD Protection Register Data (see fig. 8).
2. For Identifier addresses and data refer to table 9, Read Electronic Signature.
3. For Query Address and Data refer to Appendix B, CFI.

Table 7. Factory Program Command

Command	Phase	Cycles	Bus Write Operations									
			1st		2nd		3rd		Final -1		Final	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Buffer Enhanced Factory Program	Setup	2	WA(4)	80h	WA_1	D0h						
	Program/ Verify(3)	≥32	WA_1	PD_1	WA_1	PD_2	WA_1	PD_3	WA_1	PD_{31}	WA_1	PD_{32}
	Exit	1	NOT BA_1(2)	X								

Note: 1. WA=Word Address in targeted bank, PD=Program Data, BA=Block Address, X = Don't Care.
2. WA_1 is the Start Address, NOT BA_1 = Not Block Address of WA_1.
3. The Program/Verify phase can be executed any number of times as long as the data is to be programmed to the same block.
4. Any address within the bank can be used.

Table 8. Configuration Codes

Configuration Code	DQ1	DQ0	Mode	STS Pin	Description
00h	0	0	Ready/Busy	V_{OL} during P/E operations Hi-Z when the memory is ready	The STS pin is Low during program and erase operations and high impedance when the memory is ready for any read, program or erase operation.
01h	0	1	Pulse on Erase suspended or complete	Pulse Low then High when operation completed(2)	Supplies a system interrupt pulse at the end of a Block Erase operation.
02h	1	0	Pulse on Program suspended or complete		Supplies a system interrupt pulse at the end of a Program operation.
03h	1	1	Pulse on Erase/ Program suspended or complete		Supplies a system interrupt pulse at the end of a Block Erase or Program operation.

Note: 1. DQ2-DQ7 are reserved
2. When STS pin is pulsing it remains Low for a typical time of 250ns.

Table 9. Read Electronic Signature

Code		Address (A23-A1)	Data (DQ15-DQ0)
Manufacturer Code		000000h	0020h
Device Code		000001h	8802h
Block Protection Status	Protected	SBA+02h(1)	0001h
	Unprotected		0000h
	Protected and Locked-Down		0011h
	Unprotected and Locked-Down		0010h
Configuration Register		000005h	CR
Protection Register(2)	Protection Register Lock 0	000080h	PSR0 Lock
	Protection Register Lock 1	000089h	PSR1 Lock
	Protection Sub-Register 0 (PSR0)	000081h to 000088h	PRD
	Protection Sub-Registers 1 to 16 (PSR1-PSR16)	00008Ah to 000109h	PRD

Note: 1. SBA is the Start Base Address of each block, CR is Configuration Register data, PRD is Protection Register Data.
2. Base Address, refer to Figure 8 for more information.

Figure 8. Protection Register Locks and Protection Register Memory Map

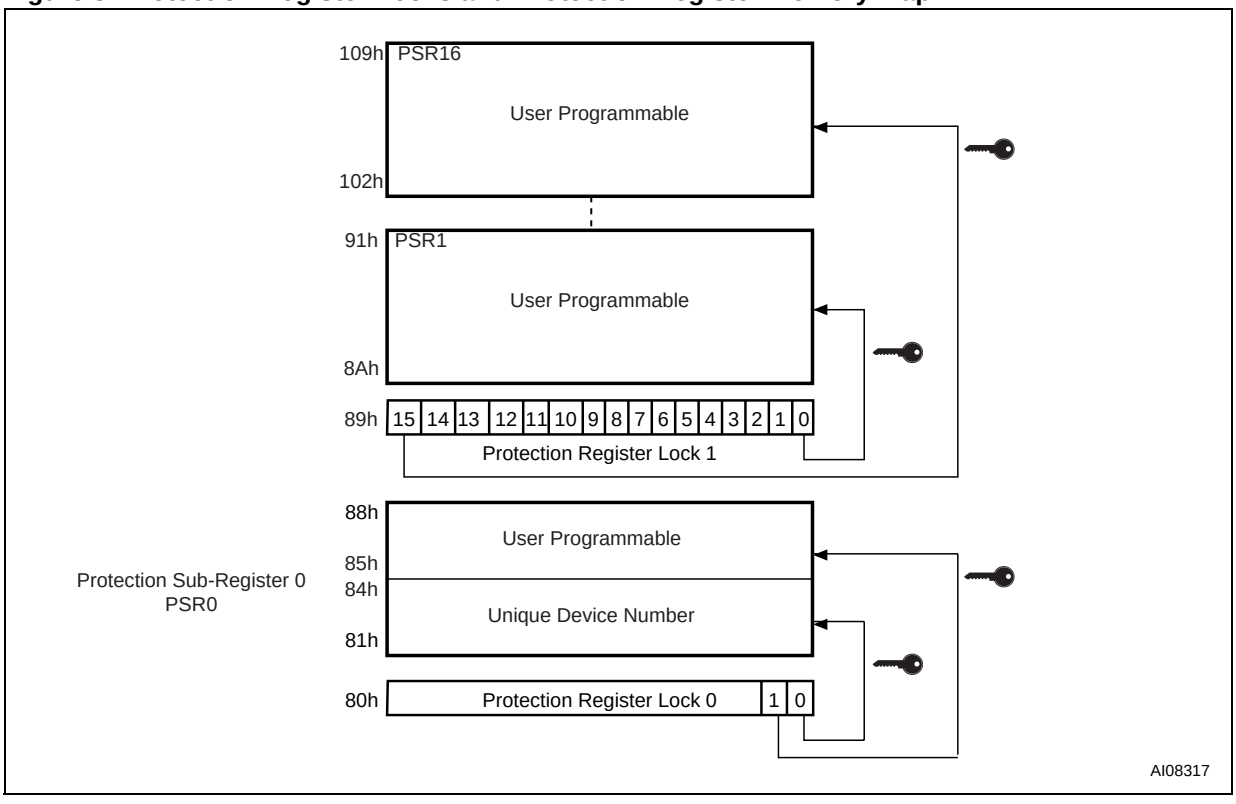


Table 10. Program, Erase Times and Program Erase Endurance Cycles

Parameters	M58LW128H			Unit
	Min	Typ(1,2)	Max(2)	
Block (1Mb) Erase		1	4(4)	s
Chip Program (Write to Buffer)		83.9	252(4)	s
Chip Erase Time		128	512(4)	s
Program Write Buffer		320	960	µs
Word/Byte Program Time (Word/Byte Program command)		150	450(4)	µs
Buffered Enhanced Factory Program Time		288	864	µs
Program Suspend Latency Time		20	25 (5)	µs
Erase Suspend Latency Time		20	25 (5)	µs
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	20			years

Note: 1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Effective byte programming time 6µs, effective word programming time 12µs.
4. Maximum value measured at worst case conditions for both temperature and V_{DD} after 100,000 program/erase cycles.
5. Maximum value measured at worst case conditions for both temperature and V_{DD}.

BLOCK PROTECTION

The M58LW128H features an instant, individual block protection scheme that allows any block to be protected or unprotected with no latency. This protection scheme has three levels of protection.

- Protect/Unprotect - this first level allows software-only control of block protection.
- Lock-Down - this second level requires hardware interaction before the protection can be changed.
- $V_{PP} \leq V_{PPLK}$ - the third level offers a complete hardware protection against program and erase on all blocks.

The protection status of each block can be set to Protected, Unprotected, and Locked-Down. Table 11, defines all of the possible protection states (WP, DQ1, DQ0), and Appendix C, Figure 28, shows a flowchart for the protection operations.

Reading a Block's Protection Status

The protection status of every block can be read in the Read Electronic Signature mode of the device. To enter this mode write 90h to the device. Subsequent reads at the address specified in Table 9, will output the protection status of that block. The protection status is represented by DQ0 and DQ1. DQ0 indicates the Block Protect/Unprotect status and is set by the Block Protect command and cleared by the Block Unprotect command. It is also automatically set when entering Lock-Down. DQ1 indicates the Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by a hardware reset or power-down.

The following sections explain the operation of the protection system.

Protected State

The default status of all blocks on power-up or after a hardware reset is Protected (states (0,0,1) or (1,0,1)). Protected blocks are fully protected from any program or erase. Any program or erase operations attempted on a protected block will return an error in the Status Register. The Status of a Protected block can be changed to Unprotected or Lock-Down using the appropriate software commands. An Unprotected block can be Protected by issuing the Block Protect command.

Unprotected State

Unprotected blocks (states (0,0,0), (1,0,0) (1,1,0)), can be programmed or erased. All unprotected blocks return to the Protected state after a hardware reset or when the device is powered-down. The status of an unprotected block can be changed to Protected or Locked-Down using the appropriate software commands. A protected block can be unprotected by issuing the Block Unprotect command.

Lock-Down State

Blocks that are Locked-Down (state (0,1,x)) are protected from program and erase operations (as for Protected blocks) but their protection status cannot be changed using software commands alone. A Protected or Unprotected block can be Locked-Down by issuing the Block Lock-Down command. Locked-Down blocks revert to the Protected state when the device is reset or powered-down.

The Lock-Down function is dependent on the $\overline{WP}$ input pin. When $\overline{WP}$=0 (V_{IL}), the blocks in the Lock-Down state (0,1,x) are protected from program, erase and protection status changes. When $\overline{WP}$=1 (V_{IH}) the Lock-Down function is disabled (1,1,x) and Locked-Down blocks can be individually unprotected to the (1,1,0) state by issuing the software command, where they can be erased and programmed. These blocks can then be re-protected (1,1,1) and unprotected (1,1,0) as desired while $\overline{WP}$ remains high. When $\overline{WP}$ is Low, blocks that were previously Locked-Down return to the Lock-Down state (0,1,x) regardless of any changes made while $\overline{WP}$ was High. Device reset or power-down resets all blocks, including those in Lock-Down, to the Protected state.

Protection Operations During Erase Suspend

Changes to block protection status can be performed during an erase suspend by using the standard protection command sequences to unprotect, protect or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change the block protection during an erase operation, first write the Erase Suspend command, then check the status register until it indicates that the erase operation has been suspended. Next write the desired Protect command sequence to a block and the protection status will be changed. After completing any desired protection, read, or program operations, resume the erase operation with the Erase Resume command.

If a block is protected or locked-down during an erase suspend of the same block, the protection status bits will be changed immediately, but when the erase is resumed, the erase operation will complete. Protection operations cannot be performed during a program suspend.

Table 11. Protection Status

Current Protection Status(1) (WP, DQ1, DQ0)		Next Protection Status(1) (WP, DQ1, DQ0)			
Current State	**Program/Erase Allowed**	**After Block Protect Command**	**After Block Unprotect Command**	**After Block Lock-Down Command**	**After $\overline{WP}$ transition**
1,0,0	yes	1,0,1	1,0,0	1,1,1	0,0,0
1,0,1(2)	no	1,0,1	1,0,0	1,1,1	0,0,1
1,1,0	yes	1,1,1	1,1,0	1,1,1	0,1,1
1,1,1	no	1,1,1	1,1,0	1,1,1	0,1,1
0,0,0	yes	0,0,1	0,0,0	0,1,1	1,0,0
0,0,1(2)	no	0,0,1	0,0,0	0,1,1	1,0,1
0,1,1	no	0,1,1	0,1,1	0,1,1	1,1,1 or 1,1,0 (3)

Note: 1. The protection status is defined by the write protect pin and by DQ1 ('1' for a locked-down block) and DQ0 ('1' for a protected block) as read in the Read Electronic Signature command with A2 = V_{IH} and A1 = V_{IL}.
2. All blocks are protected at power-up, so the default configuration is 001 or 101 according to $\overline{WP}$ status.
3. A $\overline{WP}$ transition to V_{IH} on a protected block will restore the previous DQ0 value, giving a 111 or 110.

STATUS REGISTER

The Status Register provides information on the current or previous Program, Erase, Block Protect, Block Unprotect or Block Lock-Down operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase, Block Protect, Block Unprotect, Block Lock-Down and Program/Erase Resume commands. The Status Register can be read from any address.

The Status Register can only be read using Asynchronous Bus Read or Single Synchronous Read operations. Once the memory returns to Read Memory Array mode the bus will resume the setting in the Configuration Register automatically.

The contents of the Status Register can be updated during an erase or program operation by toggling the Output Enable pin or by dis-activating (Chip Enable, V_{IH}) and then reactivating (Chip Enable and Output Enable, V_{IL}) the device.

Status Register bits SR5, SR4, SR3 and SR1 are associated with various error conditions and can only be reset with the Clear Status Register command. The Status Register bits are summarized in Table 12, Status Register Bits. Refer to Table 12 in conjunction with the following text descriptions.

Program/Erase Controller Status Bit (SR7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low, V_{OL}, the Program/Erase Controller is active and all other Status Register bits are High Impedance except during and after a Buffer Enhanced Factory Program command (in this case SR0 isn't High Impedance).

When the bit is High, V_{OH}, the Program/Erase Controller is inactive.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, Block Protect, Block Unprotect and Block Lock-Down operations the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status and Block Protection Status bits should be tested for errors.

Erase Suspend Status Bit (SR6). The Erase Suspend Status bit indicates that an erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation. When the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status Bit (SR5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Erase Status bit is Low, V_{OL}, the memory has successfully verified that the block has erased correctly or all blocks have been unprotected successfully. When the Erase Status bit is High, V_{OH}, the erase operation has failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH}.

- If only the Erase Status bit (SR5) is set High, V_{OH}, then the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly.
- If the failure is due to an erase with V_{PEN} low, V_{OL}, then V_{PEN} Status bit (SR3) is also set High, V_{OH}.
- If the failure is due to an erase on a protected block then Block Protection Status bit (SR1) is also set High, V_{OH}.
- If the failure is due to a program or erase incorrect command sequence then Program Status bit (SR4) is also set High, V_{OH}.

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new program or erase command is issued, otherwise the new command will appear to fail.

Program Status Bit (SR4). The Program Status bit is used to identify a Program or Block Protect failure. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Program Status bit is Low, V_{OL}, the memory has successfully verified that the Write Buffer has programmed correctly or the block is protected. When the Program Status bit is High, V_{OH}, the program has failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH}.

- If only the Program Status bit (SR4) is set High, V_{OH}, then the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the Write Buffer has programmed correctly.
- If the failure is due to a program or block protect with V_{PEN} low, V_{OL}, then V_{PEN} Status bit (SR3) is also set High, V_{OH}.
- If the failure is due to a program on a protected block then Block Protection Status bit (SR1) is also set High, V_{OH}.
- If the failure is due to a program or erase incorrect command sequence then Erase Status bit (SR5) is also set High, V_{OH}.

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new program or erase command is issued, otherwise the new command will appear to fail.

V_{PEN} Status Bit (SR3). The V_{PEN} Status bit can be used to identify if a Program, Erase, Block Protect or Block Unprotect operation has been attempted when V_{PEN} is Low, V_{IL}.

When the V_{PEN} Status bit is Low, V_{OL}, no Program, Erase, Block Protect or Block Unprotect operations have been attempted with V_{PEN} Low, V_{IL}, since the last Clear Status Register command, or hardware reset. When the V_{PEN} Status bit is High, V_{OH}, a Program, Erase, Block Protect or Block Unprotect operation has been attempted with V_{PEN} Low, V_{IL}.

Once set High, the V_{PEN} Status bit can only be reset by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program, Erase, Block Protect or Block Unprotect command is issued, otherwise the new command will appear to fail.

Program Suspend Status Bit (SR2). The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status Bit (SR1). The Block Protection Status bit can be used to identify if a program or erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is Low, V_{OL}, no program or erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset. When the Block Protection Status bit is High, V_{OH}, a program (SR4 set High) or erase (SR5 set High) operation has been attempted on a protected block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new program or erase command is issued, otherwise the new command will appear to fail.

Buffer Enhanced Factory Program Status Bit (SR0). The Buffer Enhanced Factory Program Status bit can be used to check the progress of Buffer Enhanced Factory Program operations. SR0 High, V_{OH}, indicates that the operation is in progress. SR0 Low, V_{OL}, indicates that the operation has completed.

For all other operations, SR0 is Low, V_{OL}, when P.E/C. is ready, otherwise SR0 is High Impedance.

Table 12. Status Register Bits

OPERATION	SR7	SR 6	SR5	SR4	SR3	SR2	SR1	SR0	STS (1)	Result (Hex)
Program/Erase Controller active	0	Hi-Z							V_{OL}	N/A
Write Buffer not ready	0	Hi-Z							V_{OL}	N/A
Write Buffer ready	1	0	0	0	0	0	0	0	Hi-Z	80h
Write Buffer ready in Erase Suspend	1	1	0	0	0	0	0	0	Hi-Z	C0h
Write Buffer ready, device busy in Buffer Enhanced Factory Program	0	0	0	0	0	0	0	0	Hi-Z	00h
Write Buffer is not available, device is busy in Buffer Enhanced Factory Program	0	0	0	0	0	0	0	1	Hi-Z	N/A
Program suspended	1	0	0	0	0	1	0	0	Hi-Z	84h
Program suspended in Erase Suspend	1	1	0	0	0	1	0	0	Hi-Z	C4h
Program/Block Protect completed successfully	1	0	0	0	0	0	0	0	Hi-Z	80h
Program completed successfully in Erase Suspend	1	1	0	0	0	0	0	0	Hi-Z	C0h
Program/Block Protect failure due to incorrect command sequence	1	0	1	1	0	0	0	0	Hi-Z	B0h
Program failure due to incorrect command sequence in Erase Suspend	1	1	1	1	0	0	0	0	Hi-Z	F0h
Program/Block Protect failure due to V_{PEN} error	1	0	0	1	1	0	0	0	Hi-Z	98h
Program failure due to V_{PEN} error in Erase Suspend	1	1	0	1	1	0	0	0	Hi-Z	D8h
Program failure due to Block Protection	1	0	0	1	0	0	1	0	Hi-Z	92h
Program failure due to Block Protection in Erase Suspend	1	1	0	1	0	0	1	0	Hi-Z	D2h
Program/Block Protect failure due to cell failure	1	0	0	1	0	0	0	0	Hi-Z	90h
Program failure due to cell failure in Erase Suspend	1	1	0	1	0	0	0	0	Hi-Z	D0h
Erase Suspended	1	1	0	0	0	0	0	0	Hi-Z	C0h
Erase/Blocks Unprotect completed successfully	1	0	0	0	0	0	0	0	Hi-Z	80h
Erase/Blocks Unprotect failure due to incorrect command sequence	1	0	1	1	0	0	0	0	Hi-Z	B0h
Erase/Blocks Unprotect failure due to V_{PEN} error	1	0	1	0	1	0	0	0	Hi-Z	A8h
Erase failure due to Block Protection	1	0	1	0	0	0	1	0	Hi-Z	A2h
Erase/Blocks Unprotect failure due to failed cells in Block	1	0	1	0	0	0	0	0	Hi-Z	A0h

Note: 1. STS Configuration Code is 00h, the device is in Ready/Busy mode.

MAXIMUM RATING

Stressing the device above the ratings listed in Table 13, Absolute Maximum Ratings, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 13. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	150	°C
V_{IO}	Input or Output Voltage	–0.6	V_{DDQ} +0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.6	5.0	V

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 14, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 14. Operating and AC Measurement Conditions

Parameter		M58LW128H		Units
		115		
		Min	Max	
Supply Voltage (V_{DD})		2.7	3.6	V
Input/Output Supply Voltage (V_{DDQ})		1.8	V_{DD}	V
Ambient Temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load Capacitance (C_L)		30		pF
Clock Rise and Fall Times			3	ns
Input Rise and Fall Times			4	ns
Input Pulses Voltages		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages		0.5 V_{DDQ}		V

Figure 9. AC Measurement Input Output Waveform

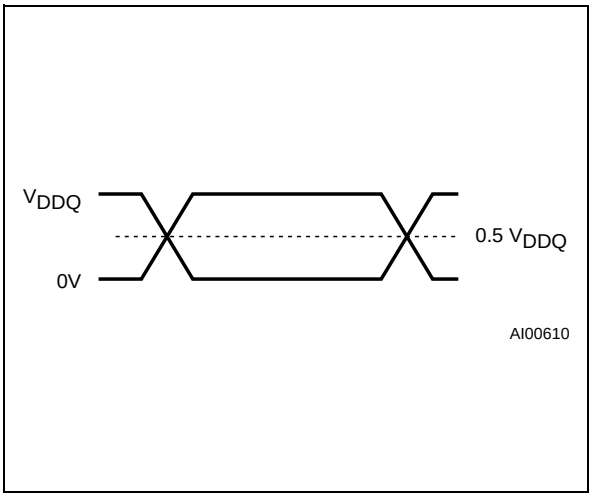


Figure 10. AC Measurement Load Circuit

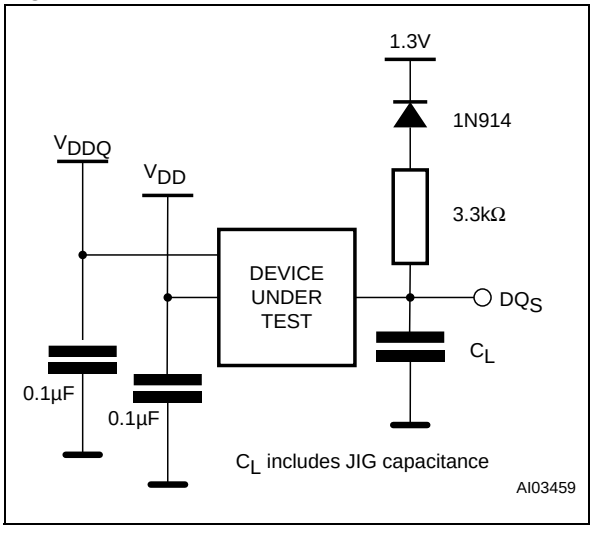


Table 15. Capacitance

Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Note: 1. T_A = 25°C, f = 1 MHz
2. Sampled only, not 100% tested.

Table 16. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{DDQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{DDQ}$		±5	µA
I_{DD}	Supply Current (Random Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{add} = 6MHz		20	mA
I_{DDB}	Supply Current (Burst Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f_{clock} = 50MHz		30	mA
I_{DD1}	Supply Current (Standby)	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		40	µA
I_{DD2}	Supply Current (Reset/Power-Down)	$\overline{RP} = V_{IL}$		40	µA
I_{DD3}	Supply Current (Program or Erase, Block Protect, Block Unprotect, Block Lock-Down)	program or erase operation in progress		30	mA
I_{DD4}	Supply Current (Erase/Program Suspend)	$\overline{E} = V_{IH}$		40	µA
V_{IL}	Input Low Voltage		–0.5	V_{DDQ} x 0.3	V
V_{IH}	Input High Voltage		V_{DDQ} x 0.7	V_{DDQ} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.2		V
V_{LKO}	V_{DD} Lock-Out Voltage			2	V
V_{PPLK}	V_{PP} Lock-Out Voltage			1	V

Figure 11. Single Asynchronous Random Read AC Waveforms

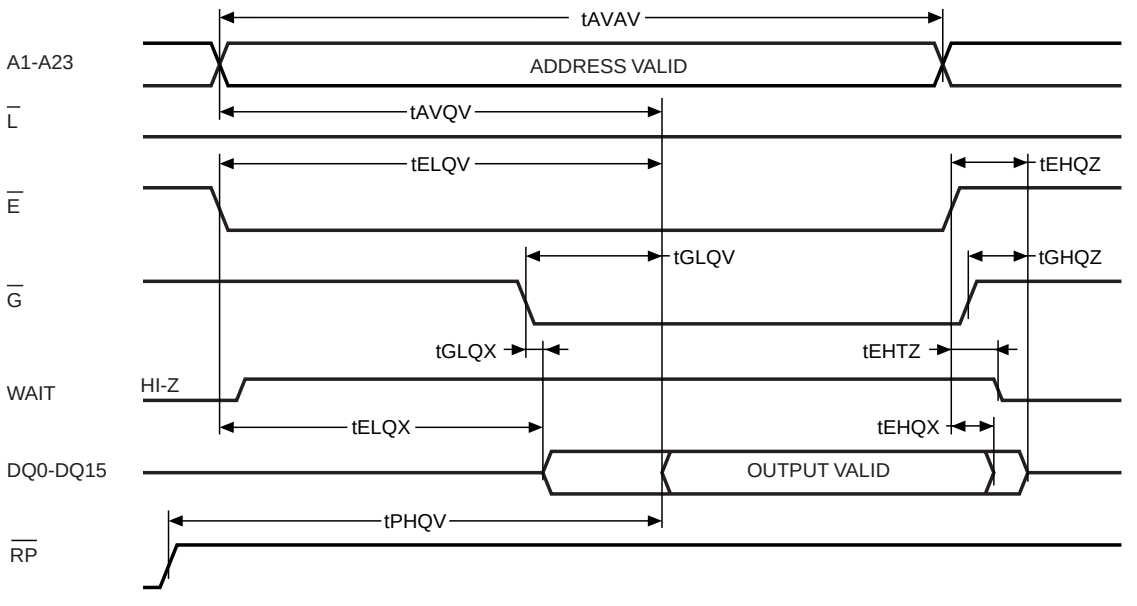


Figure 12. Single Asynchronous Latched Controlled Read AC Waveforms

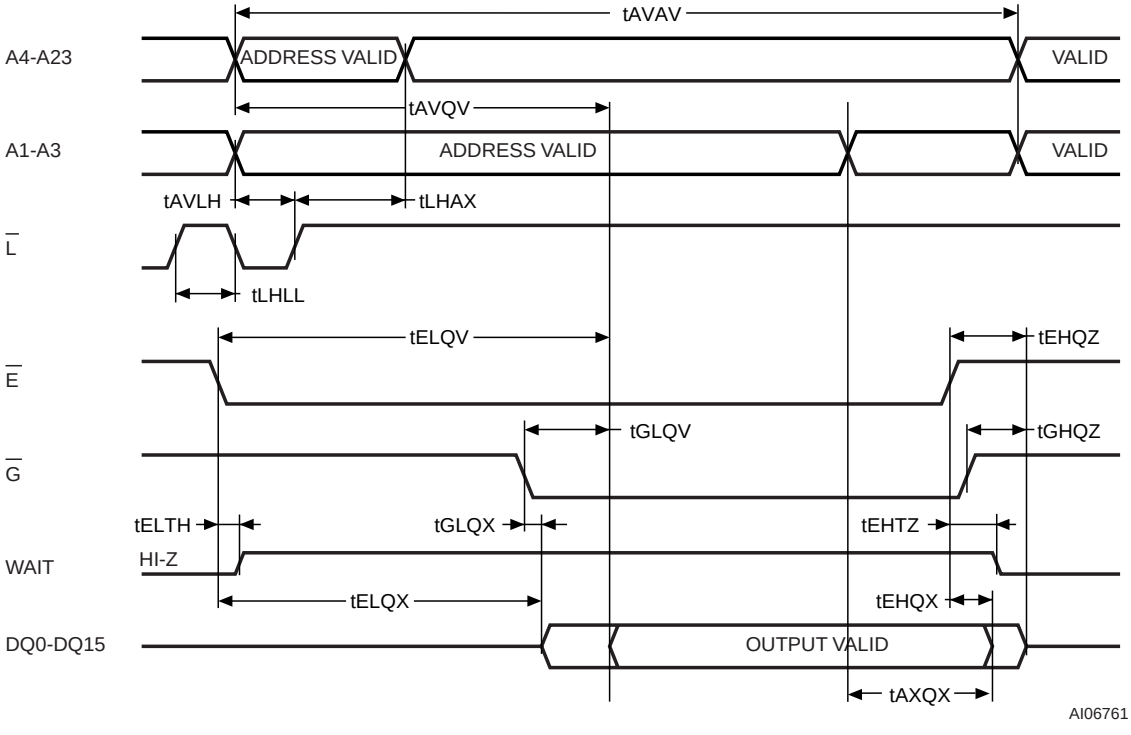


Figure 13. Asynchronous Page Read AC Waveforms

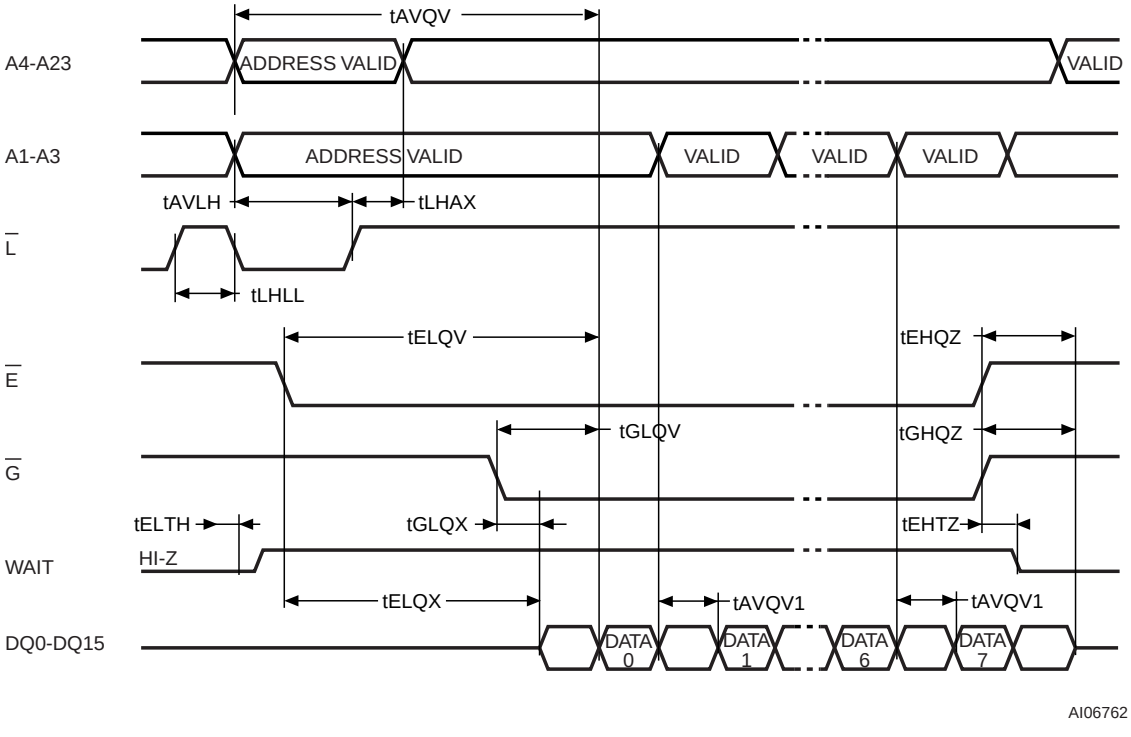


Table 17. Asynchronous Read AC Characteristics

	Symbol	Alt	Parameter	M58LW128H			Unit
				115			
				V_{DD}	2.7V to 3.3V	2.7V to 3.6V	
				V_{DDQ}	1.65V to 1.95V	2.375V to 3.6V	
Read Timings	t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	Min	115	115	ns
	t_{AVQV} (1)	t_{ACC}	Address Valid to Output Valid (Random)	Max	115	115	ns
	t_{AVQV1} (1)	t_{PAGE}	Address Valid to Output Valid (Page)	Max	30	25	ns
	t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	Max	115	115	ns
	t_{ELQX}	t_{LZ}	Chip Enable Low to Output Transition	Min	0	0	ns
	t_{EHQX} (3)	t_{OH}	Chip Enable High to Output Transition	Min	0	0	ns
	t_{EHQZ} (3)	t_{HZ}	Chip Enable High to Output Hi-Z	Max	25	25	ns
	t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	Max	30	25	ns
	t_{GLQX} (2)	t_{OLZ}	Output Enable Low to Output Transition	Min	0	0	ns
	t_{GHQX} (3)	t_{OH}	Output Enable High to Output Transition	Min	0	0	ns
	t_{GHQZ} (3)	t_{DF}	Output Enable High to Output Hi-Z	Max	25	25	ns
	t_{PHQV}		$\overline{RP}$ High to Output Valid	Max	190	180	ns
Latch Timings	t_{AVLH}	t_{AVADVH}	Address Valid to Latch Enable High	Min	9	7	ns
	t_{ELLH}	t_{ELADVH}	Chip Enable Low to Latch Enable High	Min	9	7	ns
	t_{LHAX} (4)	t_{ADVHAX}	Latch Enable High to Address Transition	Min	10	8	ns
	t_{LHLL}	$t_{ADVHADVL}$	Latch Enable High to Latch Enable Low	Min	12	10	ns
	t_{LLLH}	$t_{ADVLADVH}$	Latch Enable Pulse Width	Min	12	10	ns
	t_{LLQV}	t_{ADVLQV}	Latch Enable Low to Output Valid (Random)	Max	115	115	ns
	t_{AXQX}		Address Change to Output Transition (5)	Min	0	0	ns

Note: 1. For devices configured in Word Read mode $t_{AVQV1} = t_{AVQV}$.
2. $\overline{G}$ may go Low up to $t_{ELQV} - t_{GLQV}$ after $\overline{E}$ goes Low without any impact on t_{ELQV}.
3. Sampled, not 100% tested.
4. The Address remains Valid in Synchronous Burst mode during t_{KHAX} or t_{LHAX}, whichever timing is satisfied first.
5. Refer only to address A1-A3 if $\overline{L}$ is not active otherwise to A1-A23.

Figure 14. Single Synchronous Burst Read AC Waveform

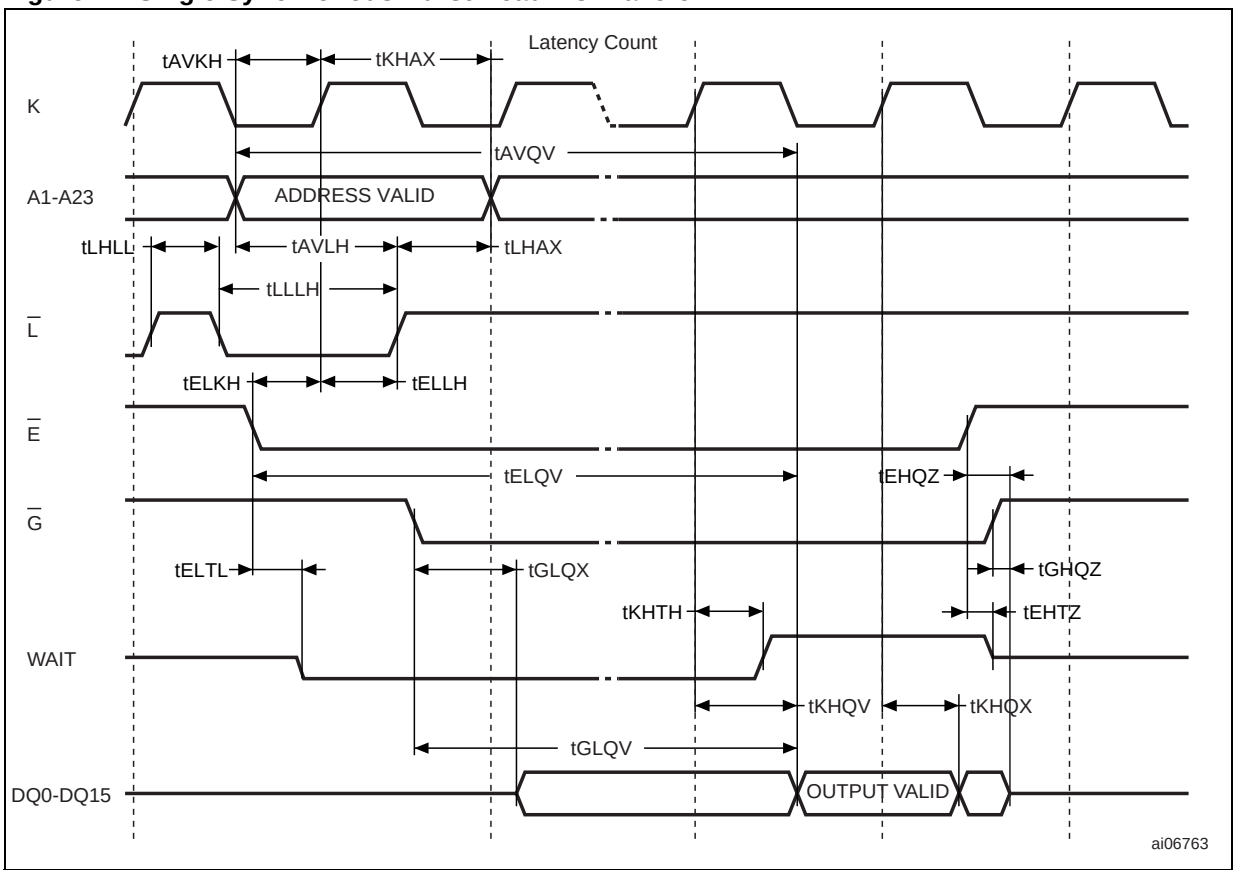
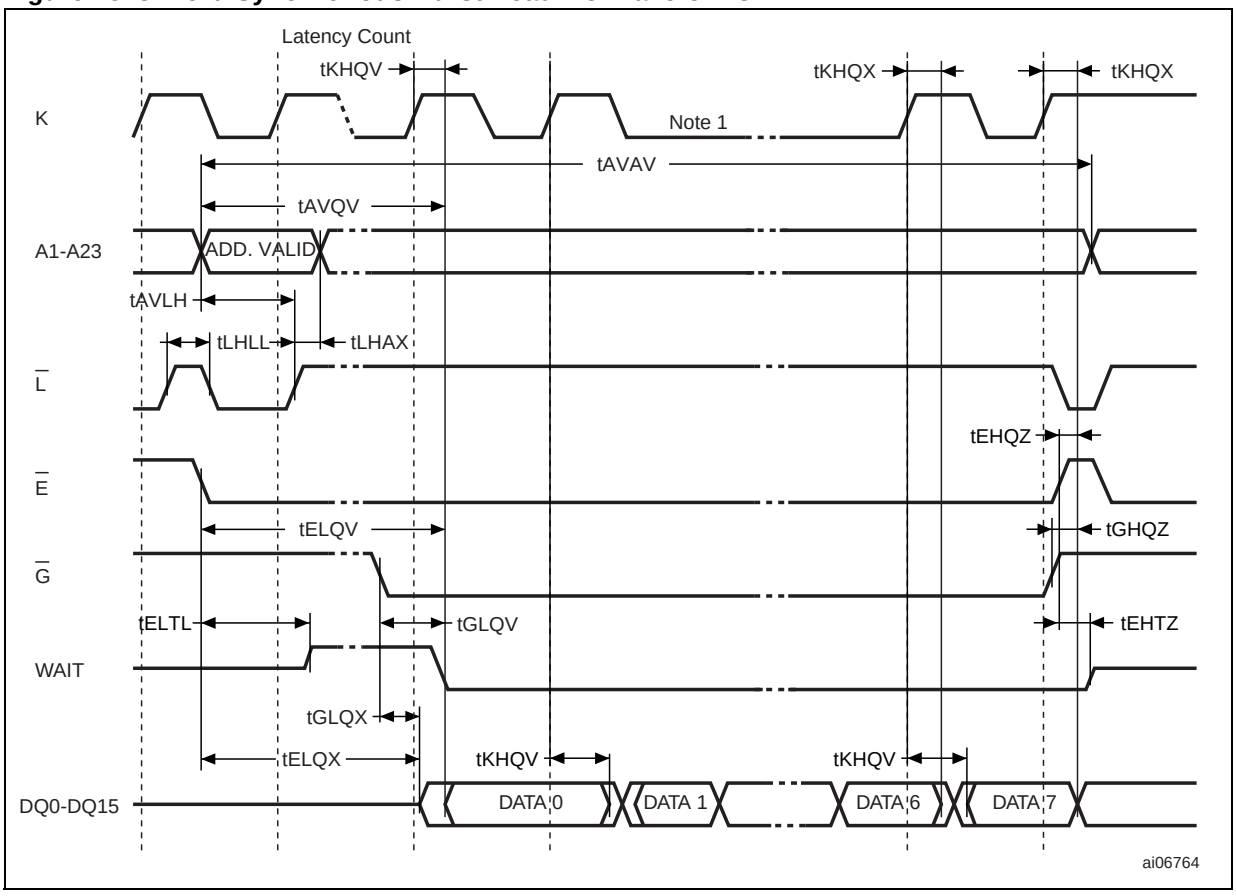


Figure 15. 8 Word Synchronous Burst Read AC Waveforms



Note: Asynchronous Read CR15 = 1

Figure 16. Clock input AC Waveform

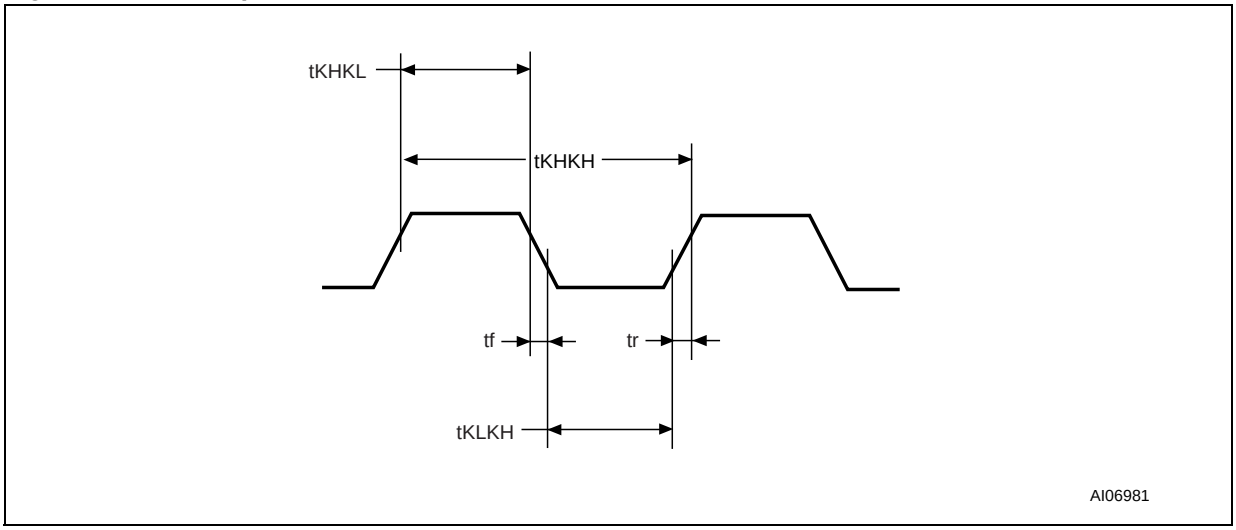


Table 18. Synchronous Read AC Characteristics

Symbol		Alt	Parameter	M58LW128H			Unit
				115			
				V_{DD}	2.7V to 3.3V	2.7V to 3.6V	
				V_{DDQ}	1.65V to 1.95V	2.375V to 3.6V	
Synchronous Read Timings	t_{AVKH}	t_{AVCLKH}	Address Valid to Clock High	Min	9	7	ns
	t_{ELKH}	t_{ELCLKH}	Chip Enable Low to Clock High	Min	9	7	ns
	t_{ELTL} (2) t_{ELTH}		Chip Enable Low to Wait Low Chip Enable Low to Wait High	Max	30	25	ns
	t_{EHTZ}		Chip Enable High to Wait Hi-Z	Max	30	25	ns
	t_{KHAX} (1)	t_{CLKHAX}	Clock High to Address Transition	Min	10	8	ns
	t_{KHLL}		Clock High to Latch Enable Low	Min	3	3	ns
	t_{KHQV} (2)	t_{CLKHQV}	Clock High to Output Valid Clock High to WAIT Valid	Max	15	13	ns
	t_{KHQX}	t_{CLKHQX}	Clock High to Output Transition Clock High to WAIT Transition	Min	3	3	ns
	t_{KHTH} (3)		Clock High to Wait High	Max	15	13	ns
	t_{LLKH}		Latch Enable Low to Clock High	Min	9	7	ns
Clock Specifications	t_{KHKH} (2)	t_{CLK}	Clock Period (f = 50MHz)	Min	20		ns
			Clock Period (f = 66MHz)	Min		15	ns
	t_{KHKL} (2) t_{KLKH}		Clock High to Clock Low Clock Low to Clock High	Min	7	4.5	ns
	t_f (2) t_r		Clock Fall or Rise Time	Max	3	3	ns

Note: 1. The Address remains Valid in Synchronous Burst mode during t_{KHAX} or t_{LHAX}, whichever timing is satisfied first.
2. The clock duty cycle should be around 50%.
3. Applies only to subsequent Synchronous Read cycles.

Figure 17. Asynchronous Write AC Waveform, Write Enable Controlled

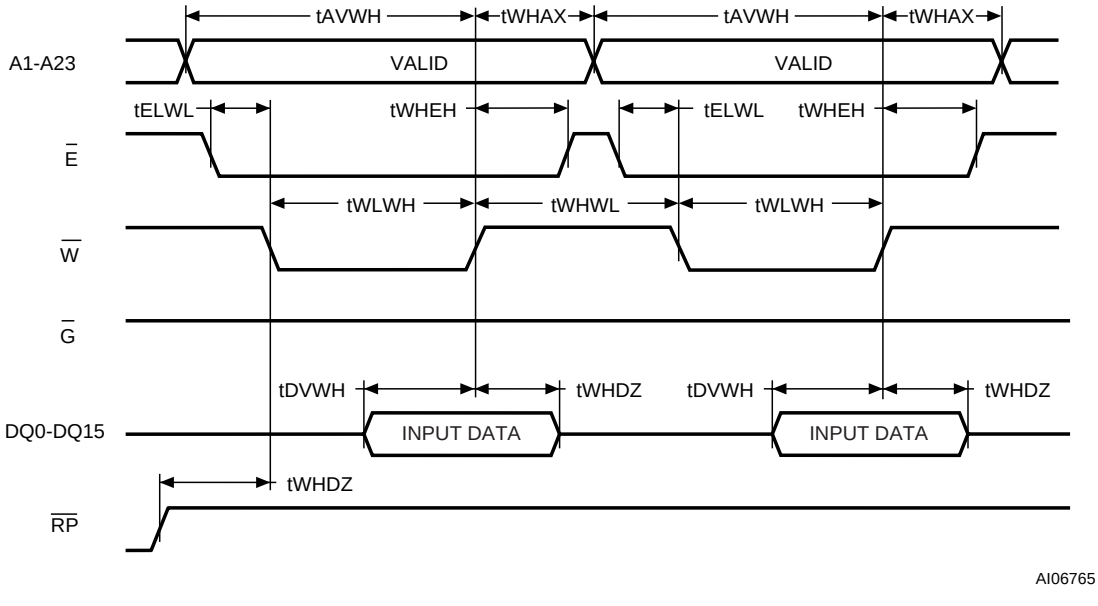


Figure 18. Asynchronous Read/Write AC Waveform

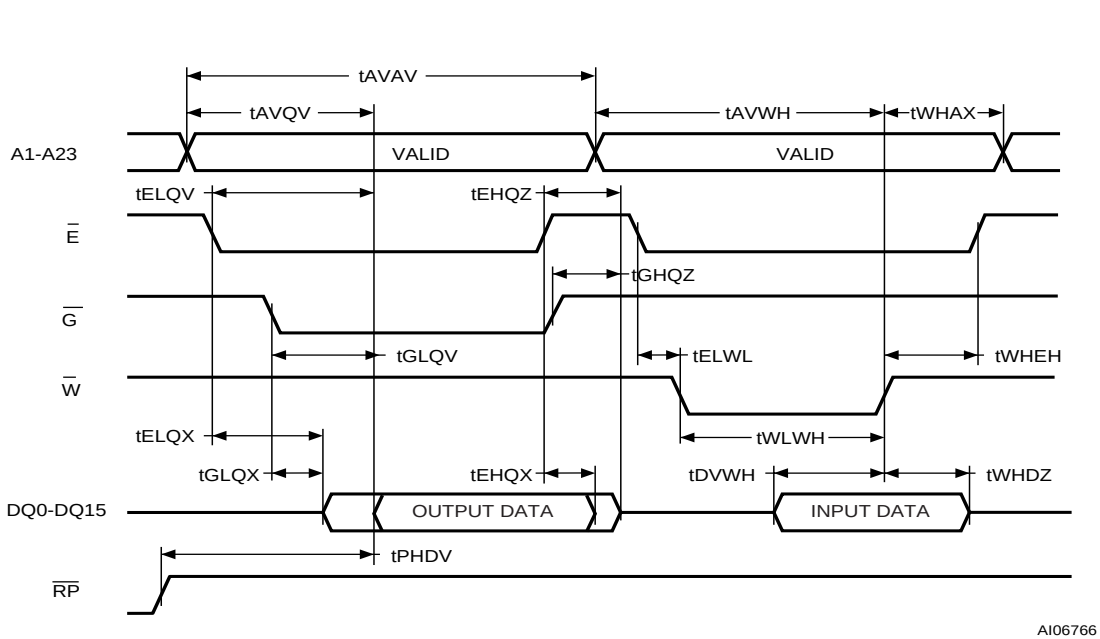


Figure 19. Asynchronous Write/Read AC Waveform

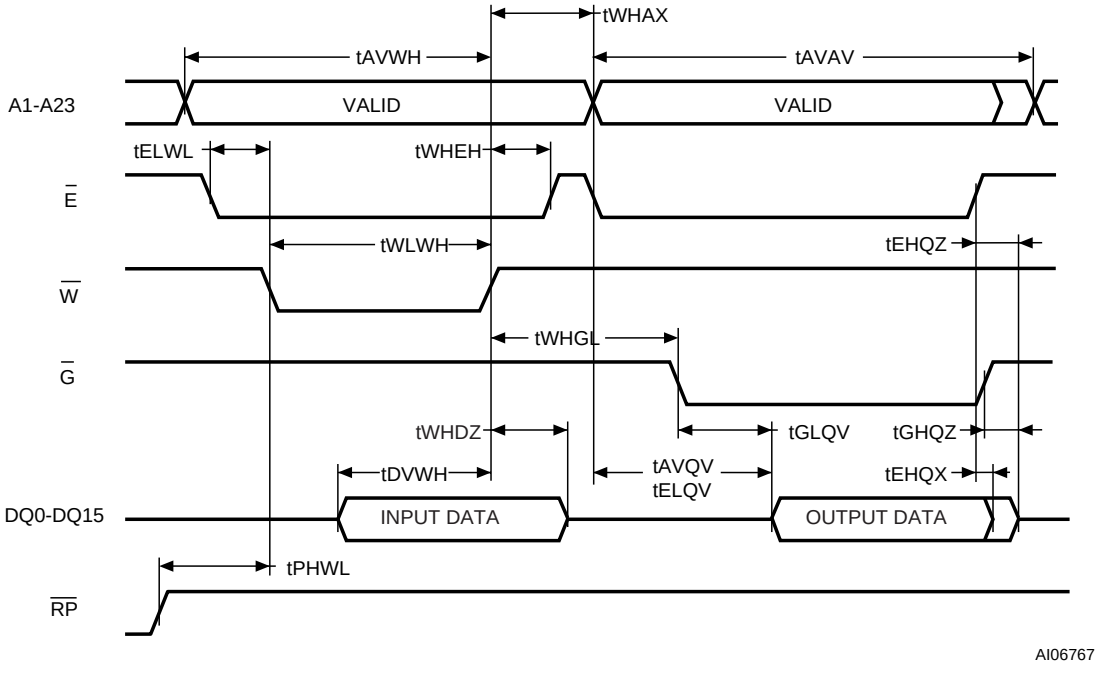
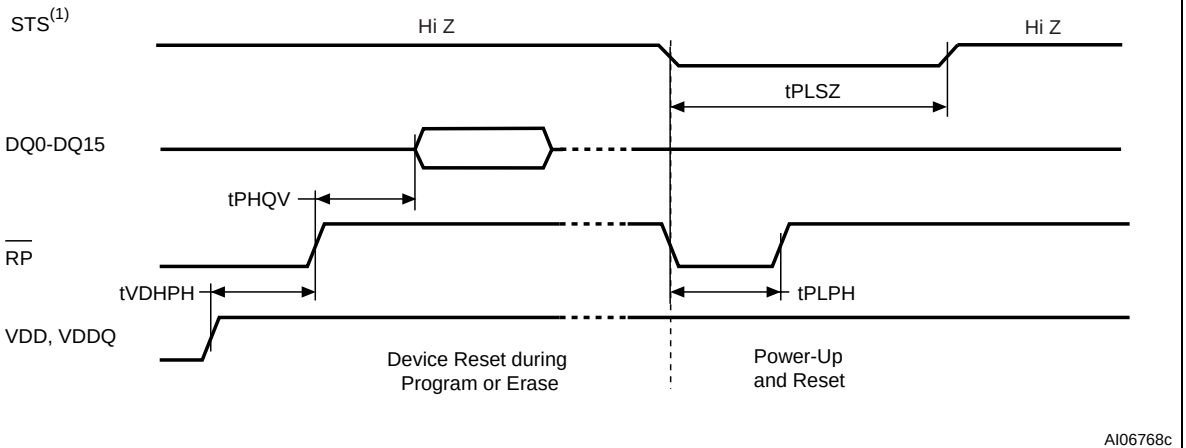


Table 19. Write AC Characteristics

Symbol	Parameter	M58LW128H			Unit
		115			
		V_{DD}	2.7V to 3.3V	2.7V to 3.6V	
		V_{DDQ}	1.65V to 1.95V	2.375V to 3.6V	
t_{AVWH}	Address Valid to Write Enable High	Min	55	55	ns
t_{DVWH}	Data Valid to Write Enable High	Min	60	60	ns
t_{ELWL}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{PHWL} (2)	$\overline{RP}$ High to Write Enable Low	Min	190	180	ns
t_{WHAX}	Write Enable High to Address Transition	Min	0	0	ns
t_{WHDZ}	Write Enable High to Data Hi-Z	Min	0	0	ns
t_{WHEH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	Write Enable High to Write Enable Low	Min	35	30	ns
t_{WLWH} (3)	Write Enable Low to Write Enable High	Min	60	60	ns
t_{WHGL}	Write Recovery Before Read	Min	35	35	ns

Note: 1. For other parameters please refer to Table 17, Asynchronous Read AC Characteristics.
2. Read operations can be initiated and terminated by either $\overline{E}$ or $\overline{W}$.
3. Sampled, not 100% tested.

Figure 20. Reset, Power-Down and Power-up AC Waveform



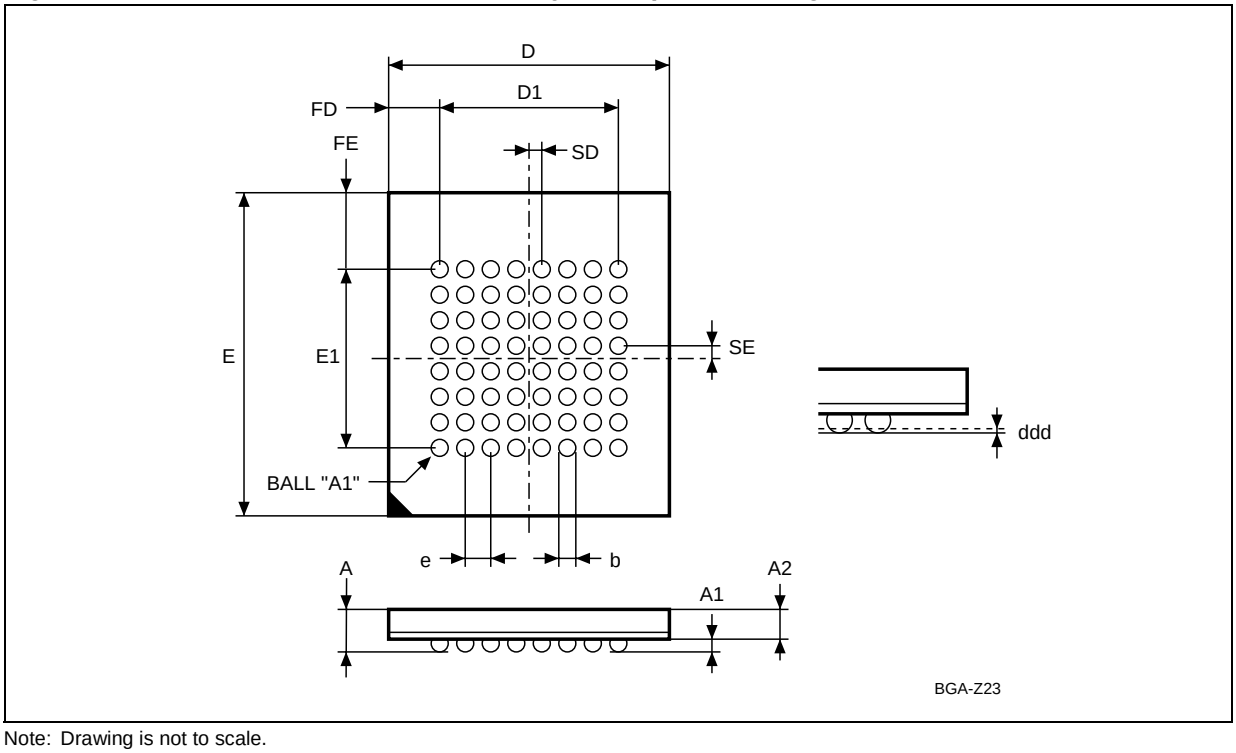
Note: 1. STS Configuration Code is 00h, the device is in Ready/Busy mode.

Table 20. Reset, Power-Down and Power-up AC Characteristics

Symbol	Parameter		M58LW128H	Unit
			115	
t_{PHQV}	Reset/Power-Down High to Data Valid	Max	190	ns
t_{PLPH}	Reset/Power-Down Low to Reset/Power-Down High	Min	100	ns
t_{VDHPH}	Supply Voltages High to Reset/Power-Down High	Min	60	µs
t_{PLSZ}	Reset/Power-Down Low to Status(Ready/Busy) High Impedance (end of the internal reset procedure Device reset during Program)	Max	20	µs
	Reset/Power-Down Low to Status(Ready/Busy) High Impedance (end of the internal reset procedure Device reset during Erase)	Max	20	µs

PACKAGE MECHANICAL

Figure 21. TBGA64 10x13mm - 8x8 ball array, 1mm pitch, Package Outline

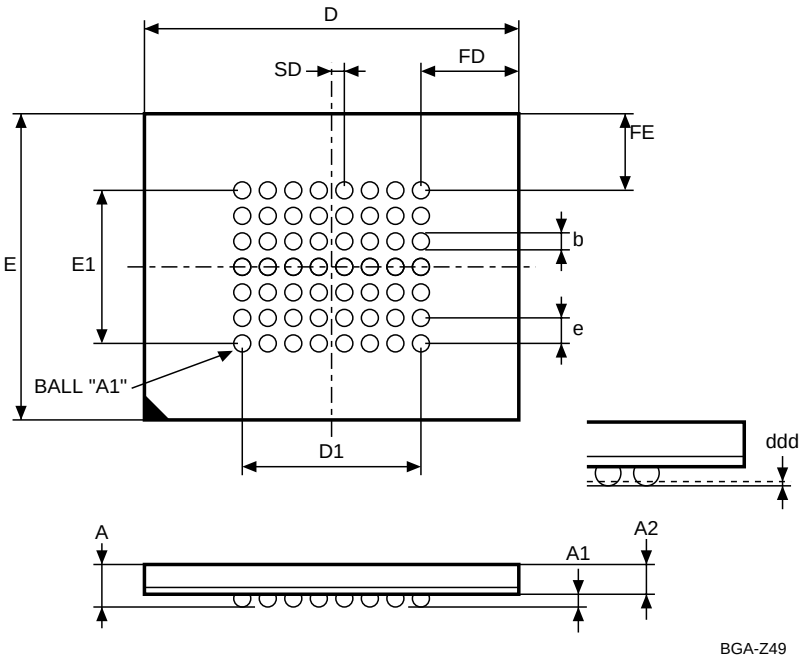


Note: Drawing is not to scale.

Table 21. TBGA64 10x13mm - 8x8 ball array, 1mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.300	0.200	0.350	0.0118	0.0079	0.0138
A2	0.800			0.0315		
b		0.350	0.500		0.0138	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	7.000			0.2756		
ddd			0.100			0.0039
e	1.000			0.0394		
E	13.000	12.900	13.100	0.5118	0.5079	0.5157
E1	7.000			0.2756		
FD	1.500			0.0591		
FE	3.000			0.1181		
SD	0.500			0.0197		
SE	0.500			0.0197		

Figure 22. VFBGA56 11x9mm - 8x7 ball array, 0.75mm pitch, Package Outline



Note: Drawing is not to scale.

Table 22. VFBGA56 11x9mm - 8x7 ball array, 0.75mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.000			0.0394
A1		0.150			0.0059	
A2	0.660			0.0260		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	11.000	10.900	11.100	0.4331	0.4291	0.4370
D1	5.250			0.2067		
ddd			0.100			0.0039
E	9.000	8.900	9.100	0.3543	0.3504	0.3583
E1	4.500			0.1772		
e	0.750	–	–	0.0295	–	–
FD	2.875			0.1132		
FE	2.250			0.0886		
SD	0.375			0.0148		

PART NUMBERING

Table 23. Ordering Information Scheme

Example: M58LW128H 115 ZA 6 T

Device Type
M58

Architecture
L = Page Mode, Burst

Operating Voltage
W = V_{DD} = 2.7V to 3.6V; V_{DDQ} = 1.8 to V_{DD}

Device Function
128H = 128 Mbit (x16), Uniform Block, Burst

Speed
115 = 115ns

Package
ZA = TBGA64 10 x 13mm, 1mm pitch
ZB = VFBGA56 11 x 9mm, 0.75mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-free Package, Standard Packing
F = Lead-free Package, Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

APPENDIX A. BLOCK ADDRESS TABLE

Table 24. Block Addresses

Block Number	Address Range (x16 Bus Width)
128	7F0000h-7FFFFFh
127	7E0000h-7EFFFFh
126	7D0000h-7DFFFFh
125	7C0000h-7CFFFFh
124	7B0000h-7BFFFFh
123	7A0000h-7AFFFFh
122	790000h-79FFFFh
121	780000h-78FFFFh
120	770000h-77FFFFh
119	760000h-76FFFFh
118	750000h-75FFFFh
117	740000h-74FFFFh
116	730000h-73FFFFh
115	720000h-72FFFFh
114	710000h-71FFFFh
113	700000h-70FFFFh
112	6F0000h-6FFFFFh
111	6E0000h-6EFFFFh
110	6D0000h-6DFFFFh
109	6C0000h-6CFFFFh
108	6B0000h-6BFFFFh
107	6A0000h-6AFFFFh
106	690000h-69FFFFh
105	680000h-68FFFFh
104	670000h-67FFFFh
103	660000h-66FFFFh
102	650000h-65FFFFh
101	640000h-64FFFFh
100	630000h-63FFFFh
99	620000h-62FFFFh
98	610000h-61FFFFh
97	600000h-60FFFFh
96	5F0000h-5FFFFFh
95	5E0000h-5EFFFFh
94	5D0000h-5DFFFFh
93	5C0000h-5CFFFFh
92	5B0000h-5BFFFFh
91	5A0000h-5AFFFFh
90	590000h-59FFFFh
89	580000h-58FFFFh
88	570000h-57FFFFh
87	560000h-56FFFFh
86	550000h-55FFFFh
85	540000h-54FFFFh
84	530000h-53FFFFh
83	520000h-52FFFFh
82	510000h-51FFFFh
81	500000h-50FFFFh
80	4F0000h-4FFFFFh
79	4E0000h-4EFFFFh
78	4D0000h-4DFFFFh
77	4C0000h-4CFFFFh
76	4B0000h-4BFFFFh
75	4A0000h-4AFFFFh
74	490000h-49FFFFh
73	480000h-48FFFFh
72	470000h-47FFFFh
71	460000h-46FFFFh
70	450000h-45FFFFh
69	440000h-44FFFFh
68	430000h-43FFFFh
67	420000h-42FFFFh
66	410000h-41FFFFh
65	400000h-40FFFFh
64	3F0000h-3FFFFFh

Block Number	Address Range (x16 Bus Width)
63	3E0000h-3EFFFFh
62	3D0000h-3DFFFFh
61	3C0000h-3CFFFFh
60	3B0000h-3BFFFFh
59	3A0000h-3AFFFFh
58	390000h-39FFFFh
57	380000h-38FFFFh
56	370000h-37FFFFh
55	360000h-36FFFFh
54	350000h-35FFFFh
53	340000h-34FFFFh
52	330000h-33FFFFh
51	320000h-32FFFFh
50	310000h-31FFFFh
49	300000h-30FFFFh
48	2F0000h-2FFFFFh
47	2E0000h-2EFFFFh
46	2D0000h-2DFFFFh
45	2C0000h-2CFFFFh
44	2B0000h-2BFFFFh
43	2A0000h-2AFFFFh
42	290000h-29FFFFh
41	280000h-28FFFFh
40	270000h-27FFFFh
39	260000h-26FFFFh
38	250000h-25FFFFh
37	240000h-24FFFFh
36	230000h-23FFFFh
35	220000h-22FFFFh
34	210000h-21FFFFh
33	200000h-20FFFFh
32	1F0000h-1FFFFFh
31	1E0000h-1EFFFFh
30	1D0000h-1DFFFFh
29	1C0000h-1CFFFFh

Block Number	Address Range (x16 Bus Width)
28	1B0000h-1BFFFFh
27	1A0000h-1AFFFFh
26	190000h-19FFFFh
25	180000h-18FFFFh
24	170000h-17FFFFh
23	160000h-16FFFFh
22	150000h-15FFFFh
21	140000h-14FFFFh
20	130000h-13FFFFh
19	120000h-12FFFFh
18	110000h-11FFFFh
17	100000h-10FFFFh
16	0F0000h-0FFFFFh
15	0E0000h-0EFFFFh
14	0D0000h-0DFFFFh
13	0C0000h-0CFFFFh
12	0B0000h-0BFFFFh
11	0A0000h-0AFFFFh
10	090000h-09FFFFh
9	080000h-08FFFFh
8	070000h-07FFFFh
7	060000h-06FFFFh
6	050000h-05FFFFh
5	040000h-04FFFFh
4	030000h-03FFFFh
3	020000h-02FFFFh
2	010000h-01FFFFh
1	000000h-00FFFFh

APPENDIX B. COMMON FLASH INTERFACE - CFI

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 25, 26, 27, 28, 29 and 30 show the addresses used to retrieve the data.

Table 25. Query Structure Overview

Offset	Sub-section Name	Description
00h		Manufacturer Code
01h		Device Code
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing and voltage information
27h	Device Geometry Definition	Flash memory layout
P(h)(1)	Primary Algorithm-specific Extended Query Table	Additional information specific to the Primary Algorithm (optional)
A(h)(2)	Alternate Algorithm-specific Extended Query Table	Additional information specific to the Alternate Algorithm (optional)
(SBA+02)h	Block Status Register	Block-related Information

Note: 1. Offset 15h defines P which points to the Primary Algorithm Extended Query Address Table.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.
3. SBA is the Start Base Address for each block.

Table 26. CFI - Query Address and Data Output

Address A23-A1	Data		Instruction
10h	51h	"Q"	Query ASCII String 51h; "Q" 52h; "R" 59h; "Y"
11h	52h	"R"	
12h	59h	"Y"	
13h	01h		Primary Vendor: Command Set and Control Interface ID Code
14h	00h		
15h	31h		Primary algorithm extended Query Address Table: P(h)
16h	00h		
17h	00h		Alternate Vendor: Command Set and Control Interface ID Code
18h	00h		
19h	00h		Alternate Algorithm Extended Query address Table
1Ah(2)	00h		

Note: 1. Query Data are always presented on DQ7-DQ0. DQ15-DQ8 are set to '0'.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.

Table 27. CFI - Device Voltage and Timing Specification

Address A23-A1	Data	Description
1Bh	27h (1)	V_{DD} Min, 2.7V
1Ch	36h (1)	V_{DD} max, 3.6V
1Dh	00h (2)	V_{PP} min – Not Available
1Eh	00h (2)	V_{PP} max – Not Available
1Fh	04h	2^n µs typical time-out for Word, DWord prog – Not Available
20h	09h	2^n µs, typical time-out for max buffer write
21h	0Ah	2^n ms, typical time-out for Erase Block
22h	00h (3)	2^n ms, typical time-out for chip erase – Not Available
23h	02h	2^n x typical for Word Dword time-out max – Not Available
24h	02h	2^n x typical for buffer write time-out max
25h	02h	2^n x typical for individual block erase time-out maximum
26h	00h (3)	2^n x typical for chip erase max time-out – Not Available

Note: 1. Bits are coded in Binary Code Decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in 100mV.
2. Bit7 to bit4 are coded in Hexadecimal and scaled in Volts while bit3 to bit0 are in Binary Code Decimal and scaled in 100mV.
3. Not supported.

Table 28. Device Geometry Definition

Address A23-A1	Data	Description
27h	18h	n where 2^n is number of bytes memory Size
28h	01h	Device Interface
29h	00h	Organization Sync./Async.
2Ah	06h	Maximum number of bytes in Write Buffer, 2^n
2Bh	00h	
2Ch	01h	Bit7-0 = number of Erase Block Regions in device
2Dh	7Fh	Number (n-1) of Erase Blocks of identical size; n=64
2Eh	00h	
2Fh	00h	Erase Block Region Information x 256 bytes per Erase block (128K bytes)
30h	02h	

Table 29. Block Status Register

Address A23-A1	Data		Selected Block Information
(BA+2)h[1]	bit0	0	Block Unprotected
		1	Block Protected
	bit1	0	Block Locked Down
		1	Block Locked Down
	bit7-2	0	Reserved for future features

Note: 1. BA specifies the first block address location, A23-A1.

Table 30. Extended Query information

Address offset	Address A23-A1	Data (Hex) x16 Bus Width		Description
(P)h	31h	50h	"P"	Query ASCII string - Extended Table
(P+1)h	32h	52h	"R"	
(P+2)h	33h	49h	"I"	
(P+3)h	34h	31h		Major version number
(P+4)h	35h	31h		Minor version number
(P+5)h	36h	E6h		Optional Feature: (1=yes, 0=no) bit0, Chip Erase Supported (0=no) bit1, Suspend Erase Supported (1=yes) bit2, Suspend Program Supported (1=yes) bit3, Legacy Block Protect/Unprotect Supported (0=no) bit4, Queue Erase Supported (0=no) bit5, Instant Individual Block protection (1=yes) bit6, Protection bits supported (1=yes) bit7, Page Read supported (1=yes) bit8, Synchronous Read supported (1=yes) bits 9 to 31 reserved for future use
(P+6)h	37h	01h		
(P+7)h	38h	00h		
(P+8)h	39h	00h		
(P+9)h	3Ah	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bit 7-1 reserved for future use
(P+A)h	3Bh	07h		Block Status Register bit0, Block Protection Bit status active (1=yes) bit1, Block Lock-Down Bit status active bit 2, Un-Lock-down bit bits 3 to 15 reserved for future use
(P+B)h	3Ch	00h		
(P+C)h	3Dh	33h		V_{DD} OPTIMUM Program/Erase voltage conditions (1)
(P+D)h	3Eh	00h		V_{PP} OPTIMUM Program/Erase voltage conditions (1)
(P+E)h	3Fh	02h		OTP protection: No. of protection register fields (2)
(P+F)h	40h	80h		Protection Sub-Register0's start address, least significant bits (80h)
(P+10)h	41h	00h		Protection Sub-Register0's start address, most significant bits (00h)
(P+11)h	42h	03h		n where 2^n is number of factory preprogrammed bytes
(P+12)h	43h	03h		n where 2^n is number of user programmable bytes
(P+13)h	44h	89h		Protection Registers1-16's start address, least significant bits (89h) Protection Registers1-16's start address, most significant bits (00h) Least significant bits (00h) in start address of number n of factory programmed Protection Sub-Registers (n = 0) Most significant bits (00h) in start address of number n of factory programmed Protection Sub-Registers (n = 0) n where 2^n is the number of factory preprogrammed bytes per Protection Sub-Register Least significant bits (10h) in start address of number n of factory programmed Protection Sub-Registers (n = 16) Most significant bits (00h) in start address of number of factory programmed Protection Sub-Registers n where 2^n is the number of user programmable bytes per Protection Sub-Register
(P+14)h	45h	00h		
(P+15)h	46h	00h		
(P+16)h	47h	00h		
(P+17)h	48h	00h		
(P+18)h	49h	00h		
(P+19)h	4Ah	00h		
(P+1A)h	4Bh	10h		
(P+1B)h	4Ch	00h		
(P+1C)h	4Dh	04h		

Note: 1. Query Data are always presented on DQ7-DQ0. DQ15-DQ8 are set to '0'.
2. Bits are coded in Binary Code Decimal, bit7 to bit4 and scaled in Volts while bit3 to bit0 are scaled in 100mV.

Table 31. Burst Read Information

Offset	Data	Description	Value
(P+1D)h = 4Eh	04h	Page-mode read capability bits 0-7 'n' such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width.	16 Bytes
(P+1E)h = 4Fh	02h	Number of synchronous mode read configuration fields that follow.	2
(P+1F)h = 50h	02h	Synchronous mode read capability configuration 1 bit 3-7 Reserved bit 0-2 'n' such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the read configuration register bits 0-2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	8
(P+20)h = 51h	03h	Synchronous mode read capability configuration 2	16

APPENDIX C. FLOWCHARTS

Figure 23. Write to Buffer and Program Flowchart and Pseudo Code

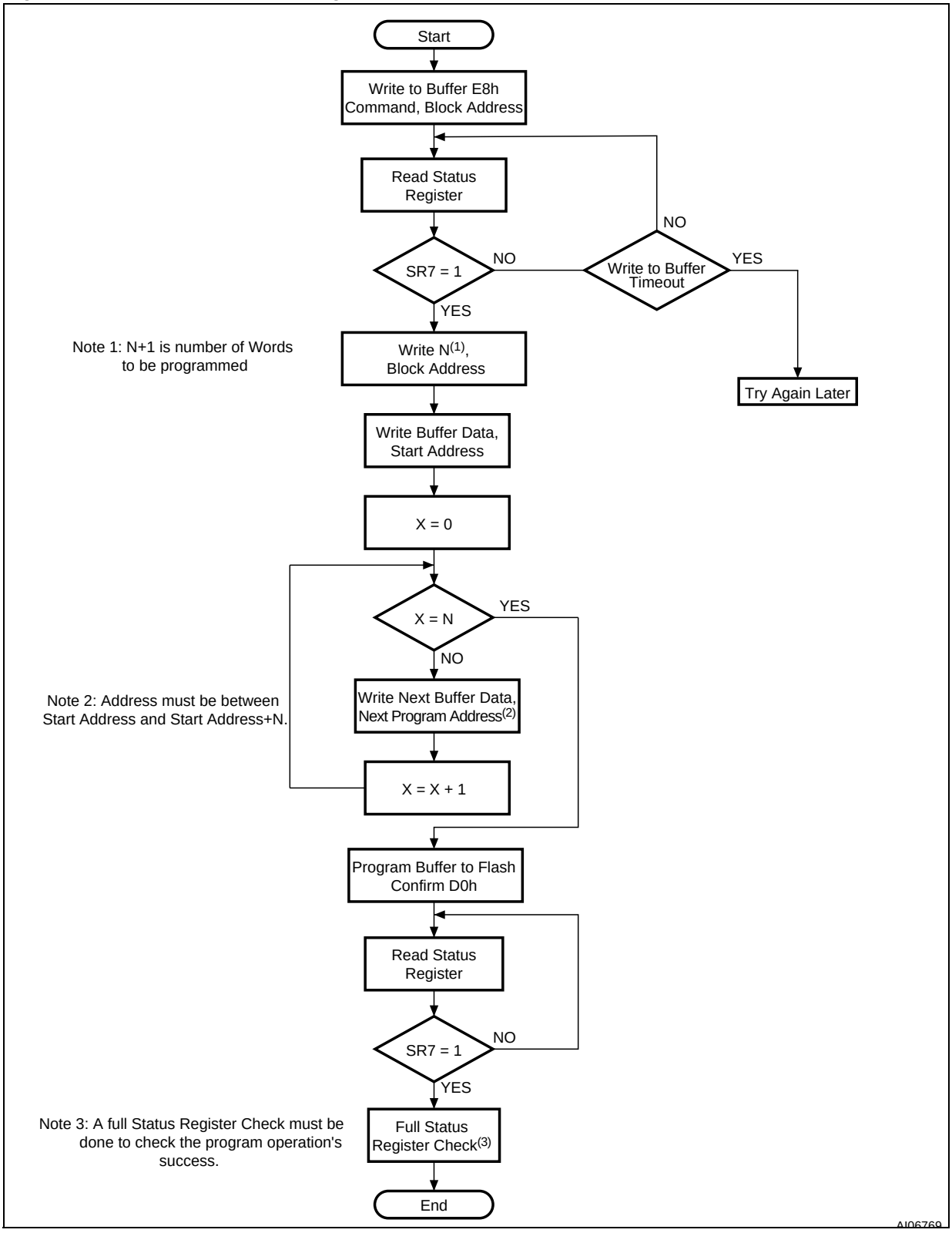


Figure 24. Buffer Enhanced Factory Program Flowchart and Pseudo Code

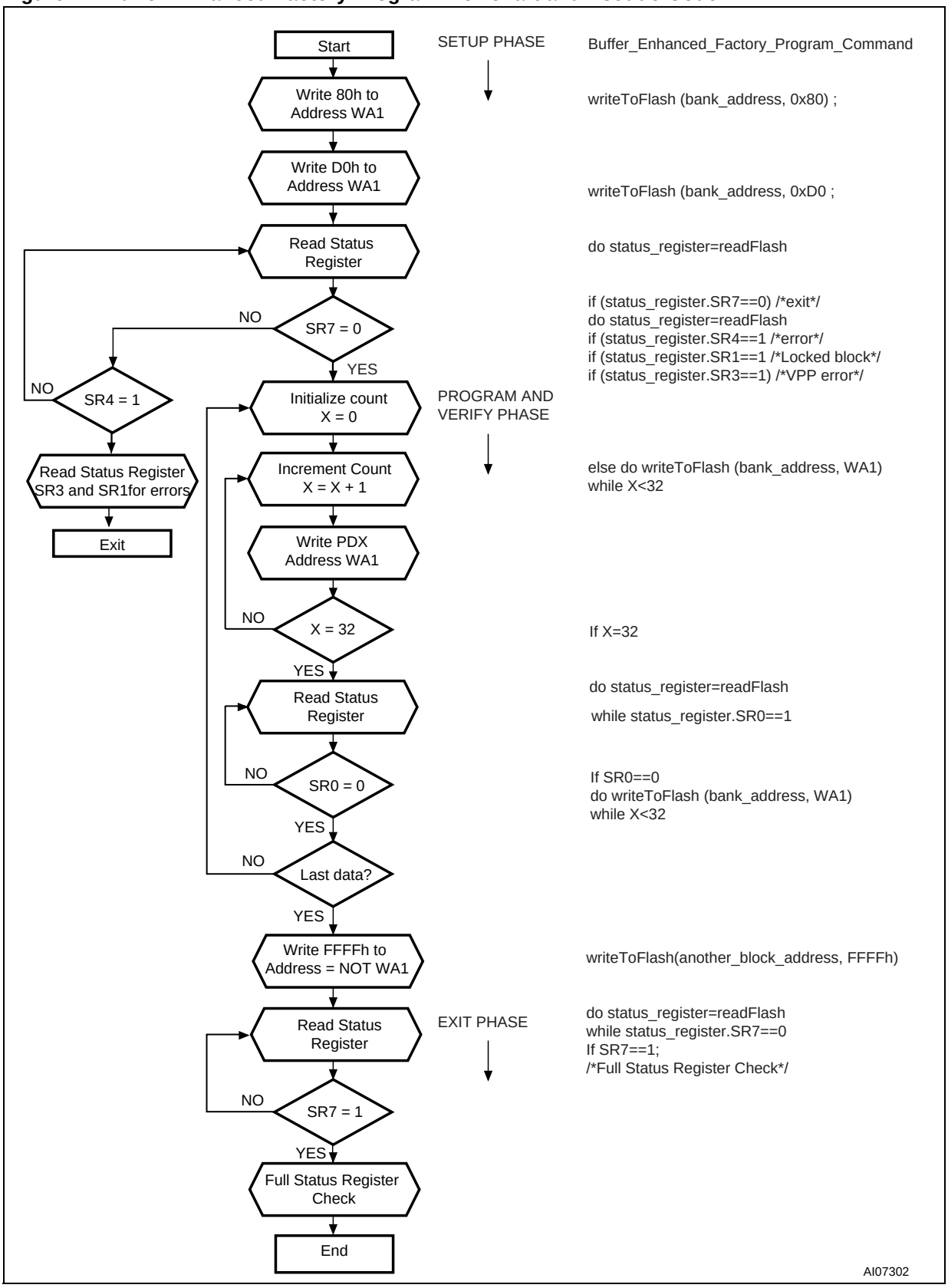
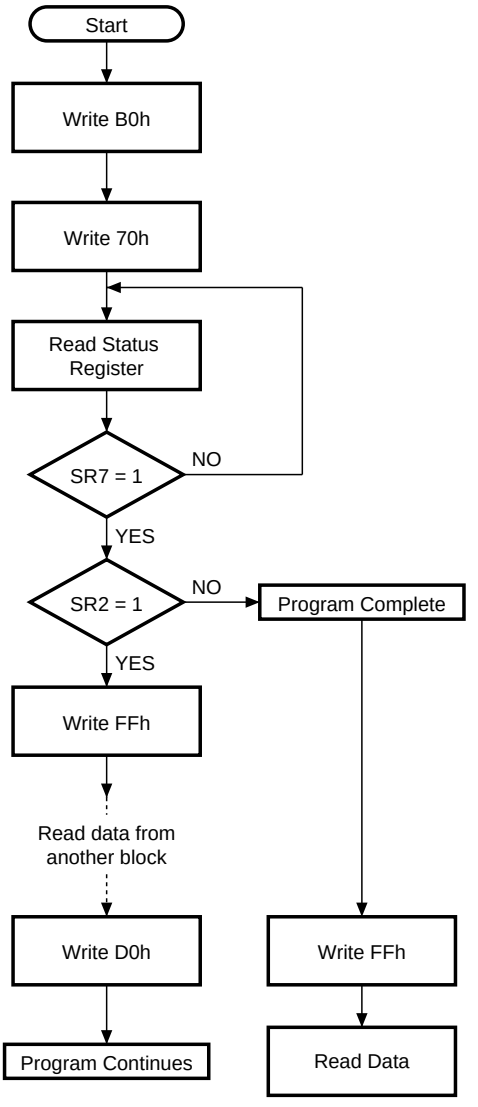


Figure 25. Program Suspend & Resume Flowchart and Pseudo Code



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while SR7 = 1

If SR2 = 0, Program completed

Read Memory Array command:
– write FFh
– one or more data reads from other blocks

Program Erase Resume Command:
– write D0h to resume erasure
– if the program operation completed then this is not necessary. The device returns to Read Array as normal (as if the Program/Erase Suspend command was not issued).

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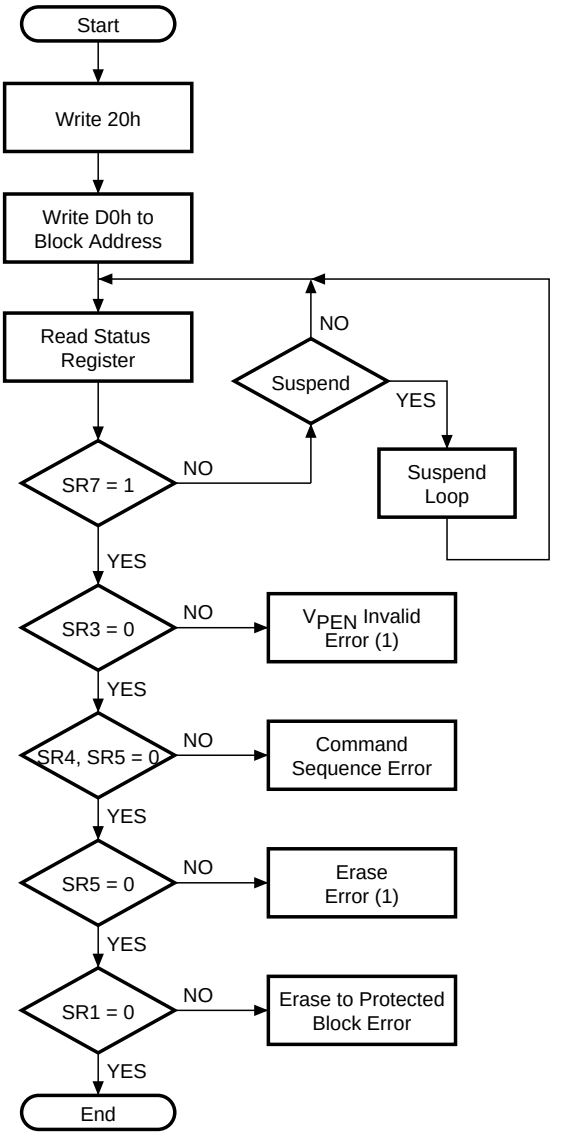
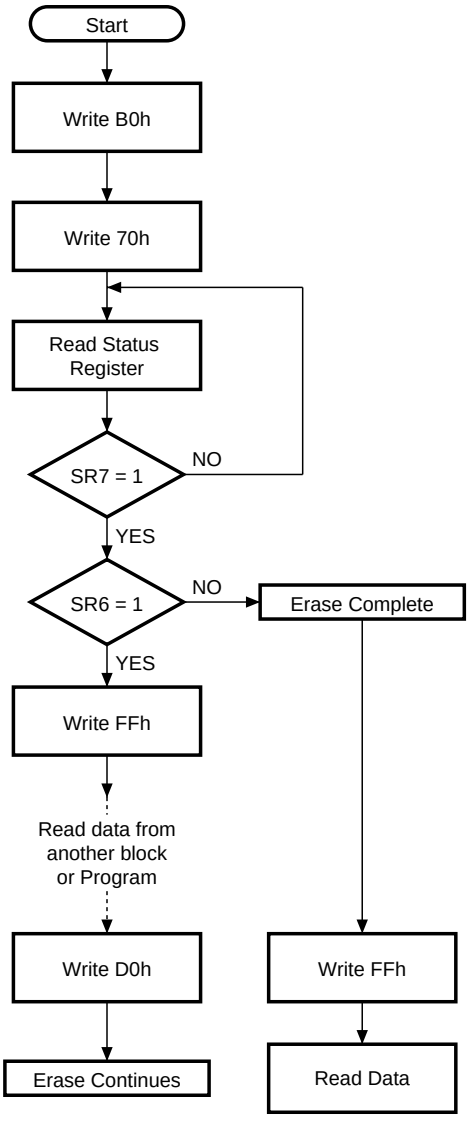
Figure 26. Erase Flowchart and Pseudo Code



Note: 1. If an error is found, the Status Register must be cleared (Clear Status Register Command) before further program or erase operations.

Figure 27. Erase Suspend & Resume Flowchart and Pseudo Code



Program/Erase Suspend Command:
– write B0h
– write 70h

do:
– read status register

while SR7 = 1

If SR6 = 0, Erase completed

Read Memory Array command:
– write FFh
– one or more data reads from other blocks

Program/Erase Resume command:
– write D0h to resume the Erase operation
– if the Program operation completed then this is not necessary. The device returns to Read mode as normal (as if the Program/Erase suspend was not issued).

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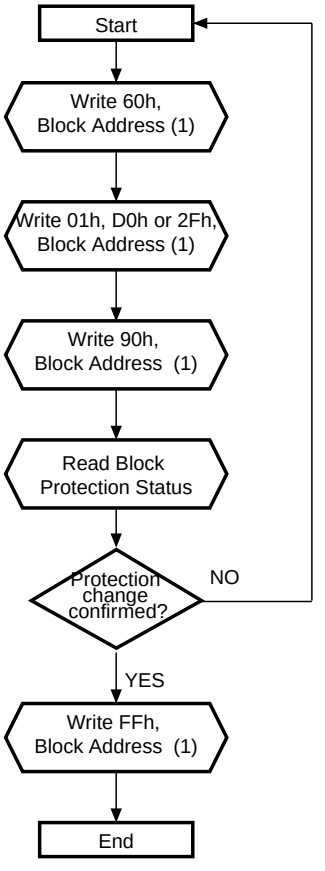
Figure 28. Protection Operations Flowchart and Pseudo Code




```
protection_operation_command   (address, protection_operation)  {
      writeToFlash (address, 0x60) ; /*configuration setup*/
                                    /* see note (1) */

      if  (protection_operation==PROTECT)  /*to protect the block*/
            writeToFlash (address, 0x01)  ;
      else if  (protection_operation==UNPROTECT)  /*to unprotect the block*/
            writeToFlash (address, 0xD0)  ;
      else if  (protection_operation==LOCK-DOWN)  /*to lock the block*/
            writeToFlash (address, 0x2F)  ;

            writeToFlash (address, 0x90) ;
                                 /*see note (1) */

      if  (readFlash (address) ! = protection_status_expected)
                  error_handler () ;
            /*Check the protection status (see Read Electronic Signature table )

      writeToFlash (address, 0xFF) ; /*Reset to Read Array mode*/
                        /*see note (1) */

}
```

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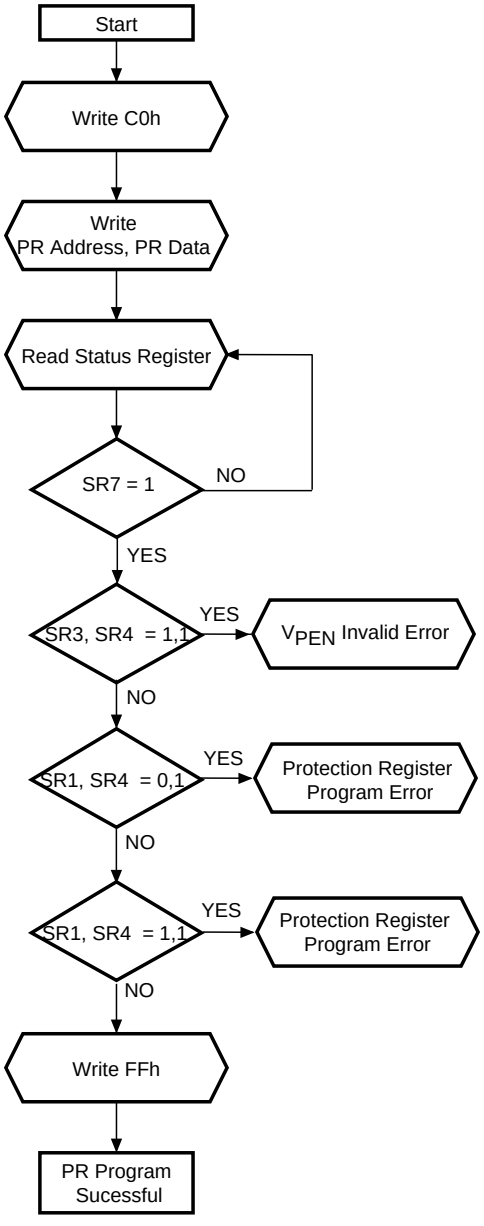
Note: 1. Any address within the block can equally be used.

Figure 29. Protection Register Program Flowchart and Pseudo Code



Protection Register Program Command
– write C0h
– write Protection Register Address,
Protection Register Data

do:
– read status register

while SR7 = 1

If SR3 = 1, SR4 = 1 V_{PEN} Invalid Error

If SR1 = 0, SR4 = 1 Protection Register
Program Error

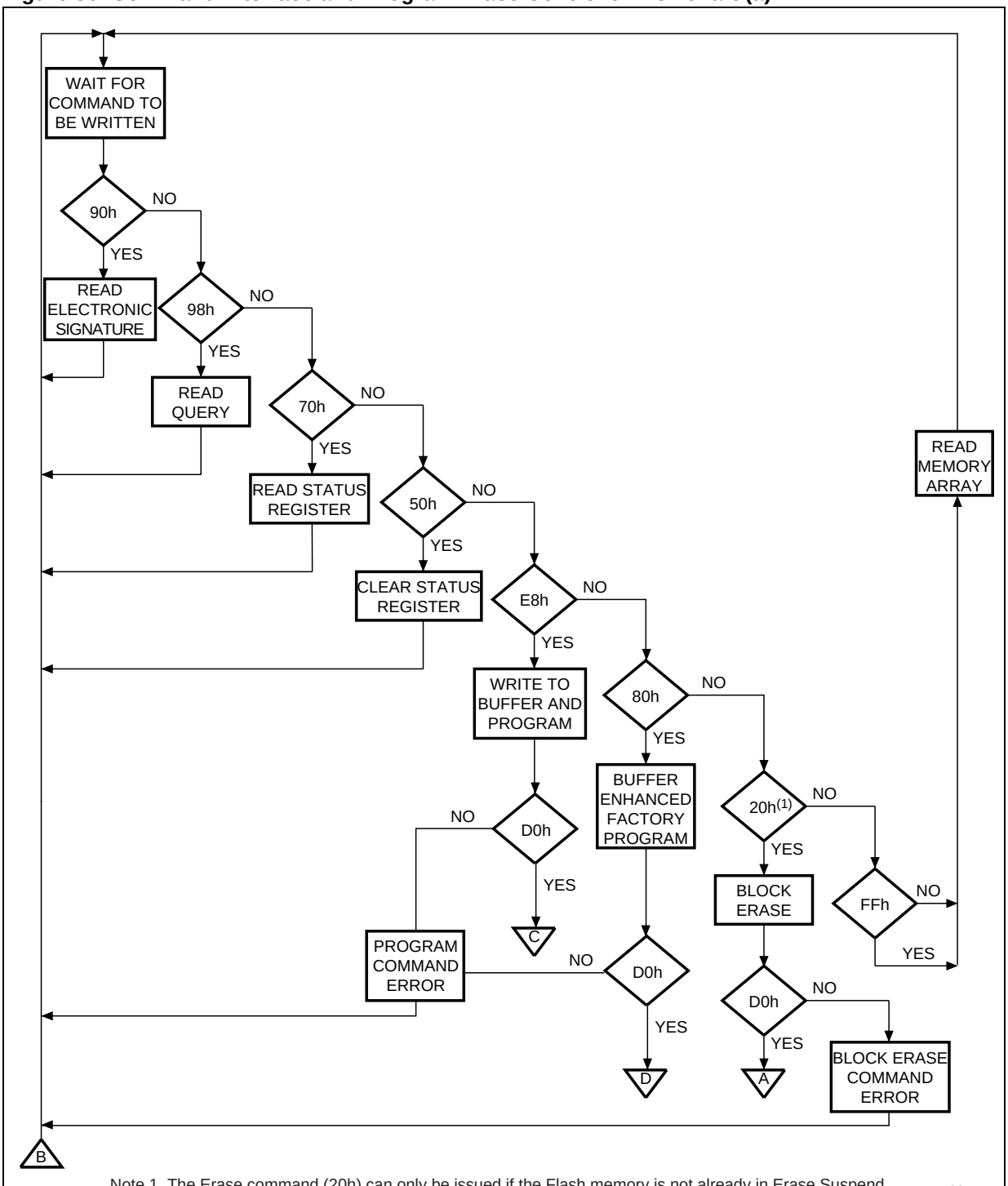
If SR1 = 1, SR4 = 1 Program Error due to
Protection Register Protection

Read Memory Array Command:
– write FFh

AI06159b

Note: PR = Protection Register

Figure 30. Command Interface and Program Erase Controller Flowchart (a)



Note 1. The Erase command (20h) can only be issued if the Flash memory is not already in Erase Suspend.

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Figure 31. Command Interface and Program Erase Controller Flowchart (b)

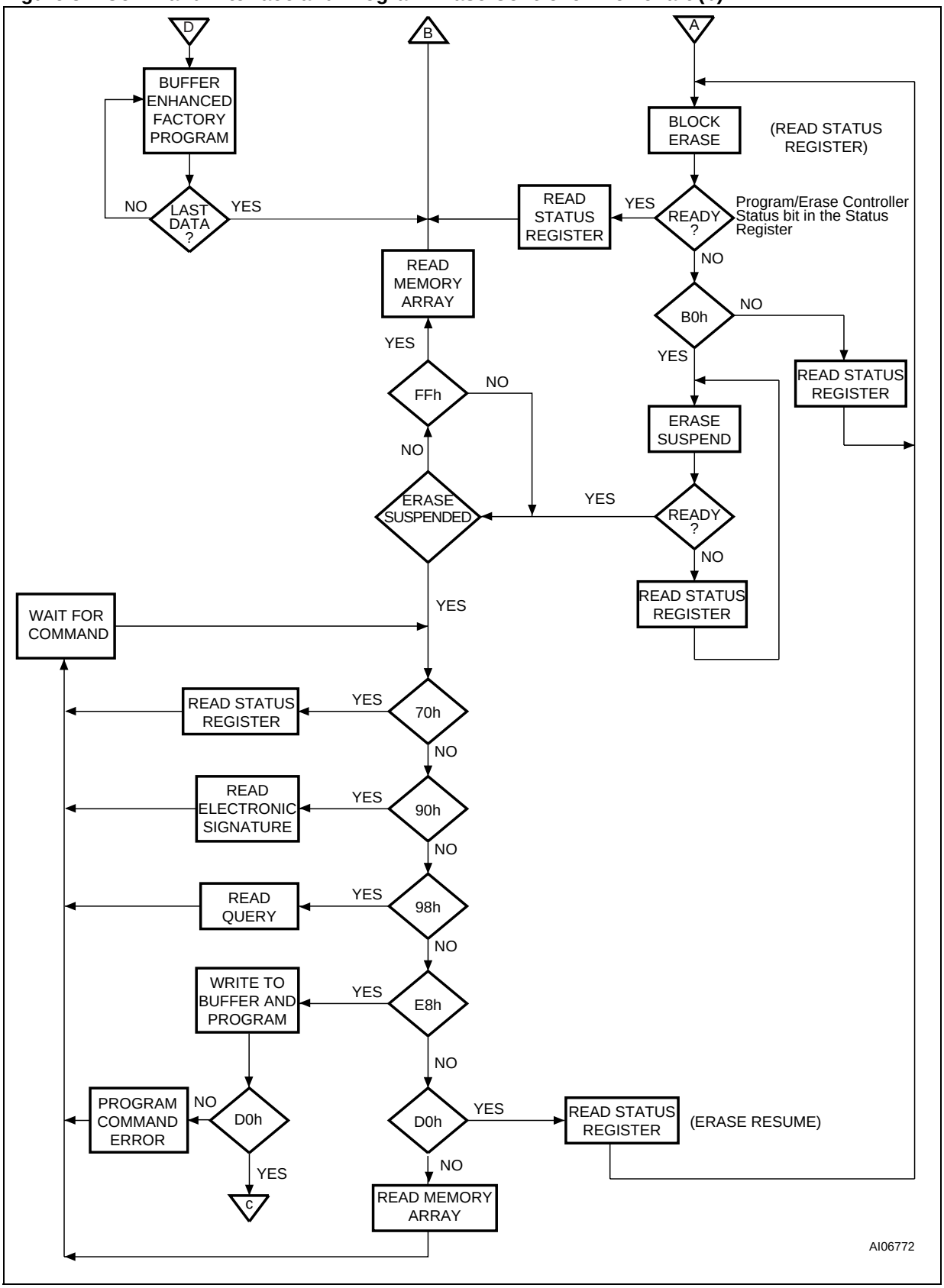
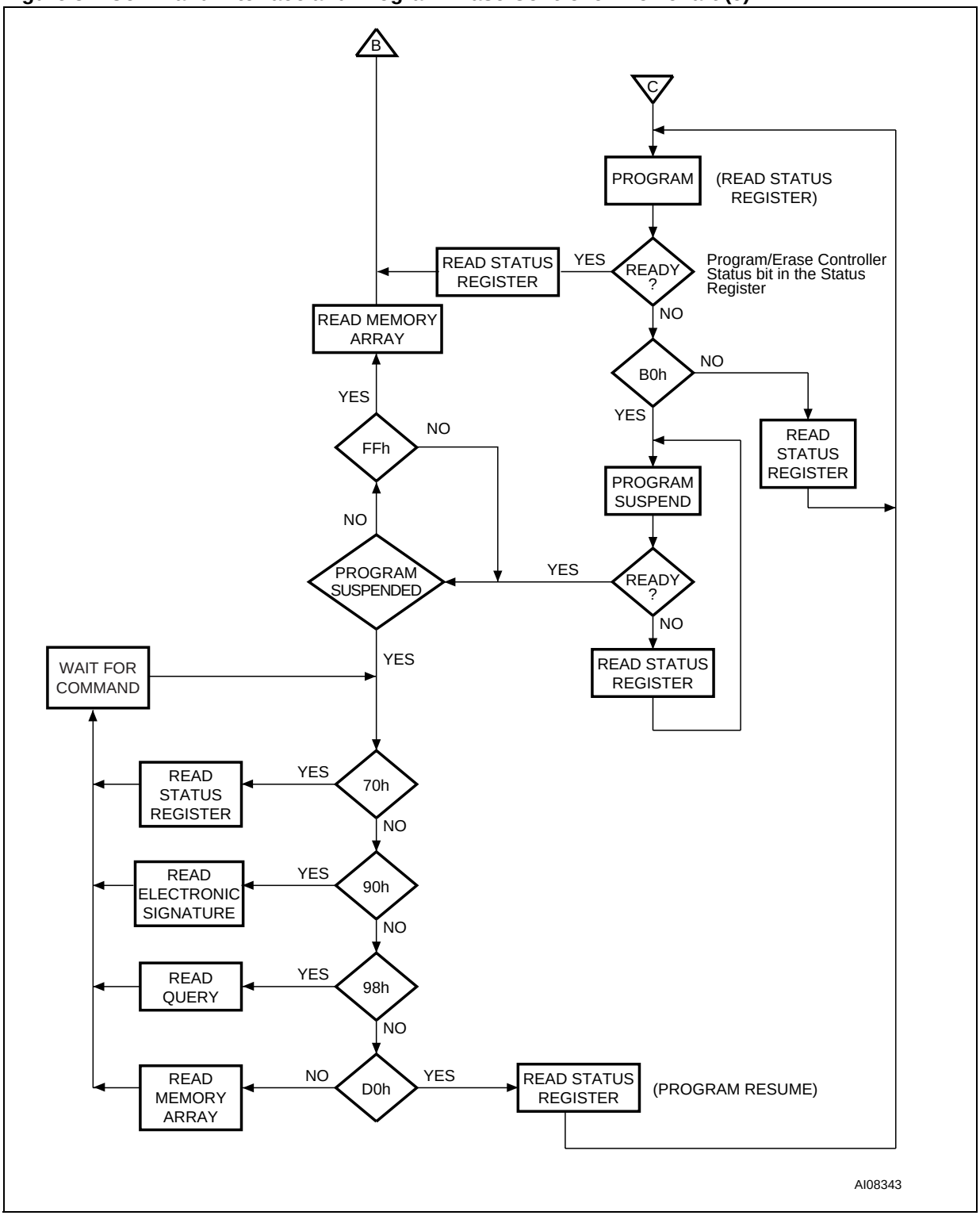


Figure 32. Command Interface and Program Erase Controller Flowchart (c)



REVISION HISTORY

Table 32. Document Revision History

Date	Version	Revision Details
18-Aug-2003	1.0	31-Jul-03: First Draft. 7-Aug-03:Second Draft t_{PLRH} changed to t_{PLRST} Figure 20 and Table 20, Reset, Power-Down and Power-up AC Waveforms and Characteristics modified 8-Aug-03: Third draft tPLRST timing name and definition modified