High density UV erasable programmable logic device

PLV750/L

DESCRIPTION

The PLV750/L is 100% more powerful than most other programmable logic devices in 24-pin packages. Increased product terms, sum terms, and flip-flops translate into more usable gates.

Each of the PLV750/L's 22 logic pins can be used as an input. Ten of these can be used as input, output, or bi-directional I/O pins. All 20 flip-flops can be fed back into the array independently. This flexibility allows burying all of the sum terms and flip-flops.

There are 171 product terms available. A variable format is used to assign between 4 and 8 product terms per sum term. There are 2 sum terms per output, providing added flexibility. Much more logic can be replaced by this one 24-pin device.

The PLV750/L has more flip-flops available than other EPLDs in this density range. Complex state machines are easily implemented.

Product terms are available providing Asynchronous Resets, flip-flop clocks, and Output Enables. One reset and one clock term are provided per flip-flop, with one Enable term per output. One product term provides a global synchronous Preset. Register Preload simplifies testing. The device has an internal power up clear function.

APPLICATIONS

- Multiple, independent state machines or storage banks, counters and shifters
- Bus protocol generation
- Timing generators
- Arbitration functions
- Peripheral control functions

FEATURES

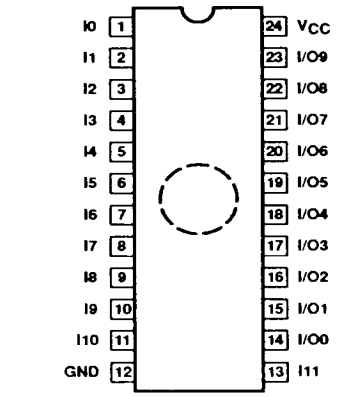
- Third generation programmable logic structure
  - High density replacement for discrete logic
- Pin-for-pin and functionally compatible with Atmel's ATV750/L
- High speed – plus a low power version
- Increased logic flexibility
  - 42 inputs and 20 sum terms
- Flexible output logic
  - 20 flip-flops – 10 extra
  - All can be individually buried or 10 output directly
  - Each has individual Asynchronous Reset or clock terms
- Multiple feedback paths provide for buried state machines and I/O bus compatibility
- Proven and reliable high speed CMOS EPROM process
  - 2000V ESD protection
  - 200mA latchup immunity
- Reprogrammable – tested 100% for programmability
- 24-pin, 300mil-wide Dual In-Line and 28-lead surface mount packages

PIN DESCRIPTIONS

PIN NAME	FUNCTION
I	Logic inputs
I/O	Bi-directional buffers
NC	No internal connection
V_{CC}	+5V Supply
GND	Ground

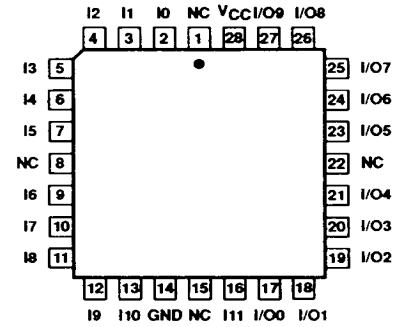
PIN CONFIGURATIONS

FA and N Packages



FA = Ceramic Dual In-Line Package with Quartz Window (300mil-wide)
N = Plastic Dual In-Line package (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line Package with Quartz Window 300mil-wide (t_{PD} = 20ns)	PLV750-20FA
24-Pin Plastic Dual In-Line Package 300mil-wide (t_{PD} = 20ns)	PLV750-20N
28-Pin Plastic Leaded Chip Carrier (t_{PD} = 20ns)	PLV750-20A
24-Pin Ceramic Dual In-Line Package with Quartz Window 300mil-wide (t_{PD} = 25ns)	PLV750-25FA, PLV750L-25FA
24-Pin Plastic Dual In-Line Package 300mil-wide (t_{PD} = 25ns)	PLV750-25N, PLV750L-25N
28-Pin Plastic Leaded Chip Carrier (t_{PD} = 25ns)	PLV750-25A, PLV750L-25A
24-Pin Ceramic Dual In-Line Package with Quartz Window 300mil-wide (t_{PD} = 30ns)	PLV750L-30FA
24-Pin Plastic Dual In-Line Package 300mil-wide (t_{PD} = 30ns)	PLV750L-30N
28-Pin Plastic Leaded Chip Carrier (t_{PD} = 30ns)	PLV750L-30A

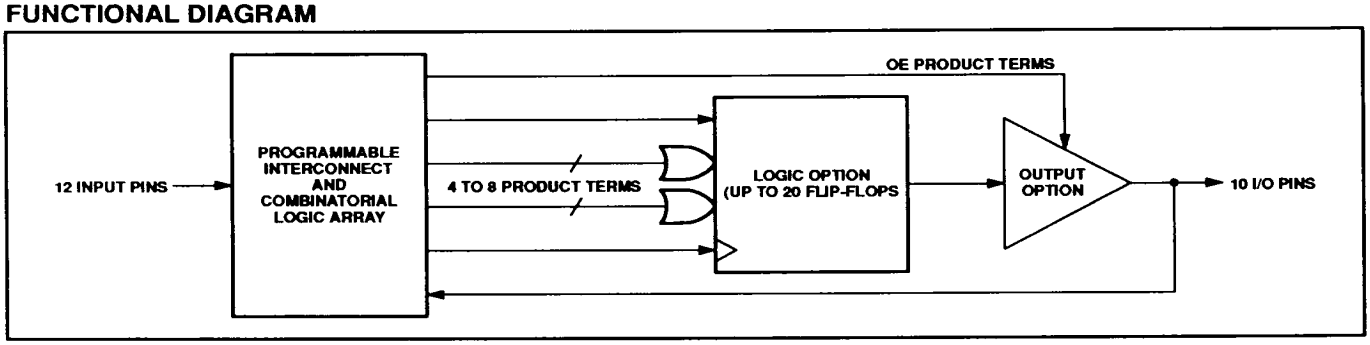
November 1991

Powered by ICminer.com Electronic-Library Service CopyRight 2003

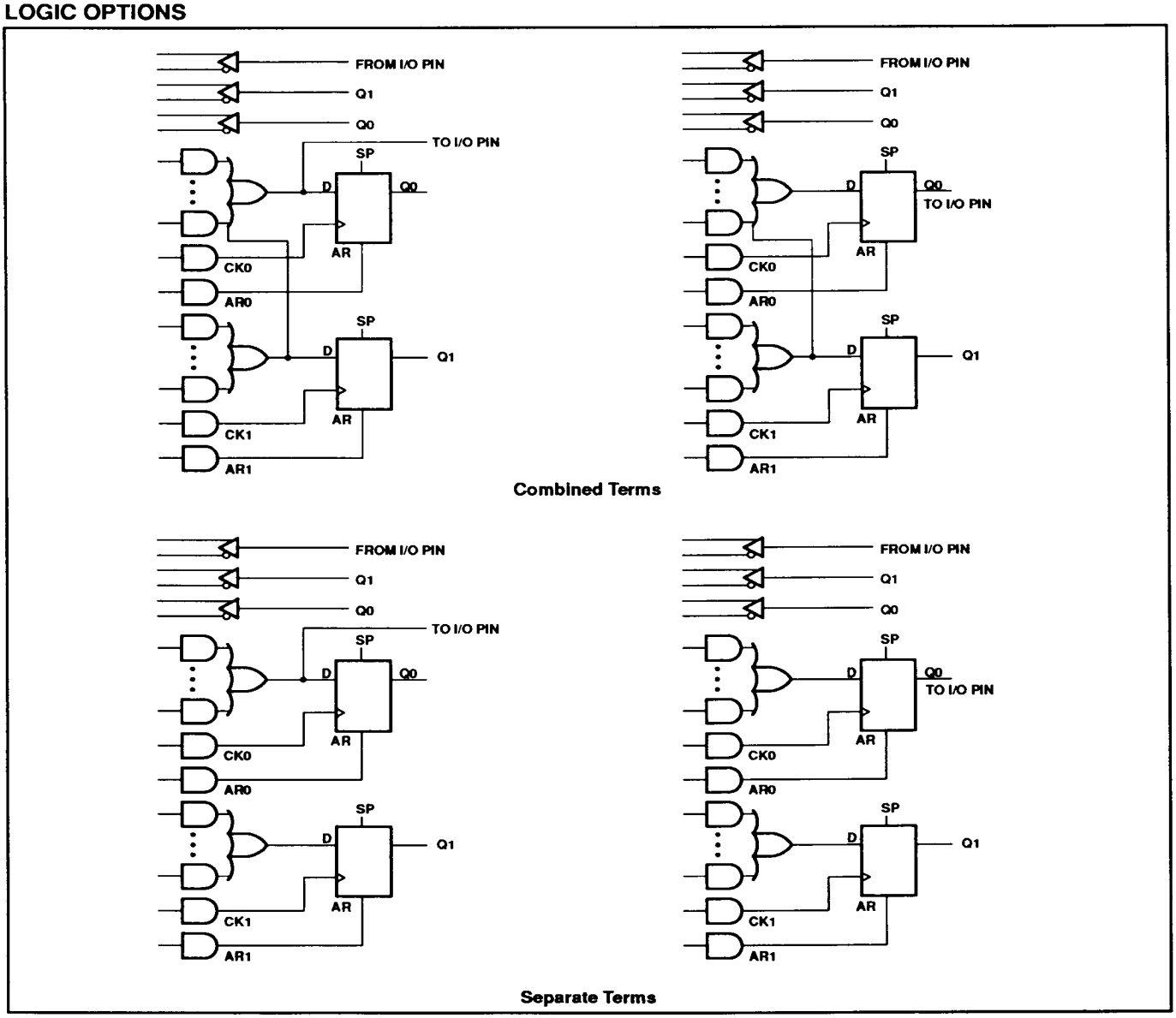
High density UV erasable programmable logic device

PLV750/L

FUNCTIONAL DIAGRAM

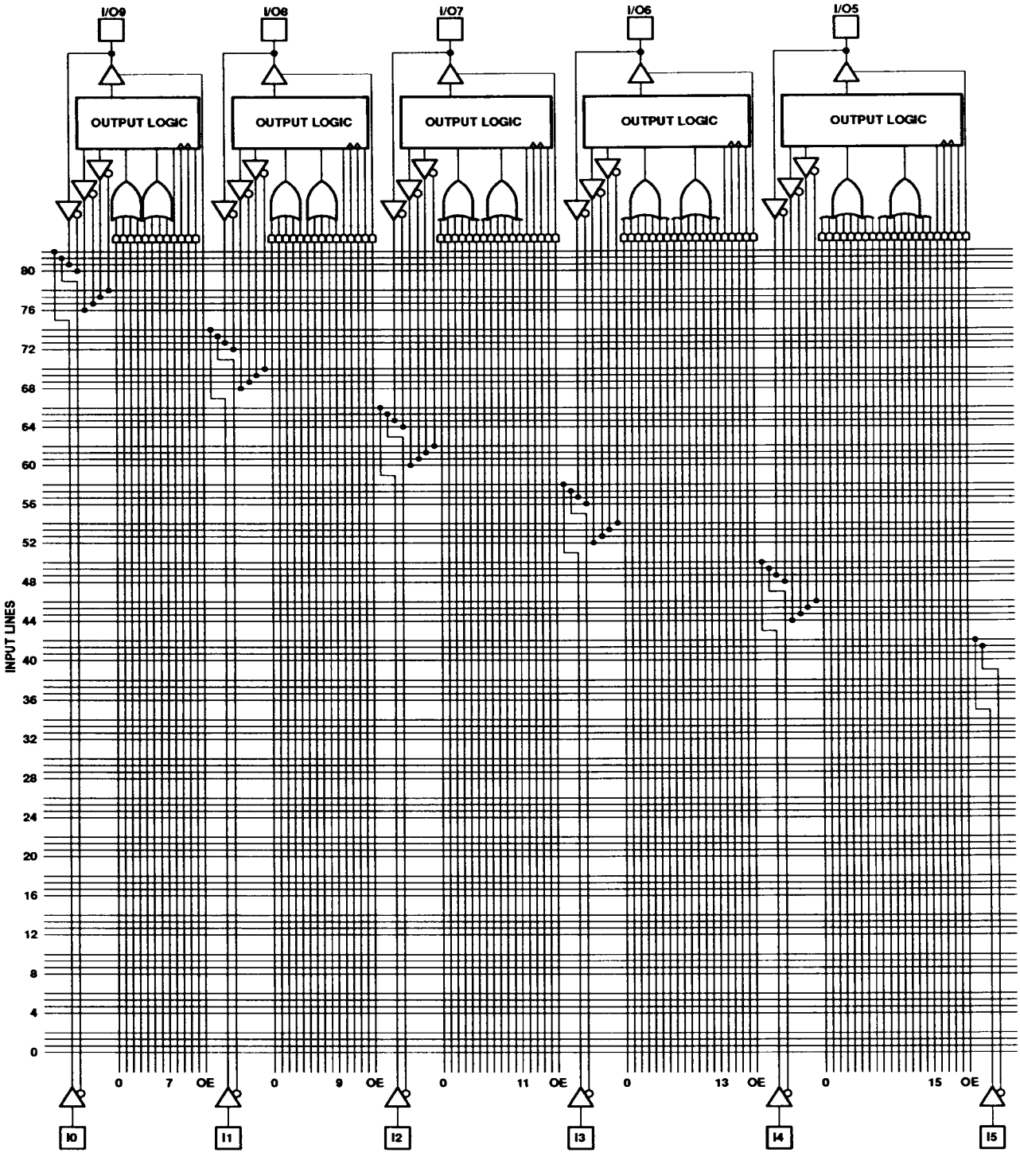


LOGIC OPTIONS



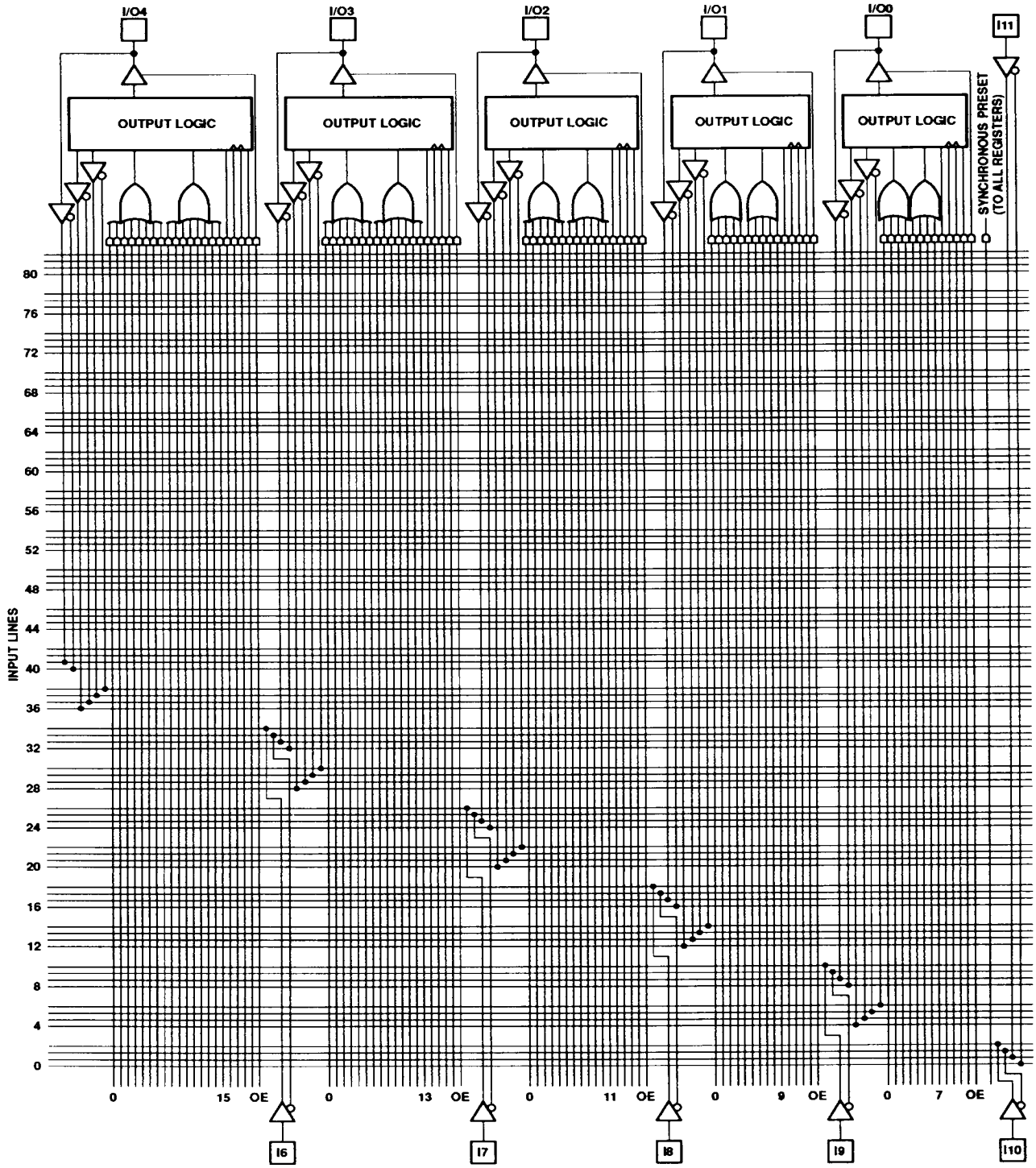
Powered by ICminer.com Electronic-Library Service CopyRight 2003

LOGIC DIAGRAM



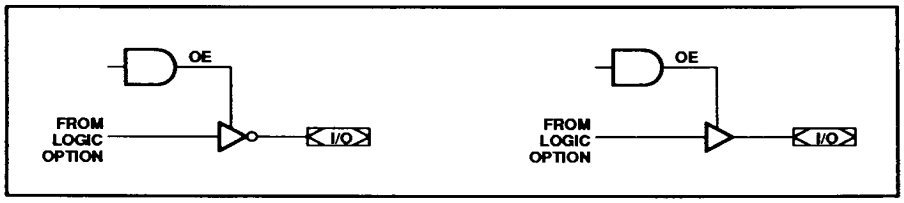
Powered by ICminer.com Electronic-Library Service CopyRight 2003

LOGIC DIAGRAM (Continued)



Powered by ICminer.com Electronic-Library Service CopyRight 2003

OUTPUT OPTIONS



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{IN}	Voltage on any pin with respect to ground[2]	–2.0 to +7.0	V_{DC}
V_{IP}	Voltage on input pins with respect to ground during programming[2]	–2.0 to +14.0	V_{DC}
V_{PP}	Programming voltage with respect to ground[2]	–2.0 to +14.0	V
—	Integrated UV erase dose	7258	Wsec/cm^2
T_{bias}	Temperature under bias	–55 to +125	°C
T_{stg}	Storage temperature	–65 to +150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum voltage is $-0.6V_{DC}$ which may undershoot to –2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC} + 0.75V_{DC}$ which may overshoot to +7.0V for pulses of less than 20ns.

OPERATING MODES

MODE	24 DIP Pin	1	5	8	11	13	I/Os	V_{CC}(24)
	28 PLCC Pin	2	6	10	13	16	I/OS	V_{CC}(28)
"EPLD"		X[1]	X	X	X	X	I/O	5V
Program		V_{PP}	X/V_H[2]	X	X/V_H	V_{PP}	D_{IN}	6V
PGM Verify		V_{PP}	X/V_H	X	X/V_H	V_{IL}	D_{OUT}	5V
PGM Inhibit		V_{PP}	X/V_H	X	X/V_H	V_{IH}	Hi-Z	5–6V
Preload #1		X	X	V_H	X	V_{IL}	D_{IN}	5V
Preload #2		X	X	V_H	X	V_{IH}	D_{IN}	5V

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq 70°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I_{IL}	Input load current	$V_{IN} = -0.1V$ to $V_{CC} + 1V$		10	µA
I_{LO}	Output leakage current	$V_{OUT} = -0.1V$ to $V_{CC} + 0.1V$		10	µA
I_{CC}	Power supply current, PLV750	V_{CC} = MAX, V_{IN} = GND, Outputs Open		120	mA
	Power supply current, PLV750L	V_{CC} = MAX, V_{IN} = GND, Outputs Open		12	mA
I_{CC2}	Clocked power supply current[2], PLV750L	f = 1MHz, V_{CC} = MAX, Outputs Open		15	mA
I_{OS}	Output short circuit current[1]	$V_{OUT} = 0.5V$		–90	mA
V_{IL}	Input Low voltage		–0.6	0.8	V
V_{IH}	Input High voltage		2.0	V_{CC}+0.75	V
V_{OL}	Output Low voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN I_{OL} = 12mA		0.5	V
V_{OL}	Output Low voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN I_{OL} = 24mA		1.0	V
V_{OH}	Output High voltage	$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN $I_{OH} = -100µA$	V_{CC}–0.3		V
		$V_{IN} = V_{IH}$ or V_{IL}, V_{CC} = MIN $I_{OH} = -4.0mA$	2.4		V
C_{IN}	Input capacitance[3]	$V_{IN} = 0V$ f = 1MHz, T_{amb} = 25°C	5	8	pF
C_{OUT}	Output capacitance[3]	$V_{OUT} = 0V$ f = 1MHz, T_{amb} = 25°C	6	8	pF

NOTES:
1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Outputs not loaded.
3. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

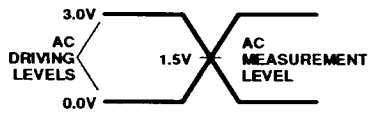
Powered by ICminer.com Electronic-Library Service CopyRight 2003

AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq 70°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	LIMITS						UNIT
		PLV750-20		PLV750/L-25		PLV750L-30		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD}	Input or feedback to non-registered output		20		25		30	ns
t_{EA}	Input to Output Enable		20		25		30	ns
t_{ER}	Input to Output Disable		20		25		30	ns
t_{CO}	Clock to output		20		22	5	25	ns
t_{CF}	Clock to feedback	5	10	5	10	5	10	ns
t_S	Input setup time	10		12		15		ns
t_{SF}	Feedback setup time	5		7		15		ns
t_H	Hold time	5		5		5		ns
t_P	Clock period	18		22		25		ns
t_W	Clock width	8		10		12		ns
f_{MAX}	Maximum frequency		55		45		40	MHz
t_{AW}	Asynchronous Reset width	15		20		30		ns
t_{AR}	Asynchronous Reset recovery time	15		20		30		ns
t_{AP}	Asynchronous Reset to registered output reset		20		25		30	ns
t_{SP}	Setup time, Synchronous Preset	12		15		15		ns

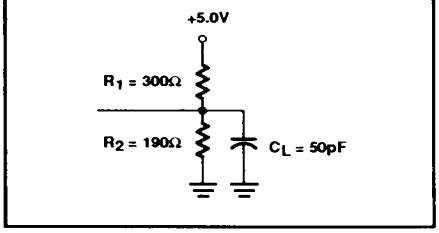
INPUT TEST WAVEFORMS AND MEASUREMENT LEVELS



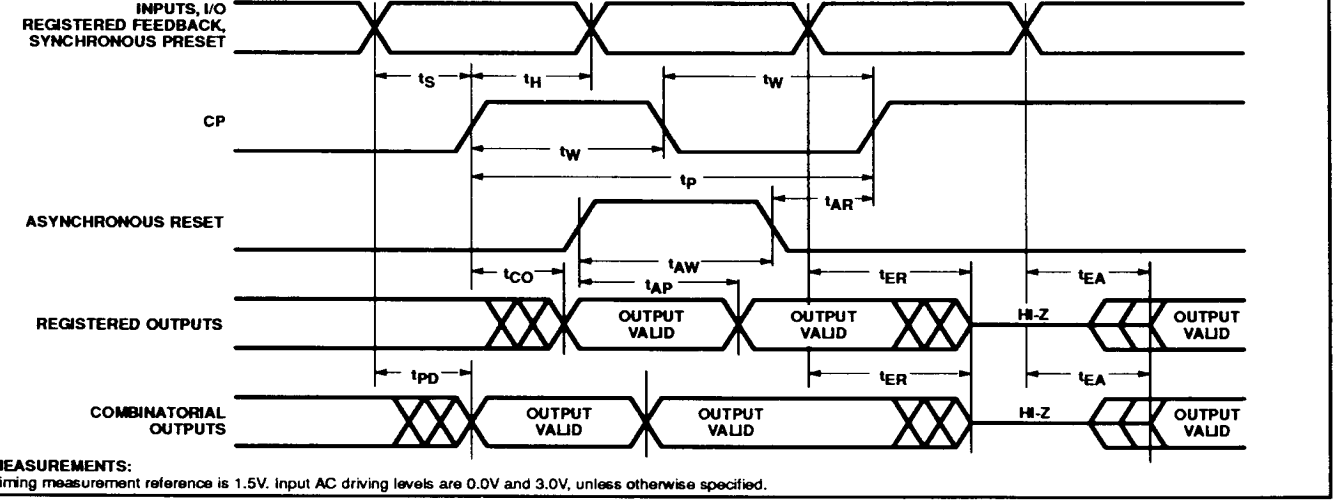
t_r, t_f < 5ns (10% to 90%)

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

OUTPUT TEST LOAD



TIMING DIAGRAMS

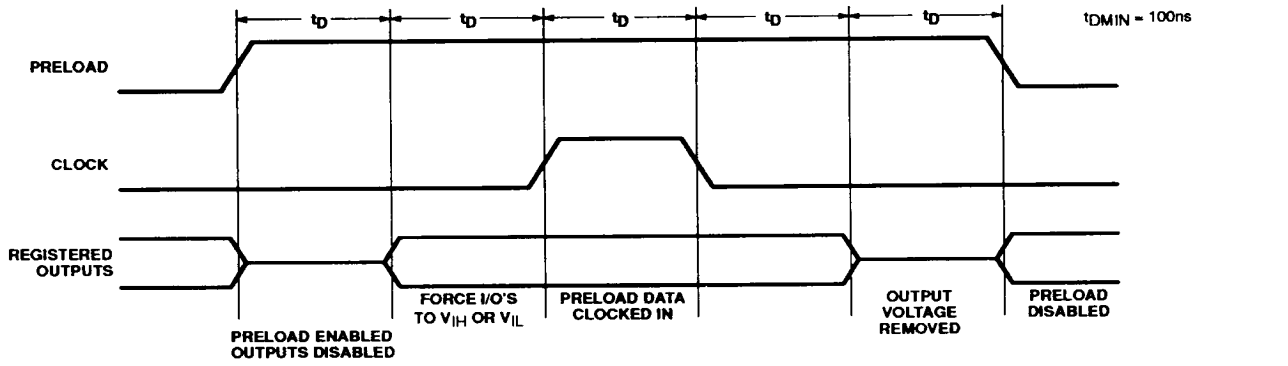


MEASUREMENTS:
Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

PRELOAD OF REGISTERED OUTPUTS

The PLV750's registers are provided with circuitry to allow loading of each register asynchronously with either a HIGH or a LOW. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A V_{IH} level on the I/O pin will force the register HIGH; a V_{IL} will force it LOW, independent of the polarity bit (S0) setting. The PRELOAD state is entered by placing an 11V to 14V signal on Pin 8 on DIPs, and Pin 10 on PLCCs. When the clock term is pulsed HIGH, the data on the I/O pin is placed into the register chosen by the Select Pin.



Output Register Preload

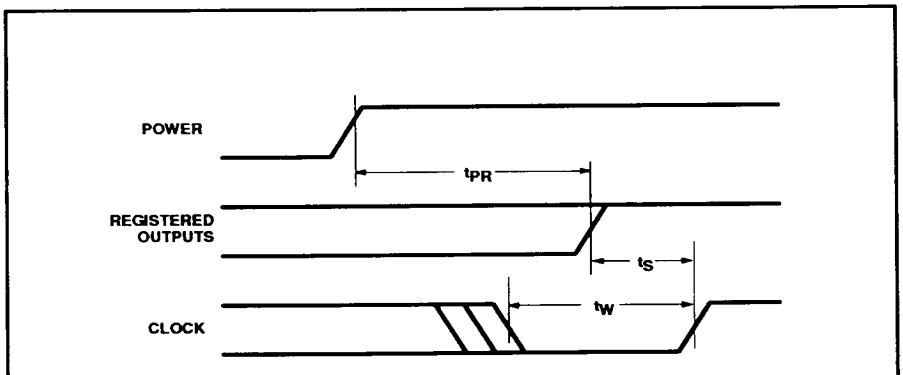
Level Forced on Registered Output Pin During PRELOAD Cycle	Select Pin State	Register #1 State after Cycle	Register #2 State after Cycle
V_{IH}	LOW	HIGH	X
V_{IL}	LOW	LOW	X
V_{IH}	HIGH	X	HIGH
V_{IL}	HIGH	X	LOW

POWER-UP RESET

The registers in the PLV750/L are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the LOW state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term HIGH, and
3. The signals from which the clock is derived must remain stable during t_{PR}.



Power-Up Reset

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{PR}	Power-Up Reset time		600	1000	ns

Powered by ICminer.com Electronic-Library Service CopyRight 2003

USING THE PLV750'S MANY ADVANCED FEATURES

The PLV750's flexibility puts more usable gates in 24 pins than other PLDs. The PLV750/L starts with an architecture similar to the popular PL22V10, and adds several features:

- Asynchronous clocks—
  Each of the flip-flops in the PLV750/L has a dedicated product term driving the clock. The user is no longer constrained to using one clock for all the registers. Buried state machines, counters, and registers can all coexist in one device, while running on separate clocks. The PLV750/L clock period matches that of similar synchronous devices.
- A full bank of 10 more registers—
  The PLV750/L provides two flip-flops for each Output Macrocell – a total of 20. Each register has its own clock and reset product terms, as well as its own sum term.
- Independent I/O pin and feedback paths—
  Each I/O pin on the PLV750/L has dedicated input path. Each of the 20 registers has individual feedback terms into the array. This feature, combined with individual product terms for each I/O's Output Enable, facilitates designs using bi-directional I/O buses.
- Combinable sum terms—
  Each Output Macrocell's 2 sum terms can be combined in an OR gate before the output or the register. This provides up to 16 product terms per output or flip-flop. This architecture increases the number of usable gates available.

PROGRAMMING SOFTWARE SUPPORT

Software which is capable of transforming Boolean equation, state machine descriptions and truth tables into JEDEC files for the PLV750/L is available from the following sources:

Data I/O / Futurenet Corp:
ABEL 2.1, 3.0, and above

Logical Devices:
CUPL 2.15B, and above.

SYNCHRONOUS PRESET AND ASYNCHRONOUS RESET

One synchronous preset line is provided for all 20 registers in the PLV750/L. The appropriate input signals to cause the internal clocks to go to a HIGH state must be received during a synchronous preset. Appropriate setup and hold times must be met, as shown in the timing diagrams.

An individual asynchronous reset line is provided for each of the 20 flip-flops. Both Master and Slave halves of the flip-flops are reset when the input signals received combine so as to force the internal resets HIGH.

SECURITY FUSE USAGE

A single fuse is provided to prevent unauthorized copying of the PLV750/L fuse patterns. Once programmed, the output buffers will remain in a high impedance state during verify.

The security fuse should be programmed last, as its effect is immediate.

ERASURE CHARACTERISTICS

The entire memory array of a PLV750/L is erased after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of $15 W \cdot sec/cm^2$. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

SIGNETICS CMOS PLDS

Signetics PLV750/L erasable Programmable Logic Devices utilize an advanced CMOS EPROM technology. This technology's state of the art features are the optimum combination for EPLDs:

- CMOS technology provides high speed, low power, and high noise immunity.
- EPROM technology is the most cost effective method for producing EPLDs – surpassing bipolar fusible link technology in low cost, while providing the necessary reprogrammability.
- EPROM reprogrammability, which is 100% tested before shipment, provides inherently better programmability and reliability than one-time fusible PLDs.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Signetics reserves the right to make changes without notice in the products, including circuits, standard cells, and/or software, described or contained herein, in order to improve design and/or performance. Signetics assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Signetics makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS

Signetics Products are not designed for use in life support appliances, devices, or systems where malfunction of a Signetics Product can reasonably be expected to result in a personal injury. Signetics customers using or selling Signetics Products for use in such applications do so at their own risk, and agree to fully indemnify Signetics for any damages resulting from such improper use or sale.

Powered by ICminer.com Electronic-Library Service CopyRight 2003

Philips – a worldwide company

Argentina: PHILIPS ARGENTINA S.A., Div. Philips Components, Vedia 3892, 1430 BUENOS AIRES, Tel. (01) 541-4261.
Australia: PHILIPS COMPONENTS PTY Ltd, 34 Waterloo Road, NORTH RYDE NSW 2113, Tel. (02) 805 4455. Fax. (02) 805 4466.
Austria: ÖSTERREICHISCHE PHILIPS INDUSTRIE G.m.b.H., UB Bauelemente, Triester Str. 64, 1101 WIEN, Tel. (0222) 60 101-820.
Belgium: N.V PHILIPS PROF. SYSTEMS – Components Div., 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02) 52 56 111.
Brazil: PHILIPS COMPONENTS (Active Devices & LCD) Rua do Rocio 220, SAO PAULO-SP, CEP 4552, P.O. Box 7383, CEP 01051, Tel. (011) 829-1166. Fax. (011) 829-1849. PHILIPS COMPONENTS (Passive Devices & Materials) Av. Francisco Monteiro 702, RIBEIRAO PIRES-SP, CEP 09400, Tel. (011) 459-8211. Fax. (011) 459-8282.
Canada: PHILIPS ELECTRONICS LTD., Philips Components, 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. (416) 292-5161. (IC Products) PHILIPS COMPONENTS – Signetics Canada LTD., 1 Eva Road, Suite 411, ETOBICOKE, Ontario, M9C 4Z5, Tel. (416) 626-6676.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. (02) 77 38 16.
Colombia: IPRELENSO LTDA., Carrera 21 No. 56-17, BOGOTA, D.E., P.O. Box 77621, Tel. (01) 249 76 24.
Denmark: PHILIPS COMPONENTS A/S, Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. 32-88 33 33.
Finland: PHILIPS COMPONENTS, Sinikalliontie 3, SF-2630 ESPOO, Tel. 358-0-50 261.
France: PHILIPS COMPOSANTS, 117 Quai du Président Roosevelt, 92134 ISSY-LES-MOULINEAUX Cedex, Tel. (01) 40 93 80 00, Fax. 01 409 38 692.
Germany: PHILIPS COMPONENTS UB der Philips G.m.b.H., Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0, Fax. 040 329 69 12.
Greece: PHILIPS HELLENIQUE S.A., Components Division, No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01) 4894 339/4894 911.
Hong Kong: PHILIPS HONG KONG LTD., Components Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-42 45 121. Fax. 0 480 69 60.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Components Dept., Shivsagar Estate 'A' Block, P.O. Box 6598, 254-D Dr. Annie Besant Rd., BOMBAY - 40 018, Tel. (022) 492 1500-492 1515. Fax. 022 494 1906 3.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Components Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan, JAKARTA 12910, Tel. (021) 51 79 95.
Ireland: PHILIPS ELECTRONICS (IRELAND) LTD., Components Division, Newstead, Clonskeagh, DUBLIN 14, Tel. (01) 693 355.
Italy: PHILIPS S.p.A., Philips Components, Piazza IV Novembre 3, I-20124 MILANO, Tel. (02) 6752.1, Fax. 02 675 226 42.
Japan: PHILIPS JAPAN LTD., Components Division, Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. (03) 813-3740-5030. Fax. 03 813 3740 570.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD. Components Division, Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. (02) 794-5011.
Malaysia: PHILIPS MALAYSIA SDN BHD, Components Div., 3 Jalan SS15/2A SUBANG, 47500 PETALING JAYA, Tel. (03) 734 5511.
Mexico: PHILIPS COMPONENTS, Paseo Triunfo de la Republica, No 215 Local 5, Cd Juarez CHI HUA HUA 32340 MEXICO Tel. (16) 18-67-01/02.
Netherlands: PHILIPS NEDERLAND B.V., Marktgroep Philips Components, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 783 749.
New Zealand: PHILIPS NEW ZEALAND LTD., Components Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. (09) 605-914.
Norway: NORSK A/S PHILIPS, Philips Components, Box 1, Manglerud 0612, OSLO, Tel. (02) 74 10 10.
Pakistan: PHILIPS ELECTRICAL CO. OF PAKISTAN LTD., Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021) 725772.
Peru: CADESA, Carretera Central 6.500, LIMA 3, Apartado 5612, Tel. 51-14-350 059.
Philippines: PHILIPS Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 911, MAKATI, Metro MANILA, Tel. (63-2) 810-0161. Fax. 632 817 3474.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (019) 68 31 21.
Singapore: PHILIPS SINGAPORE, PTE LTD., Components Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 350 2000.
South Africa: S.A. PHILIPS PTY LTD., Components Division, 195-215 Main Road, JOHANNESBURG 2000, P.O. Box 7430, Tel. (011) 470-5434. Fax. (011) 470 54 94.
Spain: PHILIPS COMPONENTS, Balmes 22, 08007 BARCELONA, Tel. (03) 301 63 12. Fax. 03 301 42 43.
Sweden: PHILIPS COMPONENTS, A.B., Tegeluddsvägen 1, S-11584 STOCKHOLM, Tel. (0)8-782 1000.
Switzerland: PHILIPS A.G., Components Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01) 488 22 11.
Taiwan: PHILIPS TAIWAN LTD., 581 Min Sheng East Road, P.O. Box 22978, TAIPEI 10446, Taiwan, Tel. 886-2-509 7666. Fax. 886 2 500 5899.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. (02) 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., Philips Components, Talatpasa Cad. No. 5, 80640 LEVENT/ISTANBUL, Tel. (01) 179 27 70.
United Kingdom: PHILIPS COMPONENTS LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. (071) 580 6633, Fax. 071 436 21 96.
United States: (Colour picture tubes – Monochrome & Colour Display Tubes) PHILIPS DISPLAY COMPONENTS COMPANY, 1600 Huron Parkway, P.O. Box 963, ANN ARBOR, Michigan 48106, Tel. 313/996-9400. Fax. 313 761 2886. (IC Products) PHILIPS COMPONENTS – Signetics, 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. (800) 227-1817. (Passive Components, Discrete Semiconductors, Materials and Professional Components & LCD) PHILIPS COMPONENTS, Discrete Products Division, 2001 West Blue Heron Blvd., P.O. Box 10330, RIVIERA BEACH, Florida 33404, Tel. (407) 881-3200.
Uruguay: PHILIPS COMPONENTS, Coronel Mora 433, MONTEVIDEO, Tel. (02) 70-4044.
Venezuela: MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, CARACAS 1074A, App. Post. 78117, Tel. (02) 241 75 09.
Zimbabwe: PHILIPS ELECTRICAL (PVT) LTD., 62 Mutare Road, HARARE, P.O. Box 994, Tel. 47211.

For all other countries apply to: Philips Components, Marketing Communications, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Telex 35000 phtcnl, Fax. +31-40-724825

ADS91
© Philips Export B.V. 1991

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

9397 328 90011

Philips Semiconductors

PHILIPS

PHILIPS

027332

Powered by ICminer.com Electronic-Library Service CopyRight 2003