

TOSHIBA CCD LINEAR IMAGE SENSOR CCD(Charge Coupled Device)

TCD1205D

The TCD1205D is a high sensitive and low dark current 2048-elements linear image sensor. The sensor can be used for POS handscanner.

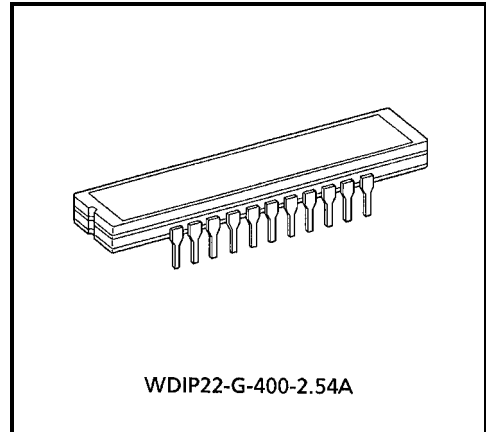
The device is operated by only 5V power supply, and mounted in 22-pin cerdip package with hermetic sealed optical glass window.

The TCD1205D has electronic shutter function (ICG).

Electronic shutter function can keep always output voltage constant that vary with the intensity of lights.

FEATURES

- Number of Image Sensing Elements : 2048
- Image Sensing Element Size : 14μm by 200μm on 14μm centers
- Photo Sensing Region : High sensitive and low dark current pn photodiode
- Clock : 2 phase (5V)
- Internal Circuit : Electronic shutter function (ICG)
- Package : 22 pin cerdip



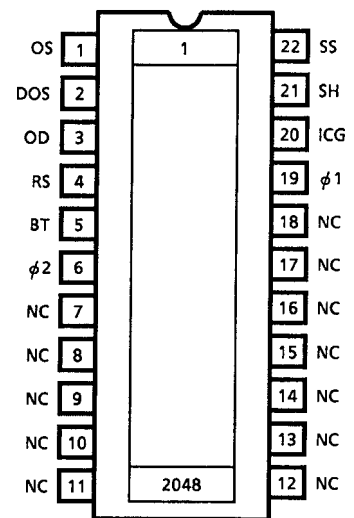
Weight: 4.4g (Typ.)

MAXIMUM RATINGS (Note 1)

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|--------------------------------------|------------------|---------|------|
| Clock Pulse Voltage | V_{ϕ} | -0.3~8 | V |
| Shift Pulse Voltage | V_{SH} | | |
| Reset, Boost Pulse Voltage | V_{RS}, V_{BT} | | |
| Integration Clear Gate Pulse Voltage | V_{ICG} | | |
| Power Supply Voltage | V_{OD} | | |
| Operating Temperature | T_{opr} | -25~60 | °C |
| Storage Temperature | T_{stg} | -40~100 | °C |

Note 1: All voltage are with respect to SS terminals (Ground).

PIN CONNECTION



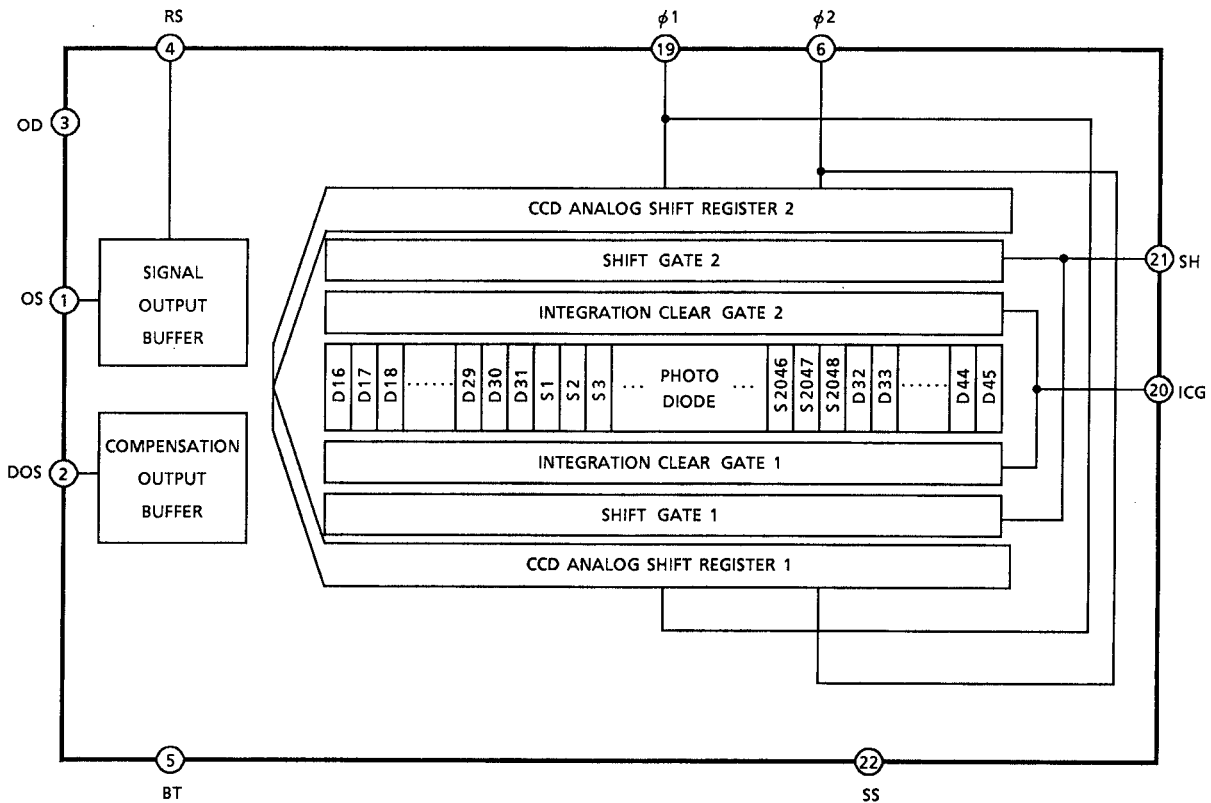
(TOP VIEW)

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CIRCUIT DIAGRAM



PIN NAMES

| | |
|----------|------------------------|
| $\phi 1$ | Clock (Phase 1) |
| $\phi 2$ | Clock (Phase 2) |
| RS | Reset Gate |
| SH | Shift Gate |
| ICG | Integration Clear Gate |
| BT | Boost Gate |
| OS | Signal Output |
| DOS | Compensation Output |
| OD | Power |
| SS | Ground |
| NC | Non Connection |

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OPTICAL / ELECTRICAL CHARACTERISTICS

(Ta = 25°C, VOD = 5V, Vφ = VSH = VRS = VBT = 5V (Pulse), fφ = 0.5MHz, fRS = 1MHz, Load Resistance = 100kΩ, tINT (Integration Time) = 10ms, Light Source = Daylight Fluorescent Lamp)

| CHARACTERISTIC | SYMBOL | MIN | TYP. | MAX | UNIT | NOTE |
|--------------------------------|----------|-------|------|-----|----------|----------|
| Sensitivity | R | 64 | 80 | — | V / lx·s | (Note 2) |
| Photo Response Non Uniformity | PRNU | — | — | 10 | % | (Note 3) |
| Saturation Output Voltage | VSAT | 0.55 | 0.8 | — | V | (Note 4) |
| Saturation Exposure | SE | 0.006 | 0.01 | — | lx·s | (Note 5) |
| Dark Signal Voltage | VMDK | — | 2 | 5 | mV | (Note 6) |
| DC Power Dissipation | PD | — | — | 25 | mW | |
| Total Transfer Efficiency | TTE | 92 | 95 | — | % | |
| Output Impedance | Zo | — | 0.5 | 1 | kΩ | |
| Dynamic Range | DR | — | 400 | — | — | (Note 7) |
| DC Signal Output Voltage | VOS | 1.5 | 3.0 | 4.5 | V | (Note 8) |
| DC Compensation Output Voltage | VDOS | 1.5 | 3.0 | 4.5 | V | (Note 8) |
| DC Mismatch Voltage | VOS-VDOS | — | — | 200 | mV | (Note 8) |

Note 2: Sensitivity for LED (660nm) is 600V / lx·s (Typ.)

Note 3: Measured at 50% of SE (Typ.)

$$\text{Definition of PRNU: } PRNU = \frac{\Delta\bar{\chi}}{\bar{\chi}} \times 100(\%)$$

Where $\bar{\chi}$ is average of total signal outputs and $\Delta\bar{\chi}$ is the maximum deviation from $\bar{\chi}$ under uniform illumination.

Note 4: VSAT is defined as minimum saturation output voltage of all effective pixels.

$$\text{Note 5: Definition of SE : } SE = \frac{VSAT}{R} (\text{lx}\cdot\text{s})$$

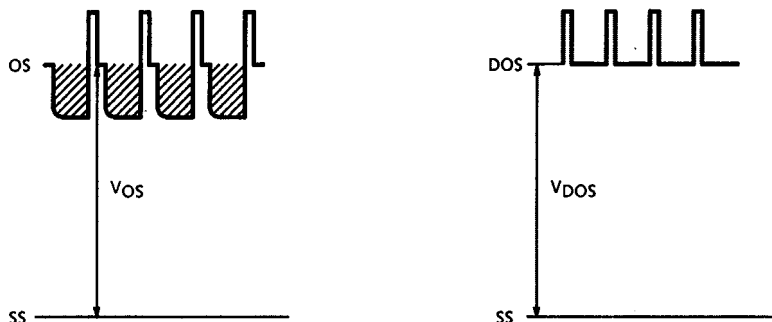
Note 6: VMDK is defined as maximum dark signal voltage of all effective pixels.



$$\text{Note 7: Definition of DR : } DR = \frac{VSAT}{VMDK}$$

VMDK is proportional to tINT (Integration time).
So the shorter tINT condition makes wider DR value.

Note 8: DC signal output voltage and DC compensation output voltage are defined as follows:



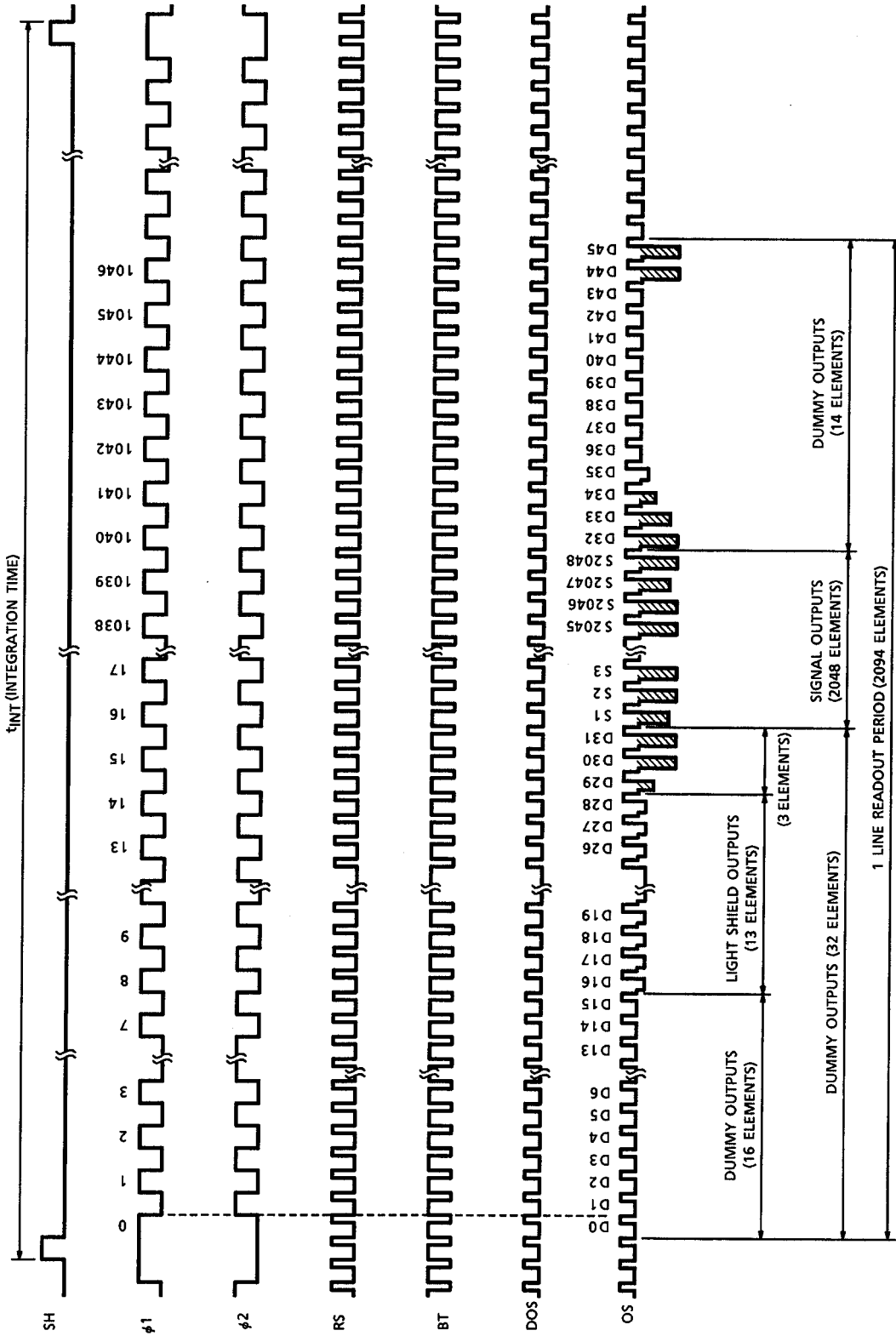
OPERATING CONDITION

| CHARACTERISTIC | | SYMBOL | MIN | TYP. | MAX | UNIT |
|--------------------------------|-----------|------------------|-----|------|-----|------|
| Clock Pulse Voltage | "H" Level | V_{ϕ} | 4.5 | 5.0 | 5.5 | V |
| | "L" Level | | 0 | 0.2 | 0.5 | |
| Shift Pulse Voltage | "H" Level | V_{SH} | 4.5 | 5.0 | 5.5 | V |
| | "L" Level | | 0 | 0.2 | 0.5 | |
| Reset, Boost Pulse Voltage | "H" Level | V_{RS}, V_{BT} | 4.5 | 5.0 | 5.5 | V |
| | "L" Level | | 0 | 0.2 | 0.5 | |
| Integration Clear Gate Voltage | "H" Level | V_{ICG} | 4.5 | 5.0 | 5.5 | V |
| | "L" Level | | 0 | 0.2 | 0.5 | |
| Power Supply Voltage | | V_{OD} | 4.5 | 5.0 | 5.5 | V |

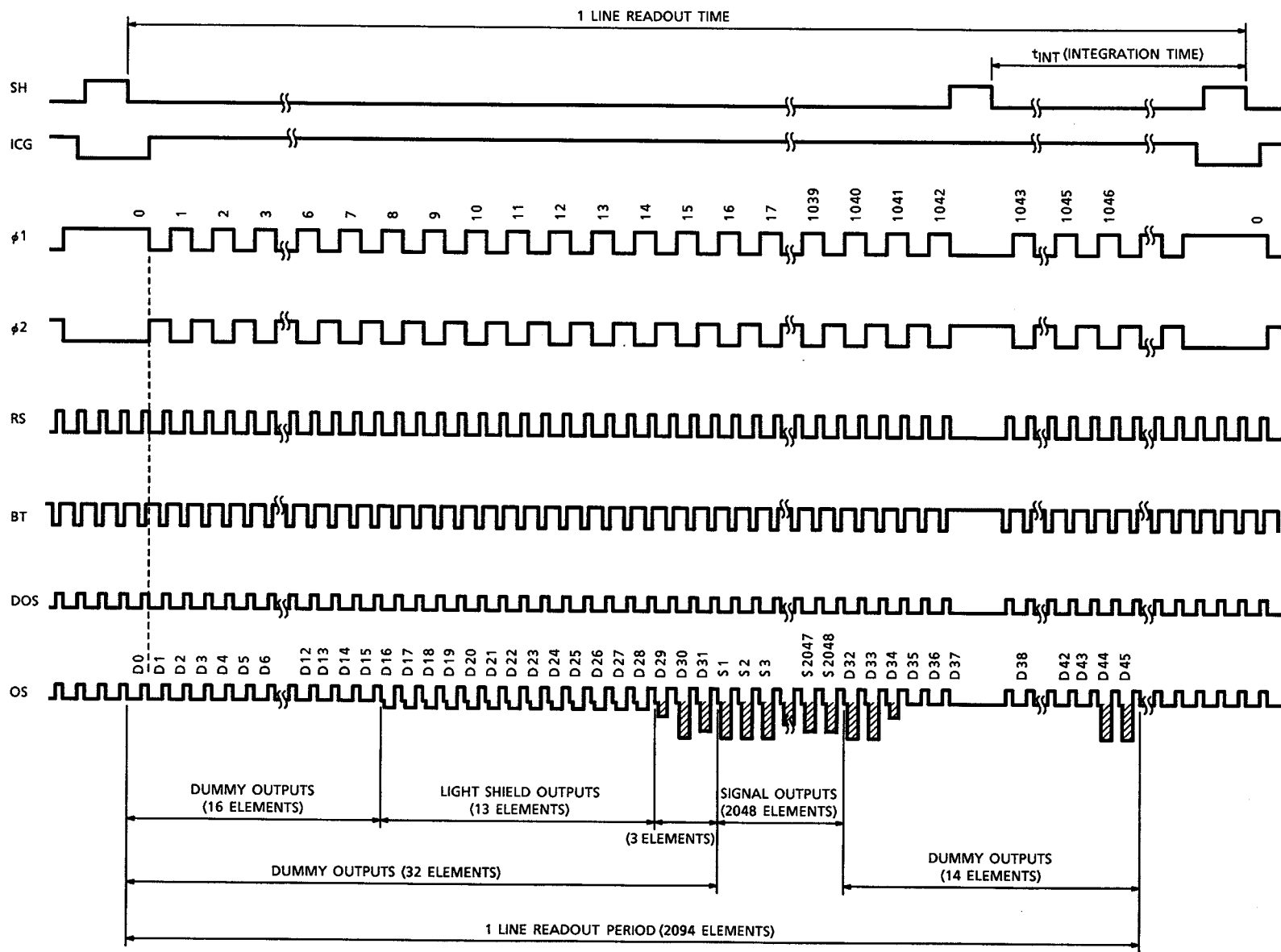
CLOCK CHARACTERISTICS (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | MIN | TYP. | MAX | UNIT |
|------------------------------------|--------------|------|------|-----|------|
| Clock Pulse Frequency | f_{ϕ} | 0.01 | 0.5 | 1.0 | MHz |
| Reset Pulse Frequency | f_{RS} | 0.02 | 1.0 | 2.0 | MHz |
| Clock Capacitance | $C_{\phi A}$ | — | 400 | 500 | pF |
| BT Gate Capacitance | C_{BT} | — | 10 | 25 | pF |
| Shift Gate Capacitance | C_{SH} | — | 200 | 250 | pF |
| Reset Gate Capacitance | C_{RS} | — | 10 | 25 | pF |
| Integration Clear Gate Capacitance | C_{ICG} | — | 100 | 200 | pF |

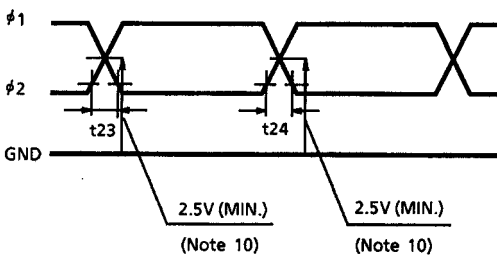
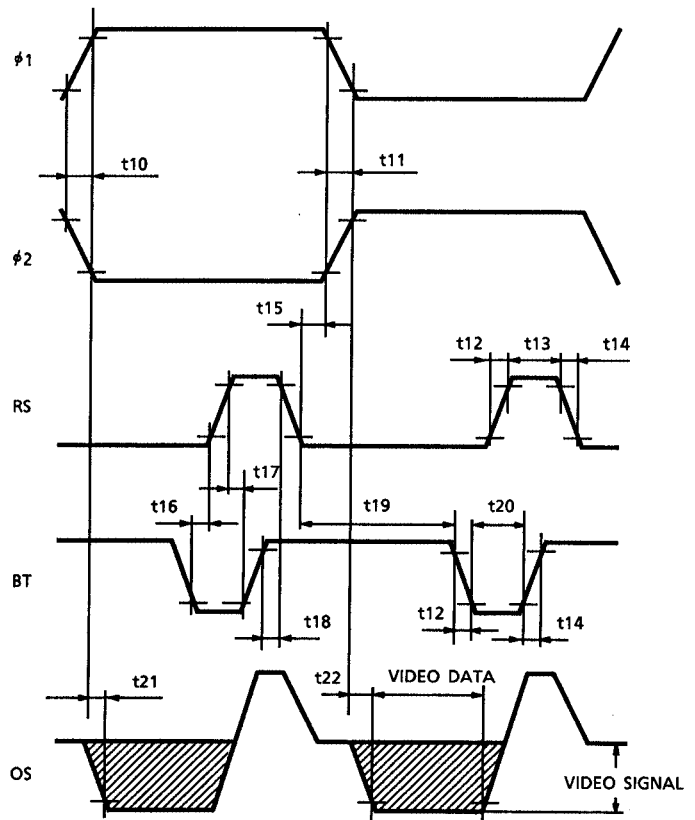
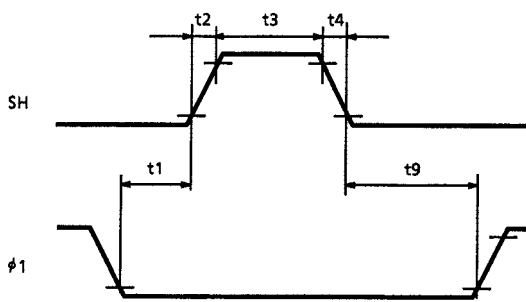
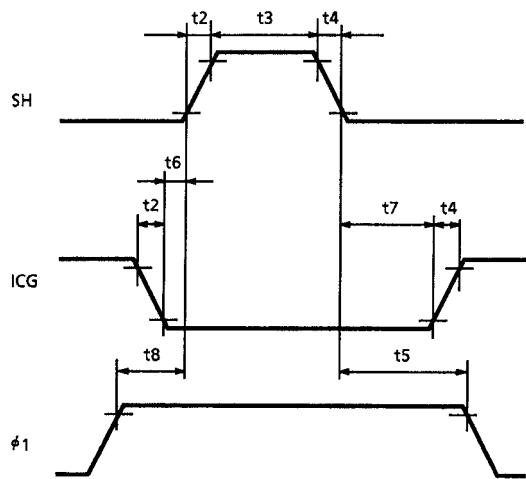
TAIMING CHART



TAIMING CHART (EXAMPLE : USE ELECTRONIC SHUTTER)



TIMING REQUIREMENTS

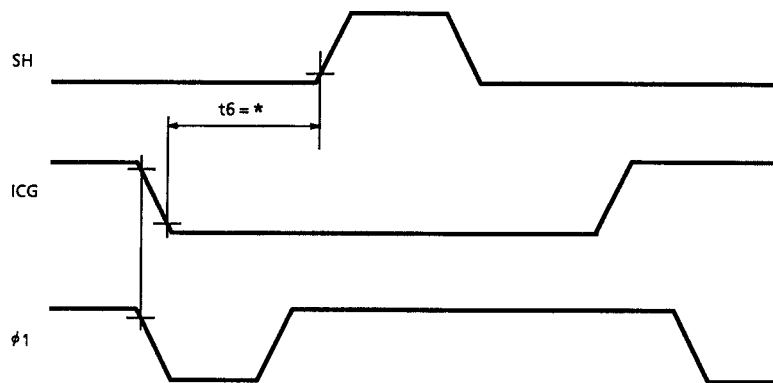


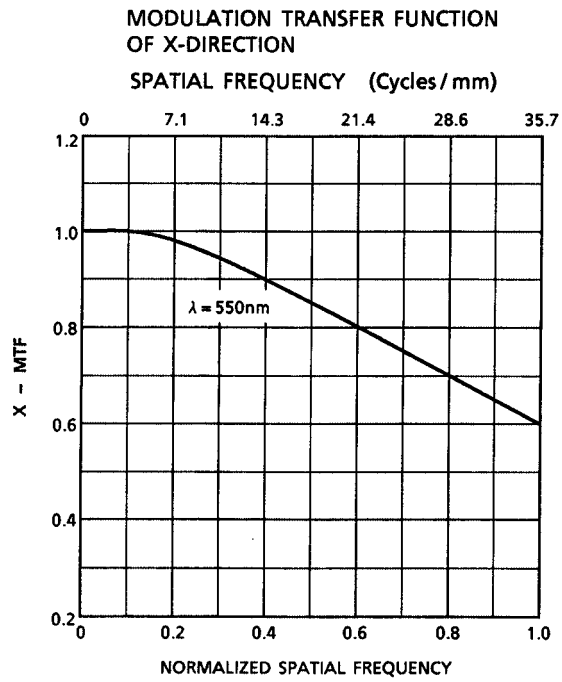
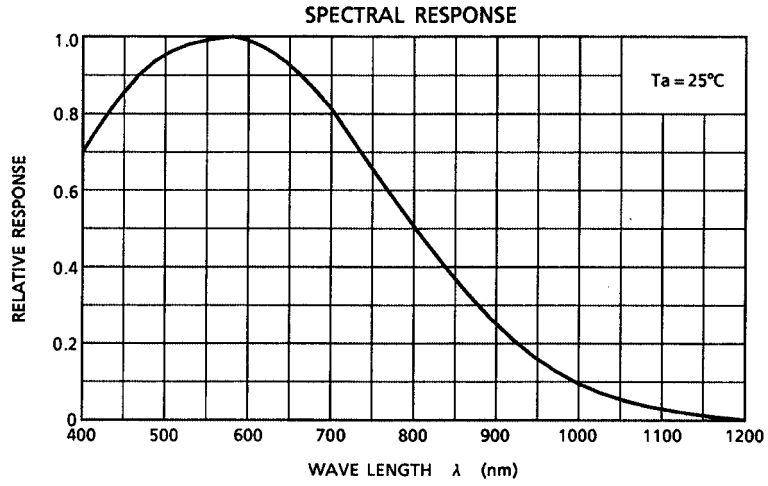
Note 10: If $\phi 1$ & $\phi 2$ pulse cross point couldn't be kept over 2.5V, it should be 1.5V and t_{23} and t_{24} should be 60ns.

| CHARACTERISTIC | SYMBOL | MIN | TYP. | MAX | UNIT |
|---|----------|------|------|-----|------|
| Pulse Timing of SH & ϕ 1 | t1 | 0 | 100 | — | ns |
| Pulse Timing of SH & ϕ 1 | t5 | 2000 | 3000 | — | ns |
| SH, ICG Pulse Rise & Fall Time | t2, t4 | 0 | 50 | — | ns |
| SH Pulse Width (Note 11) | t3, t3' | 1000 | 2000 | — | ns |
| Pulse Timing of SH & ICG | t6 | 50 | 100 | * | ns |
| Pulse Timing of SH & ICG | t7 | 1000 | — | t5 | ns |
| Pulse Timing of ICG & ϕ 1 | t8 | 0 | 100 | — | ns |
| Pulse Timing of ICG & ϕ 1 | t9 | 500 | — | — | ns |
| ϕ 1, ϕ 2 Pulse Rise & Fall Time | t10, t11 | 0 | 60 | — | ns |
| RS, BT Pulse Rise & Fall Time | t12, t14 | 0 | 60 | — | ns |
| RS Pulse Width | t13 | 60 | 260 | — | ns |
| Pulse Timing of ϕ 1, ϕ 2, RS | t15 | 20 | — | — | ns |
| Pulse Timing of RS & BT | t16 | 50 | 100 | — | ns |
| Pulse Timing of RS & BT | t17 | 20 | — | — | ns |
| Pulse Timing of RS & BT | t18 | 40 | — | — | ns |
| Pulse Timing of RS & BT | t19 | 200 | — | — | ns |
| BT Pulse Width | t20 | 70 | 250 | — | ns |
| Video Data Delay Time | t21, t22 | — | 80 | — | ns |

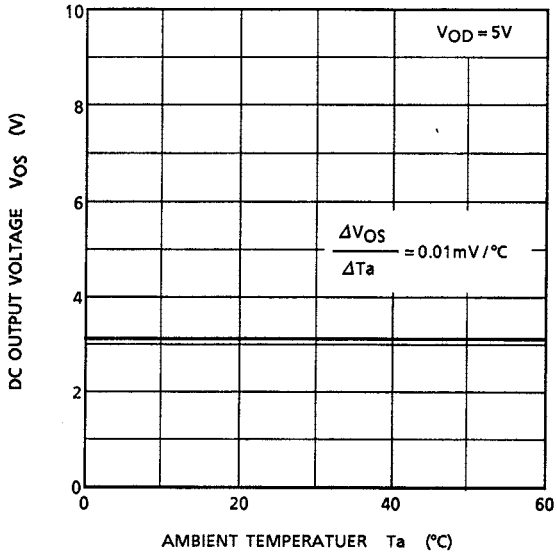
Note 11: Have to use t3 = t3'

* t6 = MAXIMUM TIMING

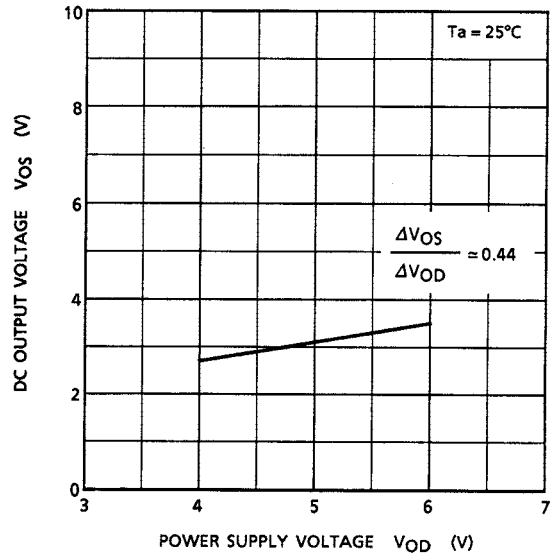




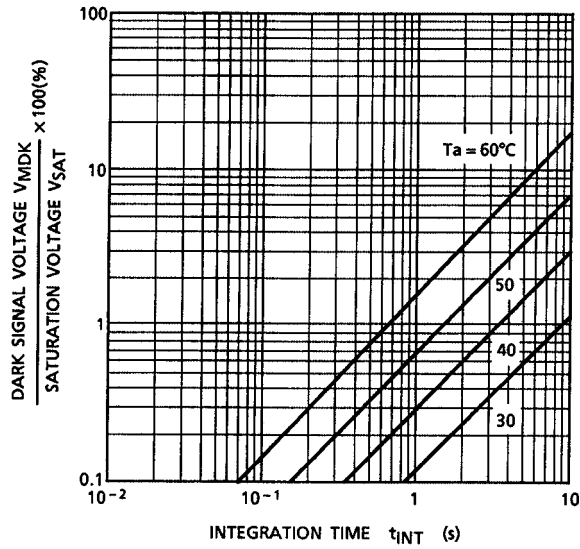
DC OUTPUT VOLTAGE – AMBIENT TEMPERATURE



DC OUTPUT VOLTAGE – POWER SUPPLY VOLTAGE



DARK SIGNAL VOLTAGE – INTEGRATION TIME



CAUTION**1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming

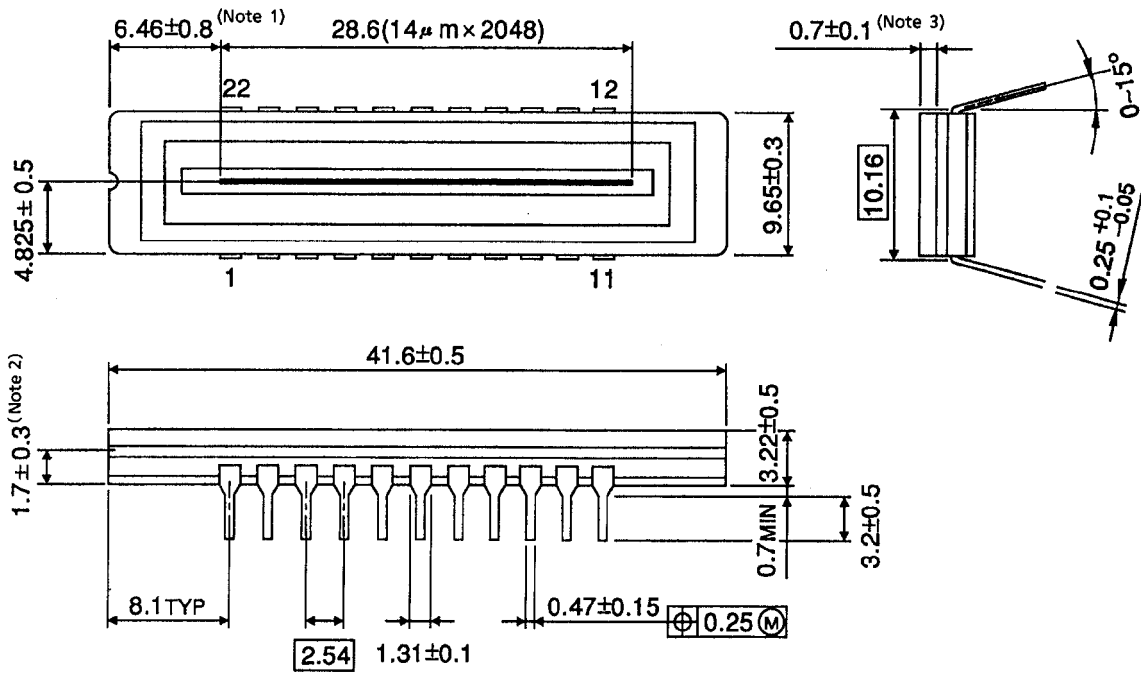
Since this package is not stout against mechanical stress, you should not reform the lead frame.

We recommend to use a IC-inserter when you assemble to PCB.

PACKAGE DIMENSIONS

WDIP22-G-400-2.54A (D)

Unit: mm



Note 1: No. 1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE.

Note 2: TOP OF CHIP TO BOTTOM OF PACKAGE.

Note 3: GLASS THICKNES (n = 1.5)

Weight: 4.4g (Typ.)