

Quad, 12-Bit DACs Voltage Output with Readback

DAC8412/DAC8413

FEATURES

+5 to ±15 Volt Operation Unipolar or Bipolar Operation True Voltage Output Double-Buffered Inputs Reset to Min or Center Scale Fast Bus Access Time Readback

APPLICATIONS

Automatic Test Equipment
Digitally Controlled Calibration
Servo Controls
Process Control Equipment

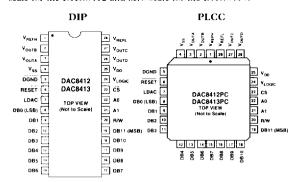
GENERAL DESCRIPTION

The DAC8412 and DAC8413 are quad, 12-bit voltage output DACs with readback capability. Built using a complementary BiCMOS process, these monolithic DACs offer the user very high package density.

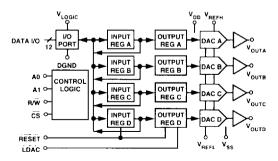
Output voltage swing is set by the two reference inputs $V_{\rm REFH}$ and $V_{\rm REFL}$. By setting the $V_{\rm REFL}$ input to 0 volts and $V_{\rm REFL}$ to a positive voltage, the DAC will provide a unipolar positive output range. A similar configuration with $V_{\rm REFH}$ at 0 volts and $V_{\rm REFL}$ at a negative voltage will provide a unipolar negative output range. Bipolar outputs are configured by connecting both $V_{\rm REFH}$ and $V_{\rm REFL}$ to nonzero voltages. This method of setting output voltage range has advantages over other bipolar offsetting methods because it is not dependent on internal and external resistors with different temperature coefficients.

Digital controls allow the user to load or read back data from any DAC, load any DAC and transfer data to all DACs at one time.

An active low RESET loads all DAC output registers to midscale for the DAC8412 and zero scale for the DAC8413.



FUNCTIONAL BLOCK DIAGRAM



The DAC8412/DAC8413 are available in 28-pin plastic DIP, cerdip, PLCC and LCC packages. They can be operated from a wide variety of supply and reference voltages with supplies ranging from single ± 5 volt to ± 15 volts, and references from ± 2.5 to ± 10 volts. Power dissipation is less than 330 mW with ± 15 volt supplies and only 60 mW with a ± 5 volt supply.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC8412/DAC8413/883 data sheet which specifies operation over the 55°C to +125°C temperature range. All 883 parts are also available on Standard Military Drawings 5962-91-76401MXA through -76404M3A.

ORDERING INFORMATION¹

INL (LSB)	Military ² Temperature -55°C to +125°C	Extended Industrial ² Temperature -40°C to +85°C	Package	Package Option	
± 1		DAC8412FPC	PLCC	P-28A	
+1.5	DAC8412BTC/883		LCC	E-28A	
±0.5		DAC8412ET	Cerdip	Q-28	
±0.75	DAC8412AT/883		Cerdip	Q-28	
± 1		DAC8412FT	Cerdip	Q-28	
±1.5	DAC8412BT/883		Cerdip	Q-28	
±0.5		DAC8412EP	Plastic	N-28	
± 1		DAC8412FP	Plastic	N-28	
± 1		DAC8412GBC	Dice	ĺ	
±1		DAC8413FPC	PLCC	P-28A	
±1.5	DAC8413BTC/883		LCC	E-28A	
±0.5	1	DAC8413ET	Cerdip	Q-28	
± 0.75	DAC8413AT/883		Cerdip	Q-28	
±1		DAC8413FT	Cerdip	Q-28	
±1.5	DAC8413BT/883		Cerdip	Q-28	
±0.5		DAC8413EP	Plastic	N-28	
± 1		DAC8413FP	Plastic	N-28	
<u>†</u> 1		DAC8413GBC	Dice	i	

NOTES

Burn-in is available on extended industrial temperature range parts in cerdip. A complete 3883 data sheet is available. For availability and burn in information, contact your local sales office.

To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212 or visit our World Wide Web site at http://www.analog.com.

For outline information see Package Information section

Parameter	Symbol	Conditions	Min	Тур	Max	Units
Integral Linearity "E"	INI.			0.25	± 0.5	LSB
Integral Linearity "F"	INI.		1		± L	LSB
Differential Linearity	DNL	Monotonic Over Temperature	1			LSB
Min Scale Error	V_{ZSE}	$R_{\rm L} = 2 k\Omega$	ĺ		± 2	LSB
Full-Scale Error	V_{ESE}	$R_1 = 2 k\Omega$			± 2	LSB
Min Scale Tempco	TCVZSE	$R_1 = 2 k\Omega$		15		ppm/°(
Full-Scale Tempco	TCV _{ESE}	$R_{1} = 2 k\Omega$		20		ppm/°(
MATCHING PERFORMANCE Linearity Matching				± 1		LSB
REFERENCE						
Positive Reference Input Range	1	Note 2	$V_{REFI} + 2.5$;	$V_{\rm DD} = 2.5$	v
Negative Reference Input Range		Note 2	-10		V _{REFH} 2.5	v
Reference High Input Current	IRFFH		2.75	+1.5	+2.75	mA
Reference Low Input Current	I_{REFL}		0	+2	+2.75	mA
AMPLIFIER CHARACTERISTICS						
Output Current	I_{OUT}		5		+5	mA
Settling Time	t _S	to 0.01%		6		μs
Slew Rate	SR	10% to 90%	ļ	2.2		V/µs
LOGIC CHARACTERISTICS						
Logic Input High Voltage	V _{INH}	$T_A = +25^{\circ}C$	2.4			V
Logic Input Low Voltage	V_{INL}	$T_A = +25^{\circ}C$			0.8	V
Logic Output High Voltage	V _{OH}	$I_{OH} = +0.4 \text{ mA}$	2.4			V
Logic Output Low Voltage	V _{o1} .	$I_{OL} = 1.6 \text{ mA}$			0.4	V
Logic Input Current	I _{IN}				1	μA
Input Capacitance	C _{IN}			8		pF
Crosstalk Large Signal Bandwidth		$-3 \text{ dB}, V_{REFH} = 0 \text{ to } +10 \text{ V p-p}$		>72 160		dB kHz
LOGIC TIMING CHARACTERISTICS	+	Note 3		100		Kriz
WRITE		Note 3				
Chip Select Write Pulse Width	twes		80	40		ns
Write Setup Write Hold	tws	$t_{WCS} = 80 \text{ ns}$	0			ns
Address Setup	t _{wH}	$t_{WCS} = 80 \text{ ns}$	0			ns
Address Hold	tas		0 0			ns
Load Setup	t _{AH}		70	30		ns
Load Hold	tis		30	10		ns
Write Data Setup	t _{IH} t _{wDS}	$t_{WCS} = 80 \text{ ns}$	20	10		ns ns
Write Data Hold	twos	$t_{WCS} = 80 \text{ ns}$	0			ns
Load Pulse Width	tiwo	1W1.S = 50 Ha	170	130		ns
Reset Pulse Width	treser		140	100		ns
READ	1		†			-
Chip Select Read Pulse Width	t _{RCS}		130	100		ns
Read Data Hold	t _{RDH}	$t_{RCS} = 130 \text{ ns}$	0	-		ns
Read Data Setup	t _{RDS}	$t_{RCS} = 130 \text{ ns}$	0			ns
Data to Hi Z	t _{DZ}	$C_L = 10 \text{ pF}$		150		ns
Chip Select to Data	t _{CSD}	$C_L = 100 \text{ pF}$		120	160	ns
SUPPLY CHARACTERISTICS						
Power Supply Sensitivity	PSS	$14.25 \text{ V} \le \text{V}_{\text{DD}} \le 15.75 \text{ V}$	Į.		150	ppm/V
Positive Supply Current	I_{DD}	$V_{REFH} = +2.5 \text{ V}$	1	8.5	12	mA
Negative Supply Current	I_{SS}		10	6.5		mA
Power Dissipation	P _{DISS}		1		330	mW

6-138 D/A CONVERTERS REV. C

¹All supplies can be varied 2.5%, and operation is guaranteed. Device is tested with nominal supplies.

^{*}Operation is guaranteed over this reference range, but linearity is neither tested no guaranteed.

All input control signals are specified with tr = tf = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

Specifications subject to change without notice.