Integrated Device Technology, Inc.

256K X 4 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4042

FEATURES:

- High density 1 megabit CMOS static RAM module
- Equivalent to the JEDEC standard for future monolithic 256K x 4 with output enable static RAMs
- Fast access time
  - — Commercial: 30ns (max.)
  - — Military: 35ns (max.)
- Surface mounted leadless chip carriers on an 28-pin 400 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL compatible
- Modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

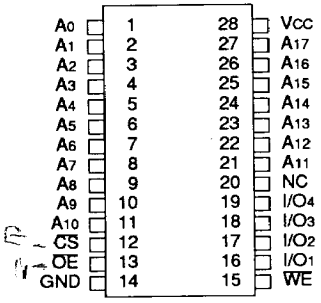
The IDT7M4042 is a (256K x 4 with output enable) static RAM module constructed on a co-fired ceramic substrate using four (64K x 4) static RAMs and an IDT74FCT139 decoder in leadless chip carriers. Extremely fast speeds can be achieved using 256K static RAMs and logic fabricated in IDT's high performance, high-reliability CEMOS™ technology. The IDT7M4042 is available with access times as fast as 30ns commercial and 35ns military with minimal power consumption.

The IDT7M4042 is packaged in a 28-pin ceramic DIP. This results in a package 1.6 inches long, 400 mils wide and only 280 mils thick.

All inputs and outputs of the IDT7M4042 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation.

All IDT7M4042 military module semiconductor components are compliant to the latest revision of MIL-STD-883, Class B, making them ideally suited for applications demanding the highest levels of performance and reliability.

PIN CONFIGURATION[1]



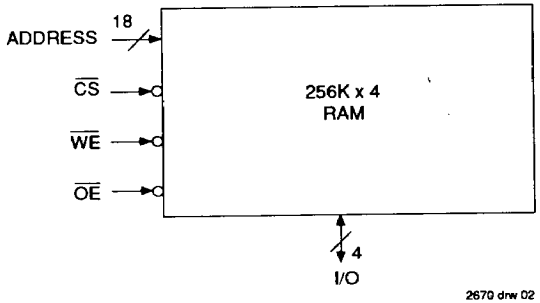
DIP
TOP VIEW

2670 drw 01

NOTE:

1. For module dimensions, please refer to module drawing M2 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

I/O1-4	Data Inputs/Outputs
A0-17	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

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NOTE:
1. VIL = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = -55°C to + 125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
ILI	Input Leakage	VCC = Max. VIN = GND to VCC	—	40	uA
ILO	Output Leakage	VCC = Max. $\overline{CS}$ = VIH, VOUT = GND to VCC	—	40	uA
VOL	Output Low Voltage	VCC = Min. IOL = 8mA VCC = Min. IOL = 10mA	— —	0.4 0.5	V V
VOH	Output High Voltage	VCC = Min. IOH = -4mA	2.4	—	V

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Symbol	Parameter	Test Conditions	Max.	Unit
ICC	Dynamic Operating Current	VCC = Max. $\overline{CS}$ = VIL f = fMAX; Outputs Open	320	mA
ISB	Standby Supply Current	VCC = Max. $\overline{CS}$ = VIH f = fMAX; Outputs Open	148	mA
ISB1	Full Standby Supply Current	$\overline{CS}$ ≥ VCC -0.2V VIN > VCC -0.2V or < 0.2V	122	mA

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TRUTH TABLE

Mode	$\overline{CS}$xx	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

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CAPACITANCE(1) (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN(1)	Input Capacitance	VIN = 0V	40	pF
CIN(2)	Input Capacitance ($\overline{CS}$, A16-17)	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

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NOTE:
1. This parameter guaranteed by design, but not tested.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to + 125°C or 0°C to +70°C)

Symbol	Parameters	7M4042S30 Min.	7M4042S30 Max.	7M4042S35 Min.	7M4042S35 Max.	7M4042S45 Min.	7M4042S45 Max.	7M4042S55 Min.	7M4042S55 Max.	7M4042S65 Min.	7M4042S65 Max.	7M4042S80 Min.	7M4042S80 Max.	Unit
Read Cycle														
tRC	Read Cycle Time	30	—	35	—	45	—	55	—	65	—	80	—	ns
tAA	Address Access Time	—	30	—	35	—	45	—	55	—	65	—	80	ns
tACS	Chip Select Access Time	—	30	—	35	—	45	—	55	—	65	—	80	ns
tCLZ(1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	12	—	15	—	27	—	32	—	37	—	47	ns
tOLZ(1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ(1)	Chip Select to Output in High Z	—	18	—	21	—	23	—	28	—	33	—	38	ns
tOHZ(1)	Output Disable to Output in High Z	—	10	—	13	—	15	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	30	—	35	—	45	—	55	—	65	—	80	ns
Write Cycle														
tWC	Write Cycle Time	30	—	35	—	45	—	55	—	65	—	80	—	ns
tCW	Chip Select to End of Write	30	—	30	—	40	—	50	—	60	—	70	—	ns
tAW	Address Valid to End of Write	30	—	30	—	40	—	50	—	60	—	70	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	22	—	30	—	40	—	50	—	60	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	2	—	2	—	2	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	13	—	13	—	15	—	20	—	25	—	30	ns
tDW	Data to Write Time Overlap	15	—	17	—	22	—	27	—	32	—	40	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW(1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	5	—	ns

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NOTE:
1. This parameter is guaranteed by design, but not tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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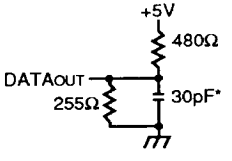

Figure 1. Output Load

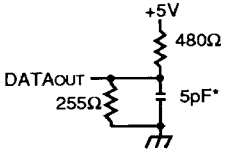

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Figure 2. Output Load

(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, tWHZ)

*** Including scope and jig.**

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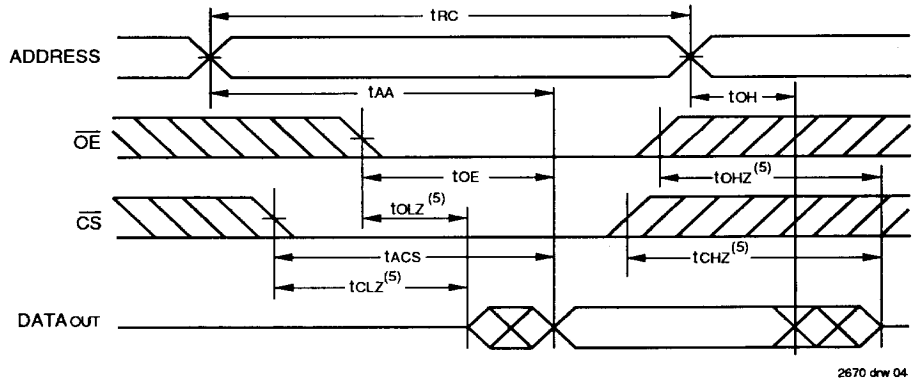
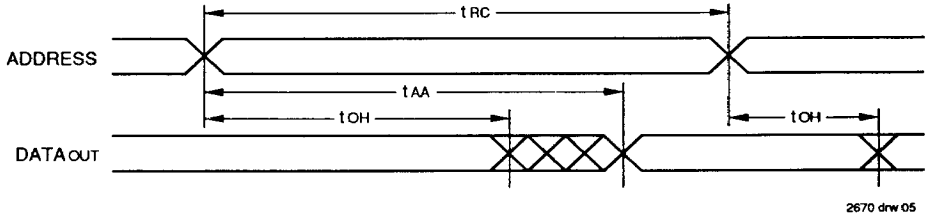
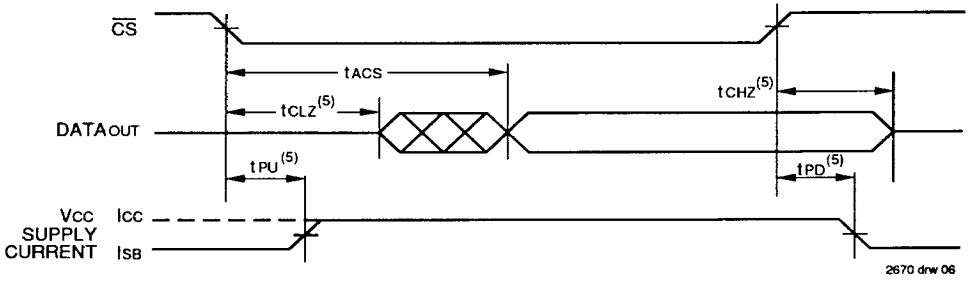
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)

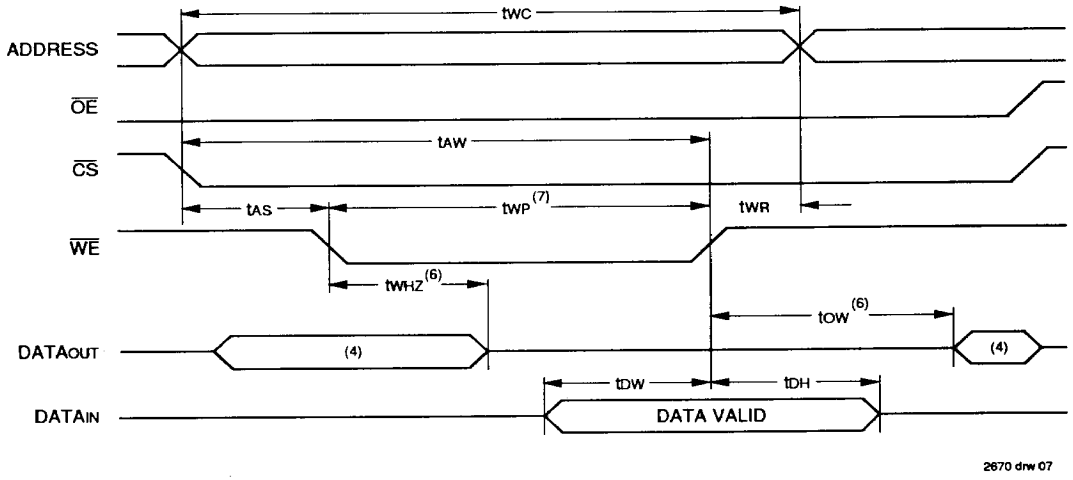


TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)

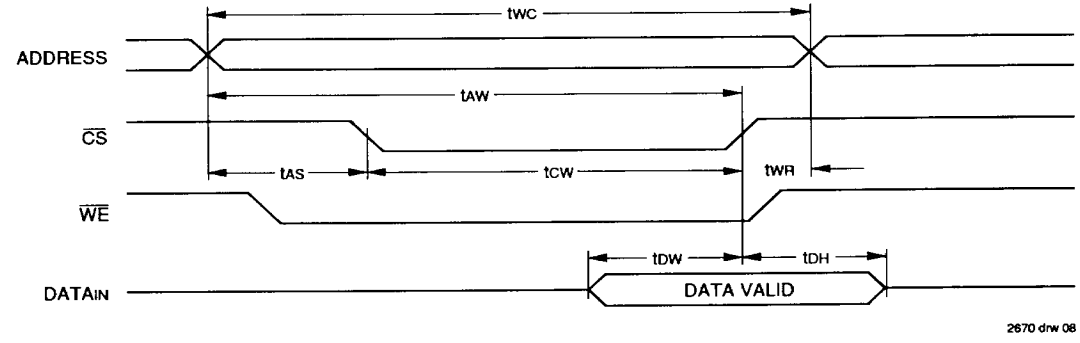


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

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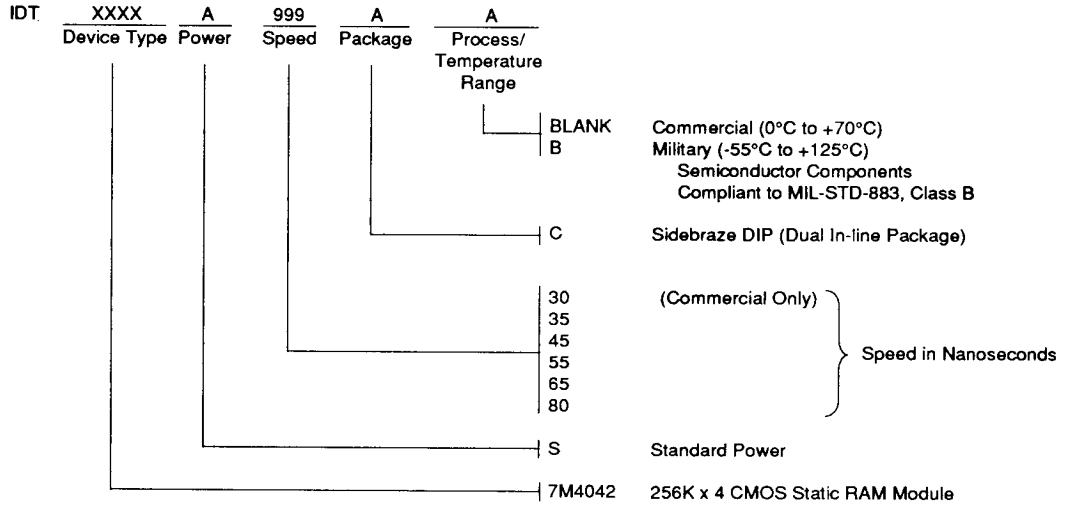
ORDERING INFORMATION



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