Integrated Device Technology, Inc.

256KB AND 512KB SECONDARY CACHE MODULES FOR THE INTEL® PENTIUM™ CPU AND VLSI WILDCAT CORE LOGIC

PRELIMINARY
IDT7MPV6239
IDT7MPV6240
IDT7MPV6241
IDT7MPV6244

FEATURES

- For Intel 3.3V Pentium-based systems using the VLSI Wildcat core logic chipset
- Asynchronous and pipelined burst SRAM option in the same module pinout
- Low-cost, low-profile card edge module with 160 leads
- Uses Burndy Computerbus™ connector, part number CELP2X80SC3Z48
- Operates with 3.3V Pentium™ processor external speeds of 66MHz
- Separate 5V (±5%) and 3.3V (±10%) power supplies
- Multiple GND pins and decoupling capacitors for maximum noise immunity

DESCRIPTION

The IDT7MPV6239/40/41/44 are 256KB/512KB secondary caches that are ideal for use with the VLSI Wildcat core logic chipset for Intel 3.3V Pentium CPU-based systems. The IDT7MPV6239/40 use IDT's asynchronous CacheRAMs™ and high-speed 16-bit IDT FCT logic, and the IDT7MPV6241/44 use IDT's 71V432 32Kx32 pipelined burst SRAMs in plastic surface mount packages, mounted on a multilayer epoxy laminate (FR-4) board. In addition, each of the modules uses 5V IDT71B74 Cache tag SRAM. Extremely high speeds are achieved using IDT's high-performance, high-reliability CMOS technology. The IDT7MPV6241/44 specifications are advance information only.

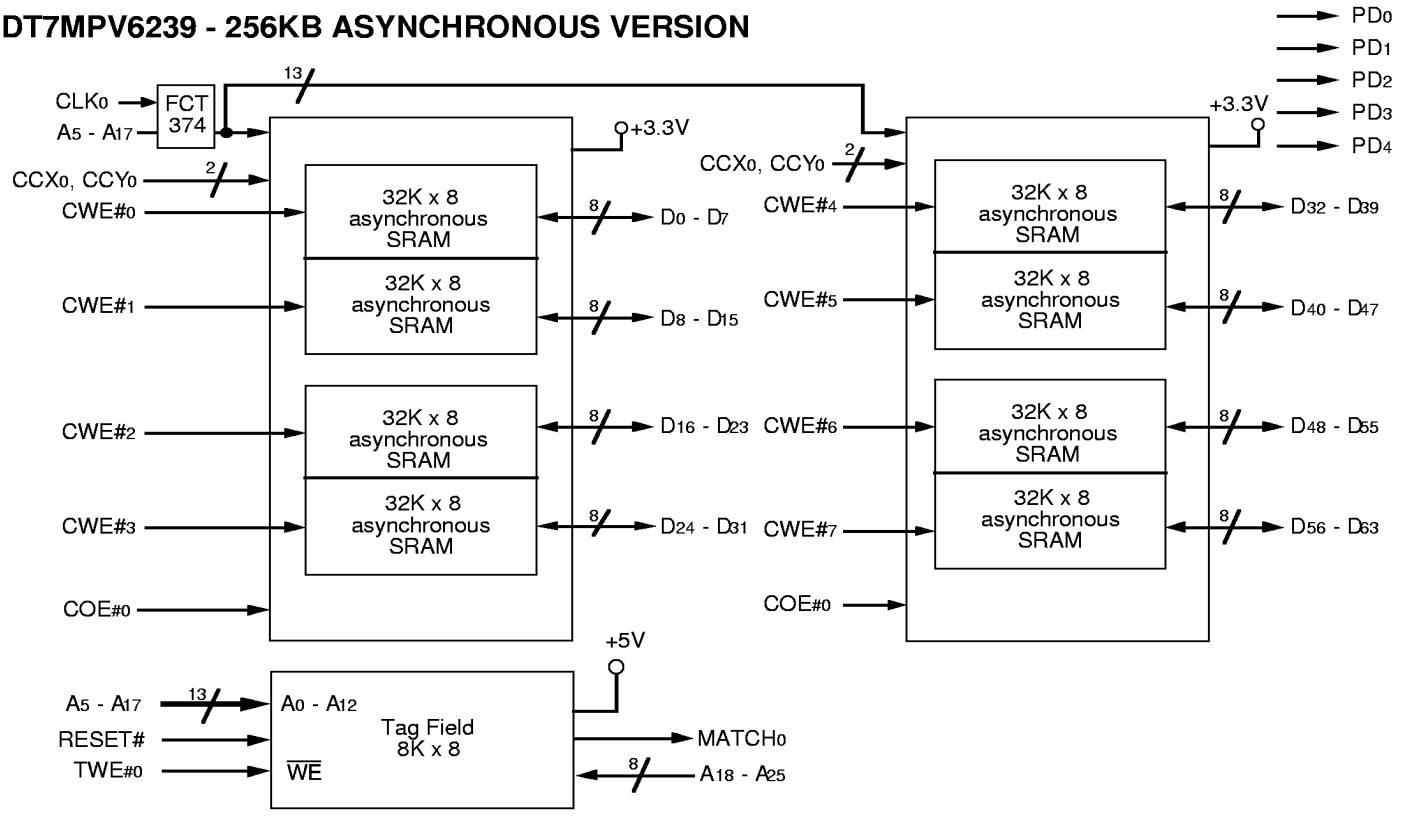
This family of cache modules have Presence Detect pins which enable active probing by the system to determine the cache size and type actually plugged into the socket. This feature supports multiple cache options without the need to change jumpers at the system level.

The low-profile card edge package configuration allows 160 signal leads to be placed on a package 4.35" long. Depending on which cache configuration is used, the module is a maximum of 0.365" thick and a maximum of 1.16" tall.

All inputs and outputs of the IDT7MPV6239/40/41/44 are TTL-compatible. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6239 - 256KB ASYNCHRONOUS VERSION



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COMMERCIAL TEMPERATURE RANGE **FEBRUARY 1995**

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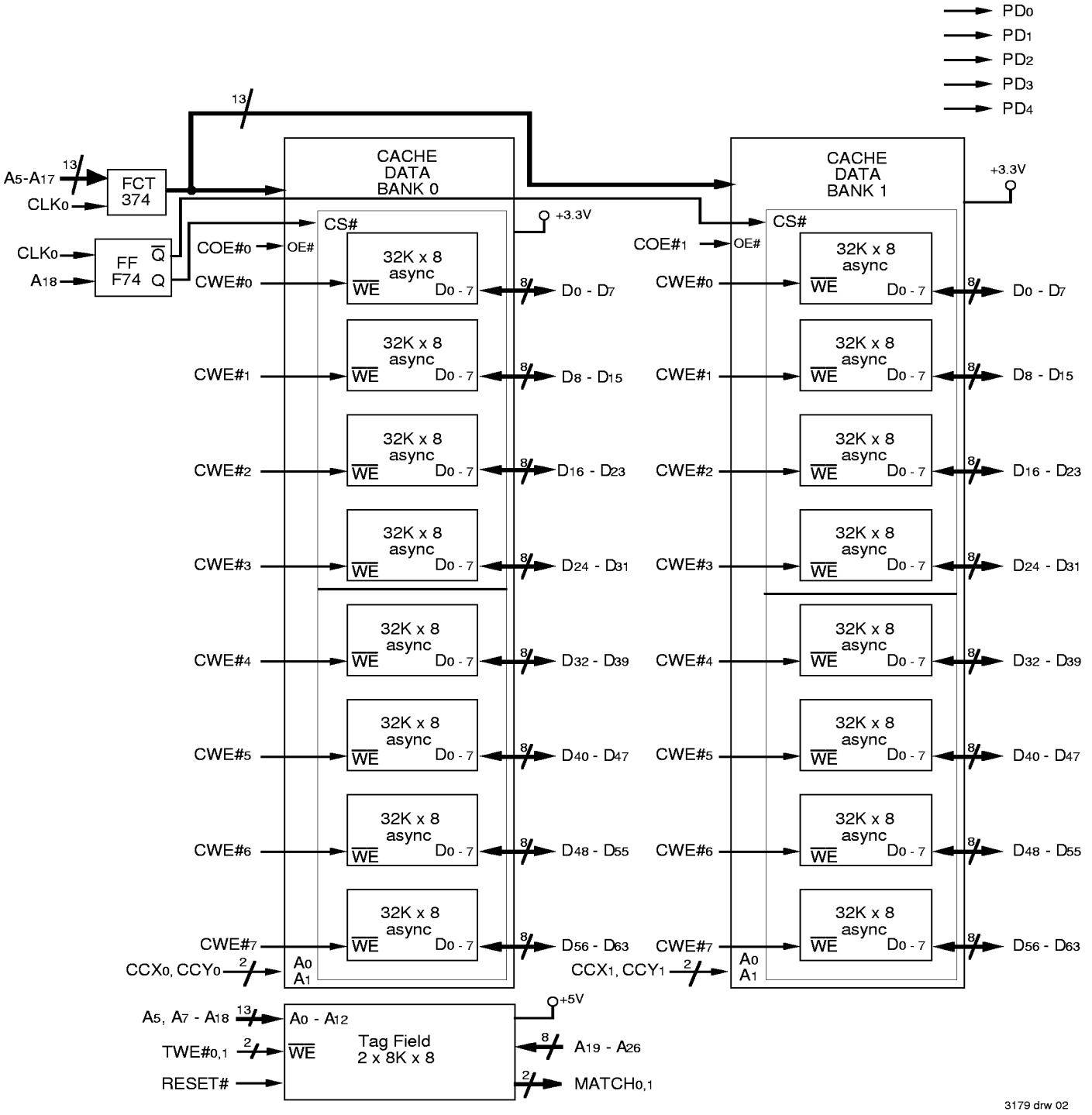
FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6240 - 512KB ASYNCHRONOUS VERSION



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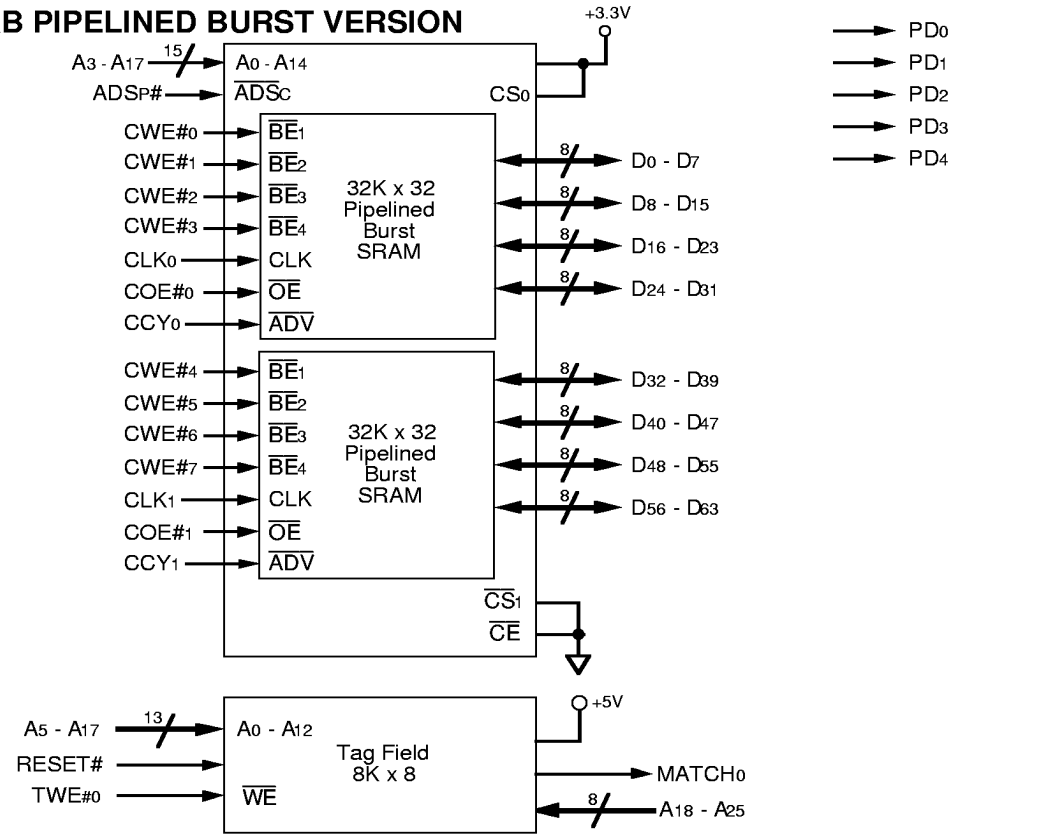
FUNCTIONAL BLOCK DIAGRAM

IDT7MPV6241 - 256KB PIPELINED BURST VERSION



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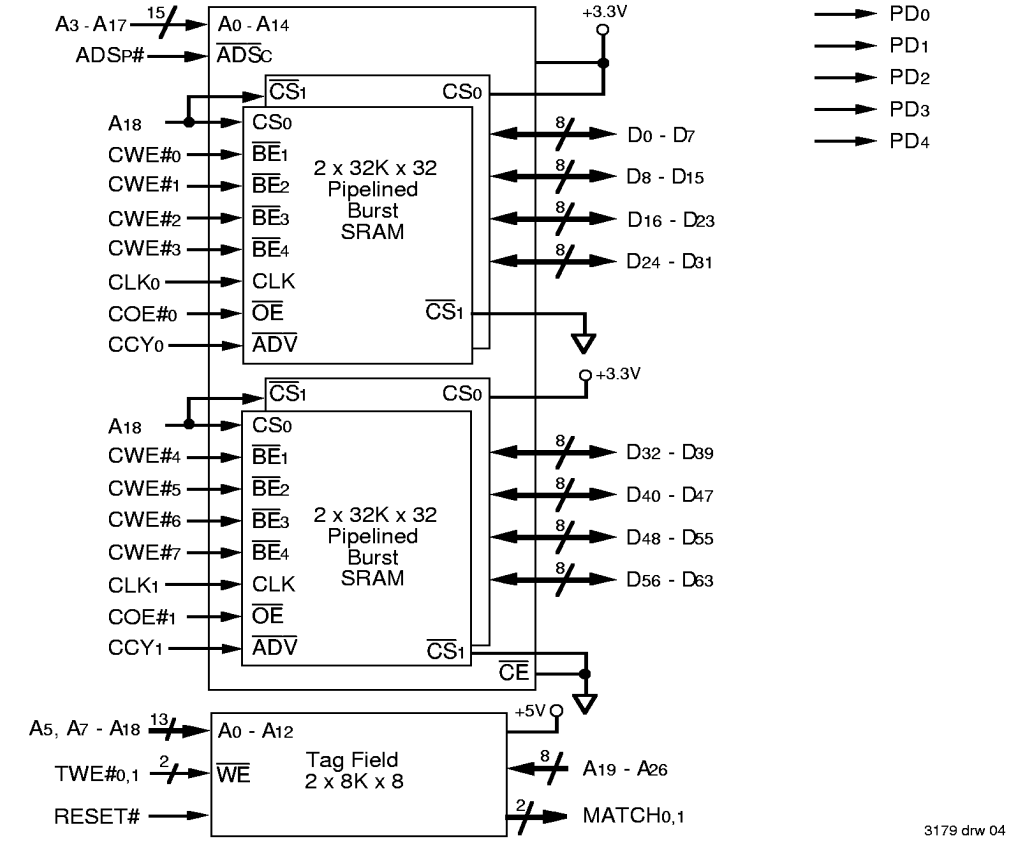
IDT7MPV6244 - 512KB PIPELINED BURST VERSION



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PIN CONFIGURATION[1,2]

GND	81	1	GND
A_{26}	82	2	A_{27}
A_{24}	83	3	A_{25}
A_{22}	84	4	A_{23}
A_{20}	85	5	A_{21}
[3] $MATCH_0$	86	6	A_{19}
V_{CC5}	87	7	TWE#1
[3] $MATCH_1$	88	8	TWE#0
CCY_0	89	9	CCX_0
GND	90	10	GND
COE#0	91	11	CWE#4
CWE#5	92	12	CWE#6
CWE#7	93	13	CWE#0
CWE#1	94	14	CWE#2
V_{CC5}	95	15	V_{CC3}
CWE#3	96	16	CCY_1
CCX_1	97	17	NC
COE#1	98	18	NC
GND	99	19	GND
RESET#	100	20	A_3/NC
A_4/NC	101	21	A_7
A_6	102	22	A_5
A_8	103	23	A_{11}
A_{10}	104	24	A_{16}
V_{CC5}	105	25	V_{CC3}
A_{17}	106	26	A_{18}
GND	107	27	GND
A_9	108	28	A_{12}
A_{14}	109	29	A_{13}
A_{15}	110	30	ADSP#/NC
NC	111	31	NC
PD_0	112	32	NC
PD_2	113	33	PD_1
PD_4	114	34	PD_3
GND	115	35	GND
CLK_0	116	36	CLK_1/NC
GND	117	37	GND
D_{63}	118	38	D_{62}
V_{CC5}	119	39	V_{CC3}
D_{61}	120	40	D_{60}
D_{59}	121	41	D_{58}
D_{57}	122	42	D_{56}
GND	123	43	GND
D_{55}	124	44	D_{54}
D_{53}	125	45	D_{52}
D_{51}	126	46	D_{50}
D_{49}	127	47	D_{48}
GND	128	48	GND
D_{47}	129	49	D_{46}
D_{45}	130	50	D_{44}
D_{43}	131	51	D_{42}
V_{CC5}	132	52	V_{CC3}
D_{41}	133	53	D_{40}
D_{39}	134	54	D_{38}
D_{37}	135	55	D_{36}
GND	136	56	GND
D_{35}	137	57	D_{34}
D_{33}	138	58	D_{32}
D_{31}	139	59	D_{30}
V_{CC5}	140	60	V_{CC3}
D_{29}	141	61	D_{28}
D_{27}	142	62	D_{26}
D_{25}	143	63	D_{24}
GND	144	64	GND
D_{23}	145	65	D_{22}
D_{21}	146	66	D_{20}
D_{19}	147	67	D_{18}
V_{CC5}	148	68	V_{CC3}
D_{17}	149	69	D_{16}
D_{15}	150	70	D_{14}
D_{13}	151	71	D_{12}
GND	152	72	GND
D_{11}	153	73	D_{10}
D_9	154	74	D_8
D_7	155	75	D_6
V_{CC5}	156	76	V_{CC3}
D_5	157	77	D_4
D_3	158	78	D_2
D_1	159	79	D_0
GND	160	80	GND

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LOW PROFILE CARD EDGE MODULE
TOP VIEW

NOTES:
1. Pins with two names delimited by a slash are functions for the burst SRAM and asynchronous SRAM module versions respectively.
2. V_{CC3} is connected to the data SRAMs for the IDT7MPV6239/40/41/44; V_{CC5} is connected to the Tag Ram and the address register.
3. MATCH is an open drain output and there must be an external pull-up resistor for proper operation (200Ω recommended)

PIN NAMES[1]

$A_3 – A_{25}$	Address Inputs from CPU
CCY_0, CCY_1	Address Control Inputs from chipset
CCX_0, CCX_1	Address Control Inputs from chipset
$D_0 – D_{63}$	Inputs/Outputs
$CWE_0 – CWE_7$	Byte Write Enable Inputs
COE#0,1	Output Enable Input
TWE#0, TWE#1	Tag Write Enable Input
ADSP#	Address Status Cache Controller Input
$MATCH_{0,1}$	Tag Data/Memory Match
RESET#	Tag Memory Reset
CLK_0, CLK_1	Clock Inputs
$PD_0 – PD_4$	Presence Detects
GND	Ground
V_{CC3}	3.3V Power Supply only
V_{CC5}	5V Power Supply only

NOTE:
1. CLK_0 is used as the address register clock input.

3179 tbl 01

PRESENCE DETECT TABLE

PD4	PD3	PD2	PD1	PD0	Module
NC	NC	NC	NC	NC	No cache present
GND	NC	GND	GND	NC	IDT7MPV6239
GND	NC	GND	NC	NC	IDT7MPV6240
GND	GND	NC	GND	GND	IDT7MPV6241
GND	GND	NC	NC	GND	IDT7MPV6244

3179 tbl 02

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RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC3}	Supply Voltage	3.0	3.3	3.6	V
V_{CC5}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3179 tbl 03
1. V_{IL} = –1.0V for pulse width less than 5ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Power Plane	Ambient Temperature	GND	Vcc
V_{CC3}	0°C to +70°C	0V	3.3V ± 10%
V_{CC5}	0°C to +70°C	0V	5.0V ± 5%

3179 tbl 04

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
V_{TERM} for V_{CC3}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 3179 tbl 06
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	7MPV6239/40		
			Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	5	µA
I_{IL}	Input Low Current (CLK, A_{18} on 7MPV6240)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	-1.8	mA
I_{IH}	Input High Current (CLK, A_{18} on 7MPV6240)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output HighVoltage	I_{OH}= –4mA, V_{CC} = Min.	2.4	—	V
I_{CC3}	Operating Power (3.3V) Supply Current	V_{CC} = Max., $\overline{CE} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	1900	mA
I_{CC5}	Operating Power (5V) Supply Current	V_{CC} = Max., $\overline{CE} \le V_{IL}$, f = f_{MAX}, Outputs Open	—	460	mA

3179 tbl 07

CAPACITANCE(1, 2)

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	7MPV6239/40	Unit
C_{IN1}	Input Capacitance (A_{5-18})	V_{IN} = 0V	15/25	pF
C_{IN2}	Input Capacitance (A_{3-4}, $\overline{CE}$, $\overline{OE}$, Ctrl)	V_{IN} = 0V	25	pF
C_{IN3}	Input Capacitance ($\overline{WE}$, CLK)	V_{IN} = 0V	15/20	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	12/20	pF

NOTES: 3179 tbl 05
1. These parameters are guaranteed by design but not tested.

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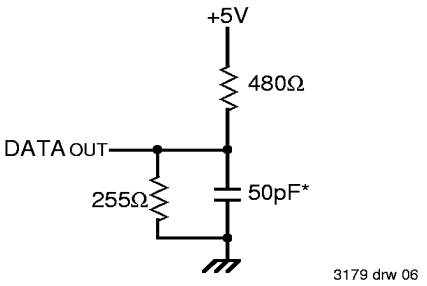
AC TEST CONDITIONS – 5V POWER SUPPLY

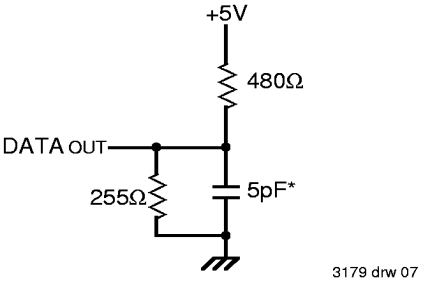
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3179 tbl 08



*including scope and jig capacitances

Figure 1. Output Load



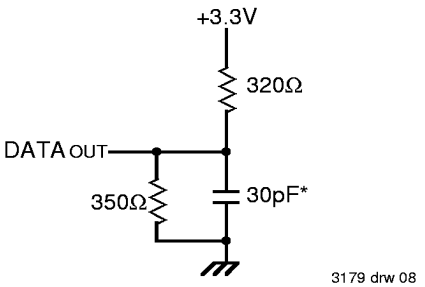
*including scope and jig capacitances

Figure 2. Output Load (for tOHZ, tCHZ, tOLZ and tCLZ)

AC TEST CONDITIONS – 3.3V POWER SUPPLY

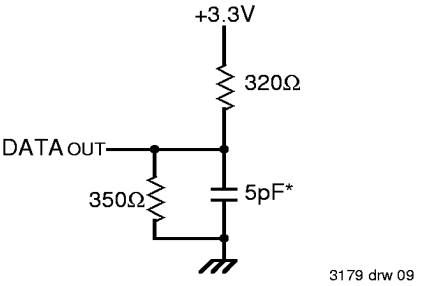
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 3 and 4

3179 tbl 09



*including scope and jig capacitances

Figure 3. Output Load



*including scope and jig capacitances

Figure 4. Output Load (for tOHZ, tCHZ, tOLZ and tCLZ)

SRAM ACCESS TIMES

Bus Speed	Async	Burst(1)	Tag	Performance(2)
66MHz	15ns	—	15ns(3)	3-2-2-2/4-2-2-2
66MHz	—	8.5ns	15ns	3-1-1-1/3-1-1-1
50MHz	20ns	—	15ns(3)	3-2-2-2/4-2-2-2

3179 tbl 10

NOTES:
1. Burst SRAMs are measured by Clock to Data Out (tCD).
2. Performance is shown for read and write burst cycles respectively.
3. Consult factory regarding faster tag SRAM speeds.

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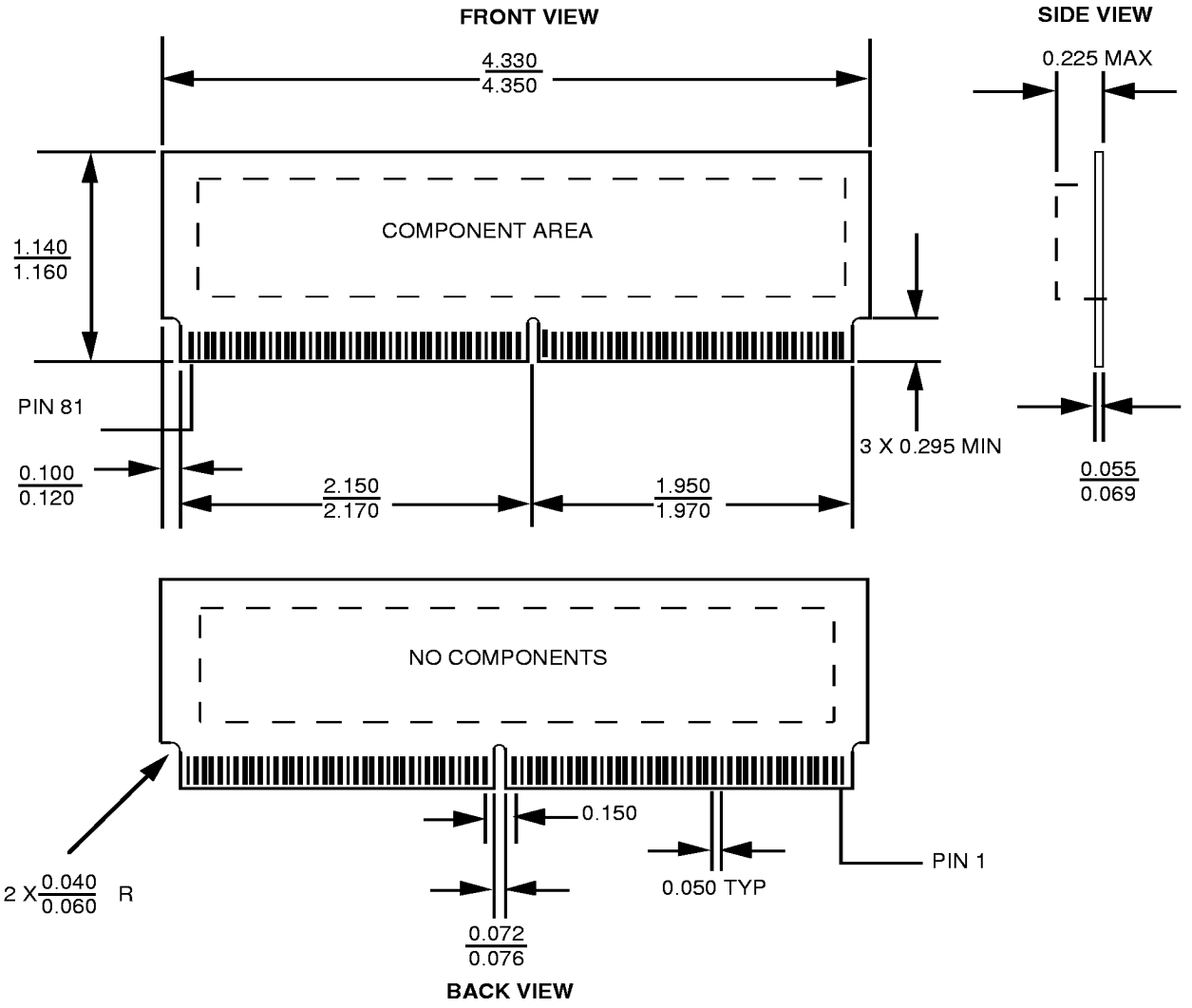
PACKAGE DIMENSIONS
IDT7MPV6239



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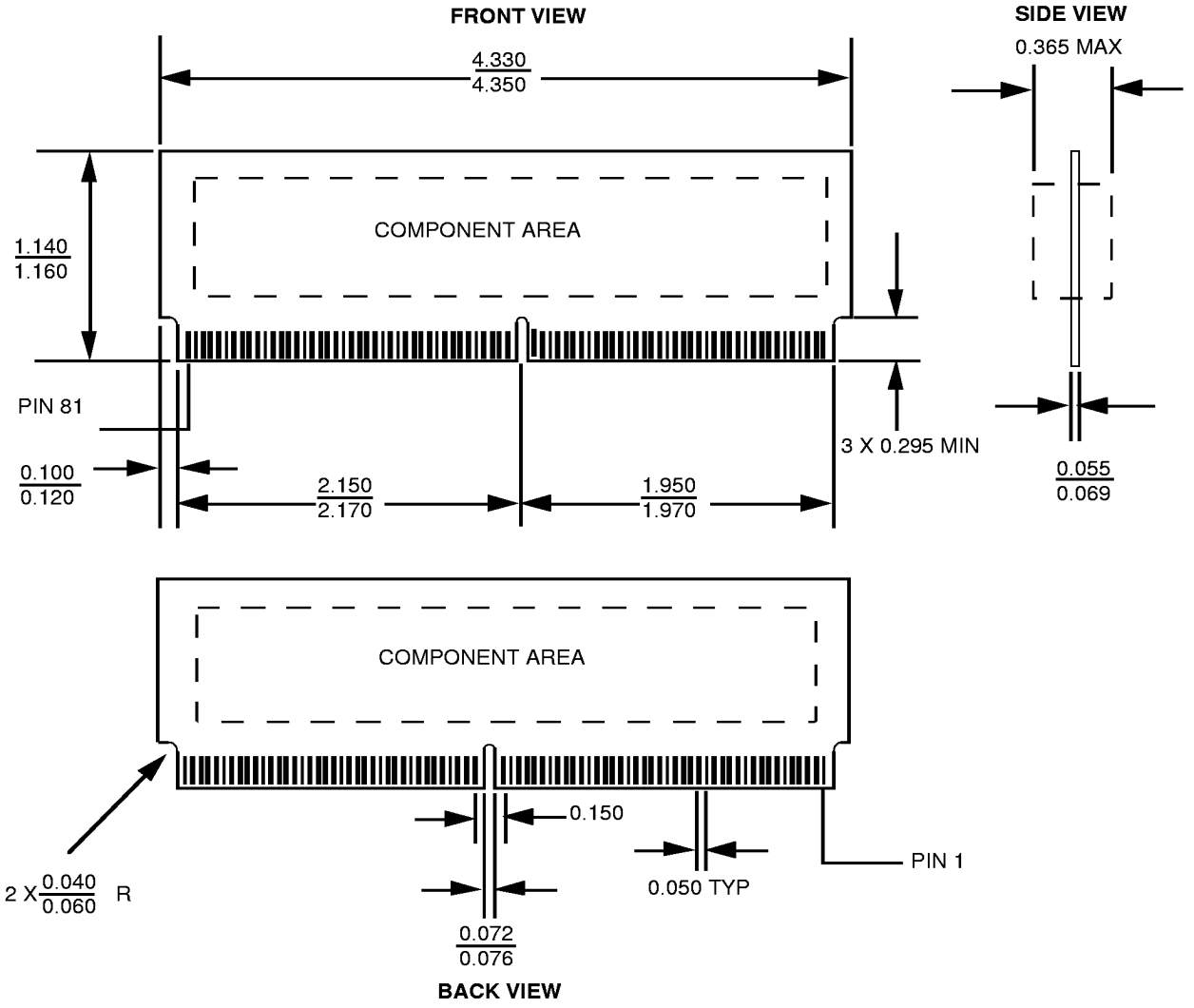
PACKAGE DIMENSIONS

IDT7MPV6240



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PACKAGE DIMENSIONS

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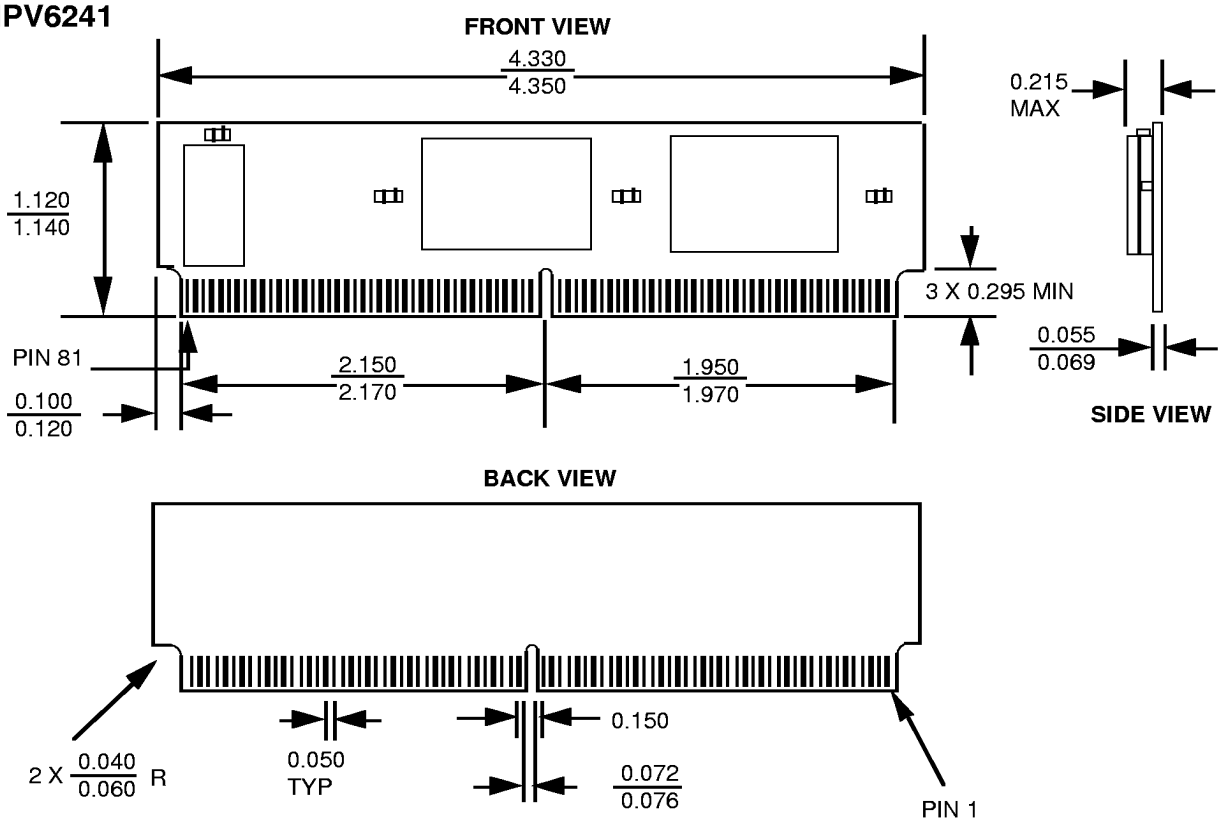

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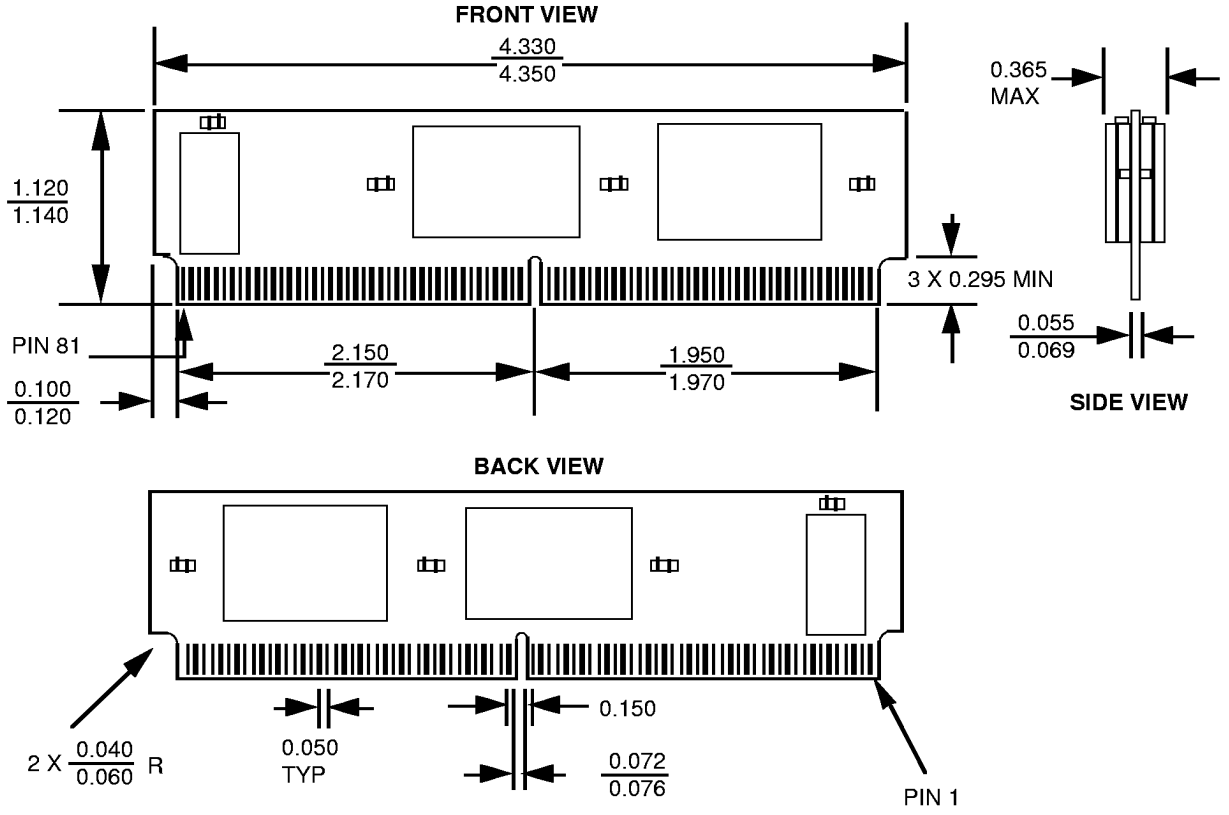

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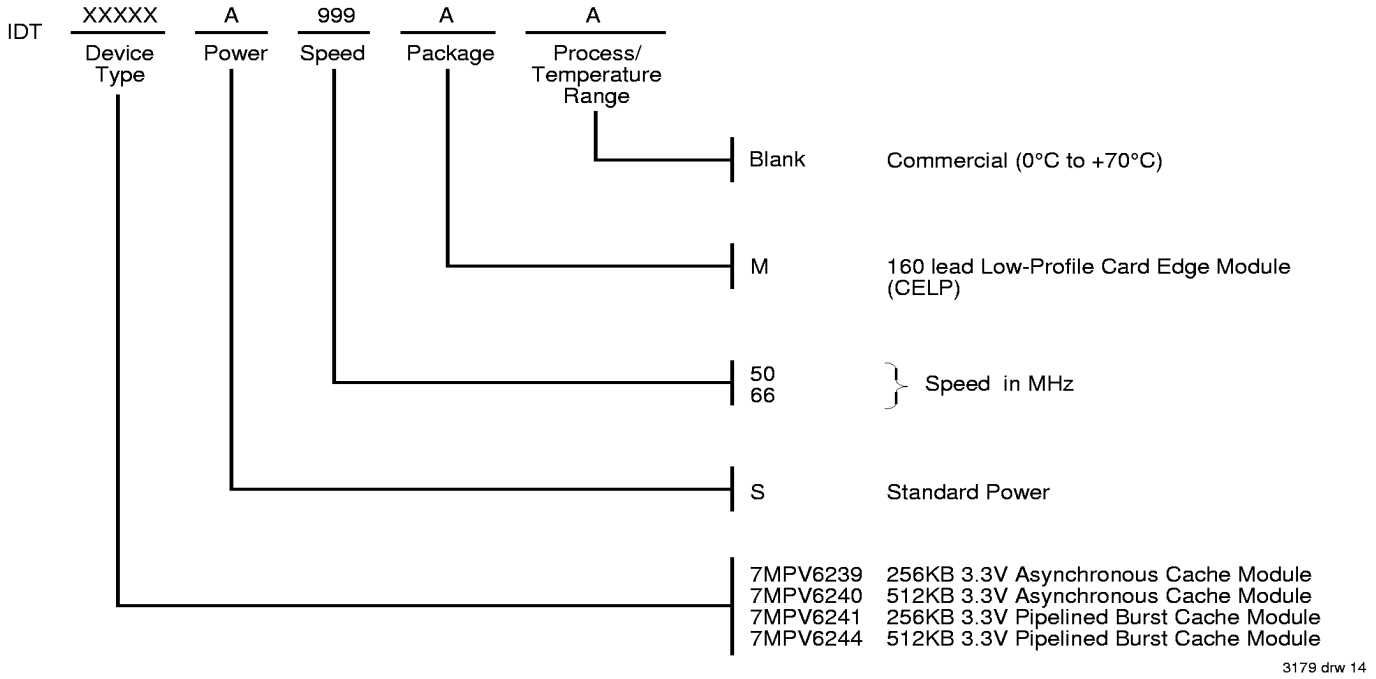

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