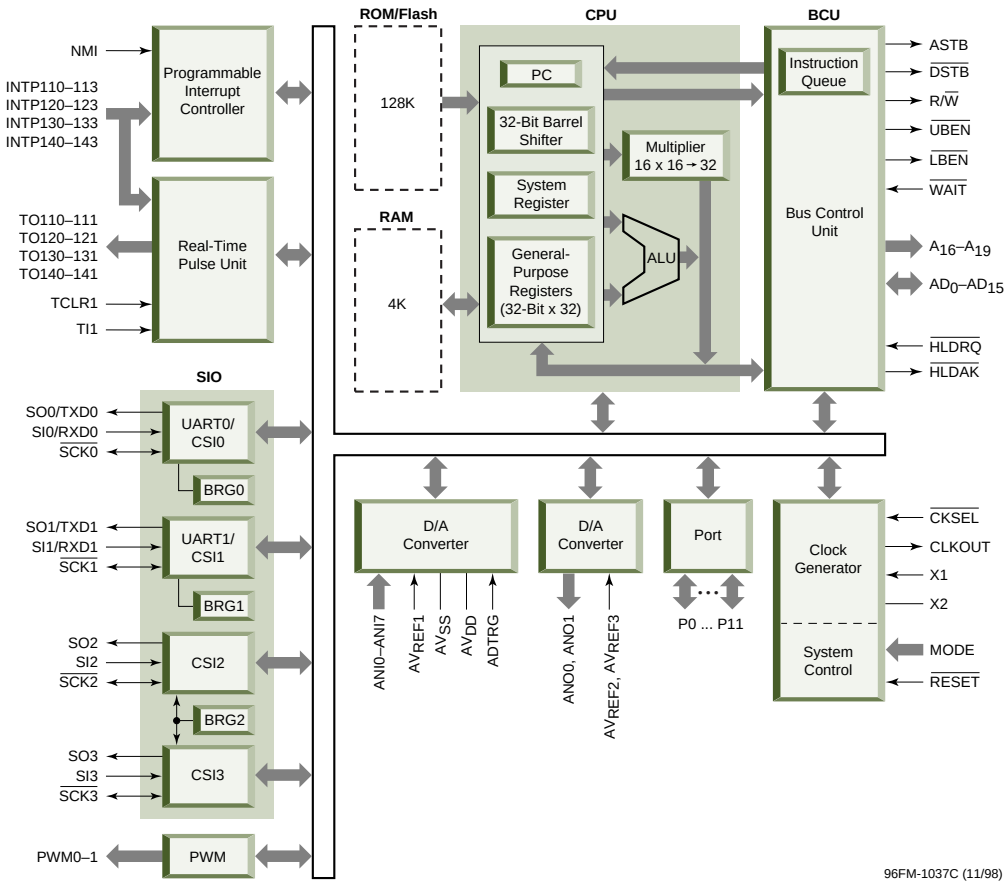
V853™ 32-BIT RISC MICROCONTROLLER

The high-performance, low-power V853 microcontroller features the advanced 32-bit RISC engine of NEC's V850™ family. With 128K of on-chip, single-cycle flash memory, designers have the flexibility to perform in-system programming of devices, decreasing product development upgrade cycles. The V853 microcontroller provides a wide array of on-chip peripherals for embedded applications, including two UARTs, four clocked serial interfaces, three baud rate generators, one 12-bit pulse-width modulator, one 10-bit A/D converter, and one 8-bit D/A converter. Many versions of the V850 core are available as part of NEC's ASIC library. The architecture of the V853 device is highly optimized for fast DSP-like operation and very efficient implementation of C programmability.

SPECIFICATIONS

- Clock frequency: DC to 33 MHz
- Performance
  - 38 Dhrystone MIPS
  - 88 MIPS/W
- Two-cycle MAC instruction
- Single-cycle frequency shift
- 5V operation
- Power consumption: 431 mW at 33 MHz
- 0.5 µm CMOS process technology
- 6.4 mm x 6.5 mm die size
- Package
  - 100-pin plastic QFP
  - 14 mm x 14 mm

BLOCK DIAGRAM



96FM-1037C (11/98)

FEATURE DESCRIPTION

CPU

- Highly integrated microcontroller
  - 32-bit arithmetic logic unit (ALU)
  - Thirty-two general-purpose 32-bit registers
  - 32-bit barrel shifter
- Single-cycle 16 x 16 –> 32-bit hardware multiplier
- Powerful RISC instruction set
  - 74 RISC instructions: 16- and 32-bit
  - Two-cycle MAC function for DSP applications
  - Saturated operation instructions (over/underflow detection)
  - Single-cycle, 32-bit shift instructions
  - Bit manipulation instructions
  - Load and store instructions with 8-/16-/32-bit data
- Fast instruction execution: 30 ns at 33 MHz

MEMORY

- 128K single-cycle internal flash memory or ROM
- 4K single-cycle internal RAM

EXTERNAL BUS INTERFACE

- 1-MB linear address space
- Multiplexed 20-bit address/16-bit data bus
- Multiple bus mastership
- Programmable and external wait functions
- Idle state insertion for slow memory

INTERRUPTS

- 32 maskable interrupts plus NMI
- Eight programmable priority levels on all interrupts and traps
- Specifiable rising and/or falling edge detection
- 32 software traps

PERIPHERALS

- 75 general-purpose, reassignable I/O pins
- Real-time pulse unit
  - Four-channel 16-bit timer/event counter
    - Four 16-bit timers
    - Sixteen 16-bit capture/compare registers
  - One-channel 16-bit interval timer
- Serial interface
  - UART: two channels
  - Clocked serial interface: two to four channels
  - Dedicated baud rate generator: three channels
- Clock generator
  - Internal PLL (5x, 1x)
  - Direct clock input ($^1/_2$x)
- Analog interface
  - Eight-channel A/D converter with 10-bit resolution
  - Two-channel D/A converter with 8-bit resolution
  - Two-channel PWM with 8-/9-/10-/12-bit resolution

OTHER

- Power saving features
  - Halt/idle/stop modes
  - Clock output stop function
  - Fully static operation

ORDERING INFORMATION

PART NUMBER	INTERNAL ROM	PACKAGE
µPD703003GC-25	128K masked ROM	100-pin plastic QFP (fine pitch), 14 mm x 14 mm
µPD703003GC-33	128K masked ROM	100-pin plastic QFP (fine pitch), 14 mm x 14 mm
µPD70F3003GC-25	128K flash memory	100-pin plastic QFP (fine pitch), 14 mm x 14 mm
µPD70F3003GC-33	128K flash memory	100-pin plastic QFP (fine pitch), 14 mm x 14 mm

NEC

For literature, call 1-800-366-9782 7 a.m. to 6 p.m. Pacific time
or fax your request to 1-800-729-9288
or visit our Web site at www.nec.com

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