DUAL 4-INPUT MULTIPLEXER

The HEF4539B is a dual 4-input multiplexer with common select logic. Each multiplexer has four *multiplexer inputs* (I_0 to I_3), *an active LOW enable input* ($\overline{E}$) *and a multiplexer output* (O). When HIGH, $\overline{E}$ forces O of the respective multiplexer LOW, independent of the select inputs (S_0 and S_1) and I_0 to I_3. When $\overline{E}$ is LOW, S_0 and S_1 determine which multiplexer input (I_0 to I_3) on each of the multiplexers is routed to the respective multiplexer output (O).

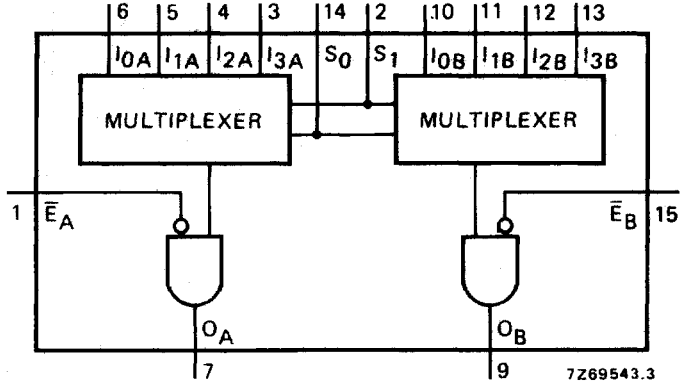

Fig. 1 Functional diagram.

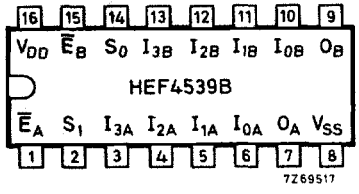

Fig. 2 Pinning diagram.

HEF4539BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4539BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4539BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

I_{0A}, I_{1A}, I_{2A}, I_{3A}	multiplexer inputs
I_{0B}, I_{1B}, I_{2B}, I_{3B}	multiplexer inputs
S_0, S_1	select inputs
$\overline{E}_A$, $\overline{E}_B$	enable inputs (active LOW)
O_A, O_B	multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

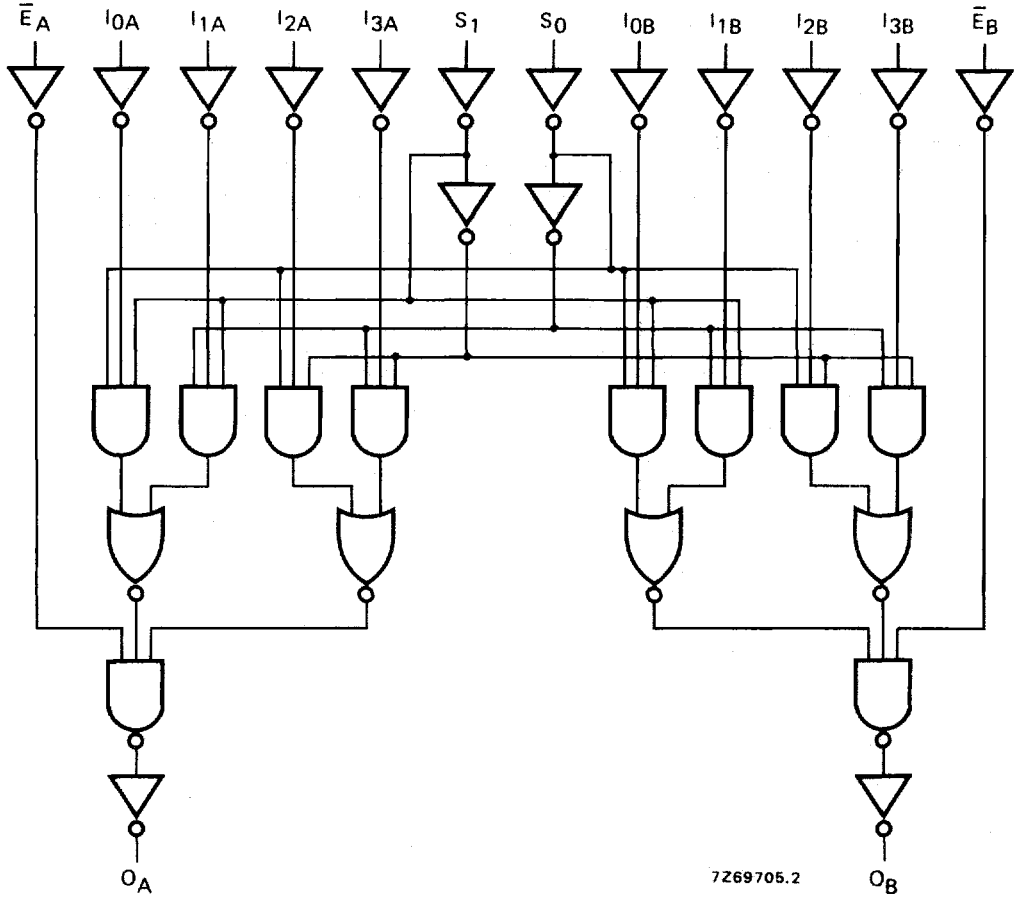

Fig. 3 Logic diagram.

FUNCTION TABLE

inputs			output
S_0	S_1	$\overline{E}_n$	O_n
X	X	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min.	typ.	max.		typical extrapolation formula
Propagation delays							
$I_n \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			120	245	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
$S_n \rightarrow O_n$	5			165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	125	ns	54 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow O_n$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	700 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2900 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	
	15	8100 f_i + $\Sigma(f_o C_L)$ × V_{DD}^2	

APPLICATION INFORMATION

Some examples of applications for the HEF4539B are:

- Data selectors.
- Data multiplexers.