



Integrated Device Technology, Inc.

**HIGH-SPEED BiCMOS
NON-INVERTING
BUFFER TRANSCEIVER**

ADVANCE INFORMATION
IDT54/74FBT245
IDT54/74FBT245A
IDT54/74FBT245C

FEATURES:

- IDT54/74FBT245 equivalent to the 54/74BCT245
- IDT54/74FBT245A 25% faster than the 245
- IDT54/74FBT245C 10% faster than the 245A
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

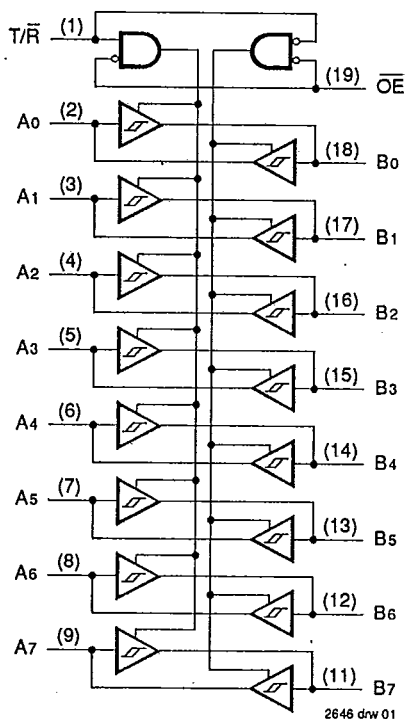
T-52-31

The FBT series of BiCMOS Buffer Transceivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

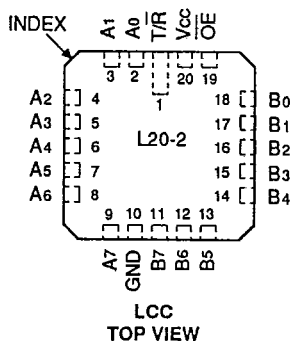
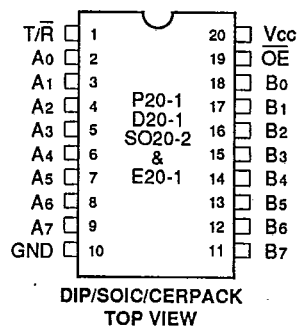
The IDT54/74FBT245 series of 8-bit non-inverting, bidirectional buffers have 3-state outputs and are intended for bus interface applications. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports. Receive (active LOW) enables data from B ports to A ports. The Output Enable (OE) input, when HIGH, disables both A and B ports by placing them in the high impedance state.

The FBT series of bus interface devices are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1990

IDT5474FBT245/A/C
HIGH-SPEED BICMOS NON-INVERTING BUFFER TRANSCEIVER

MILITARY AND COMMERCIAL TEMPERATURE RANGES

PIN DESCRIPTION

Pin Names	Description
\overline{OE}	Output Enable Input (Active LOW)
T/\overline{R}	Transmit/Receive Input
A0 - A7	Side A Inputs or 3-State Outputs
B0 - B7	Side B Inputs or 3-State Outputs

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FUNCTION TABLE⁽¹⁾

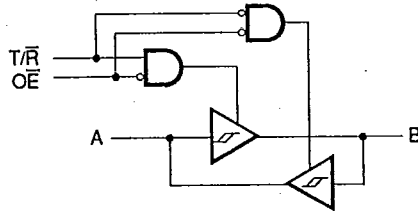
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Inputs		Outputs
\overline{OE}	T/\overline{R}	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

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NOTE:
1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOGIC SYMBOL



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	0.5	0.5	W
IOUT	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.

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CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	6	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

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IDT5474FBT245/A/C

HIGH-SPEED BICMOS NON-INVERTING BUFFER TRANSCEIVER

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

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Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, Vcc = 5.0V ± 10%; Military: TA = -55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I _{IH}	Input HIGH Current	Vcc = Max. Vi = 2.7V	Except I/O Pins	—	—	10	μA
			I/O Pins	—	—	60	
I _{IL}	Input LOW Current	Vcc = Max. Vi = 0.5V	Except I/O Pins	—	—	-10	μA
			I/O Pins	—	—	-60	
I _I	Input HIGH Current	Vcc = Max., Vi = 5.5V		—	—	100	μA
V _{IK}	Clamp Diode Voltage	Vcc = Min., I _N = -18mA		—	-0.7	-1.2	V
I _{OS}	Short Circuit Current	Vcc = Max., Vo = GND ⁽³⁾		-75	—	-225	mA
V _{OH}	Output HIGH Voltage	Vcc = Min. VIN = V _{IH} or V _{IL}	I _{OH} = -12mA MIL.	2.4	3.3	—	V
			I _{OH} = -15mA COM'L.				
			I _{OH} = -18mA MIL.	2.0	3.0	—	V
			I _{OH} = -24mA COM'L.				
V _{OL}	Output LOW Voltage		I _{OL} = 48mA MIL.	—	0.3	0.55	V
			I _{OL} = 64mA COM'L.				
V _H	Input Hysteresis	Vcc = 5V		—	200	—	mV
I _{OFF}	Bus Leakage Current	Vcc = 0V, Vo = 4.5V		—	—	100	μA
I _{CC}	Quiescent Power Supply Current	Vcc = Max. VIN = GND or Vcc		—	0.2	1.5	mA

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

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Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, Outputs Open $OE = GND$, $T/\bar{R} = GND$ or V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$, Outputs Open $f_i = 10\text{MHz}$, 50% Duty Cycle $T/\bar{R} = \overline{OE} = GND$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	—	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	—	5.0	
		$V_{CC} = \text{Max.}$, Outputs Open $f_i = 2.5\text{MHz}$, 50% Duty Cycle $T/\bar{R} = \overline{OE} = GND$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	—	6.5 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	—	14.5 ⁽⁵⁾	

NOTES:

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ C$ ambient, and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_{H} = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamperes and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FBT245		IDT54/74FBT245A				IDT54/74FBT245C				Unit		
			Com'l.		Mil.		Com'l.		Mil.		Com'l.			Mil.	
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.		Min. ⁽²⁾	Max.
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	$C_L = 50pF$ $R_L = 500\Omega$	1.5	7.0	—	—	1.5	4.9	—	—	1.5	4.1	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time \overline{OE} to A or B		1.5	10.9	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OE} to A or B		1.5	9.1	—	—	1.5	5.0	—	—	1.5	4.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time T/\bar{R} to A or B		1.5	10.9	—	—	1.5	6.2	—	—	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/\bar{R} to A or B		1.5	9.1	—	—	1.5	5.0	—	—	1.5	4.8	—	—	ns

NOTES:

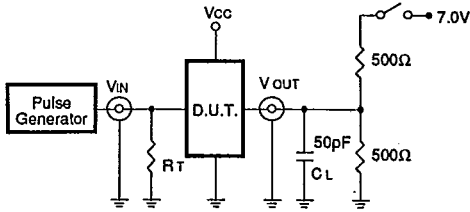
2646 tbl 07

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS

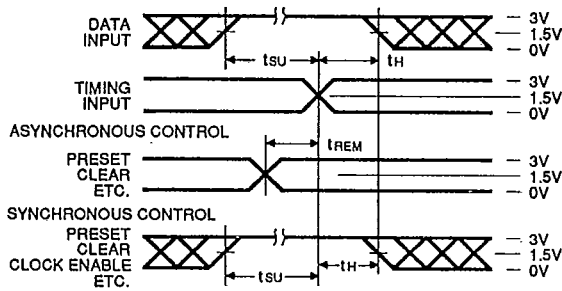


SWITCH POSITION

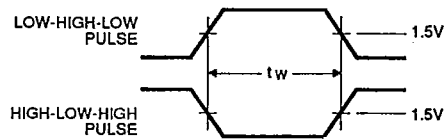
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS: 2846 (b) 03
 CL = Load capacitance: includes jig and probe capacitance.
 RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

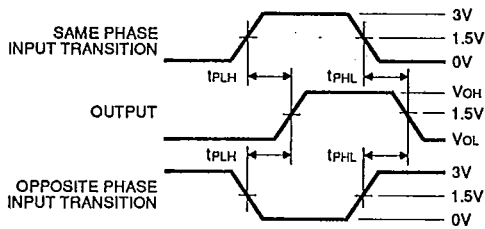
SET-UP, HOLD AND RELEASE TIMES



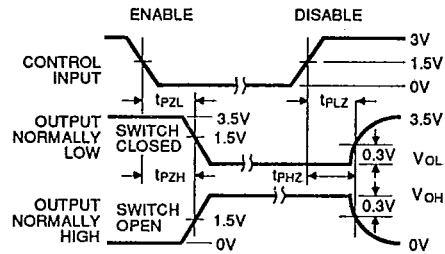
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

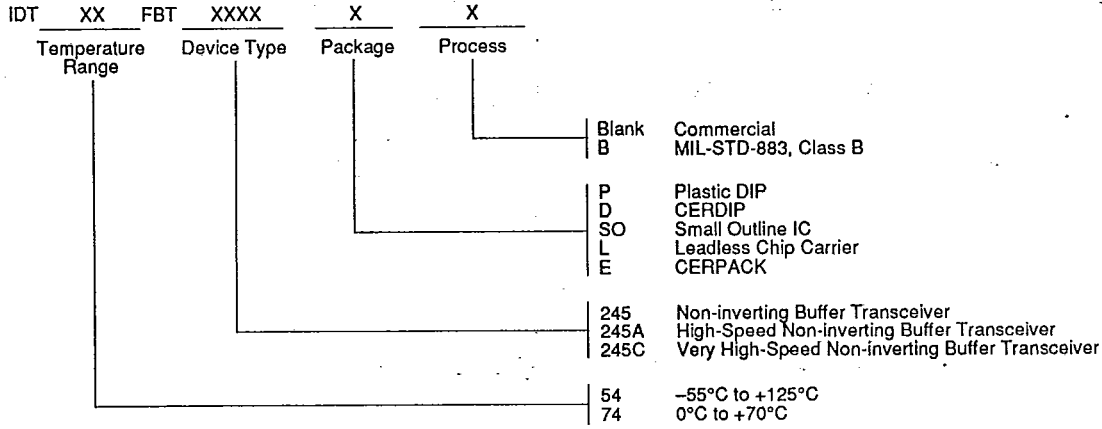


NOTES 2846 drw 05
 1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
 2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; tr ≤ 2.5ns; tr ≤ 2.5ns.



ORDERING INFORMATION

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