PARADIGM®

PDM4M6212
PDM4M6213

COASt Compliant 256KB and 512KB Second Level Cache Modules with 3.3V 8-bit Tag Field for Intel Pentium™ CPUs

Features

- Available in 256KB and 512KB pipelined burst configurations.
- Ideal for use with Intel Pentium™ based systems. Especially those using VLSI's Lynx chipset or the COASt specification from Intel.
- 3.3V power supplies.
- Operates with a wide range of system speeds including 50, 60 and 66 MHz.
- Low cost, low profile cardedge 160-pin module.
- Uses Burndy Computerbus™ connector part number CELP2X80SC3Z48.
- Multiple ground pins and decoupling capacitors for maximum noise immunity.

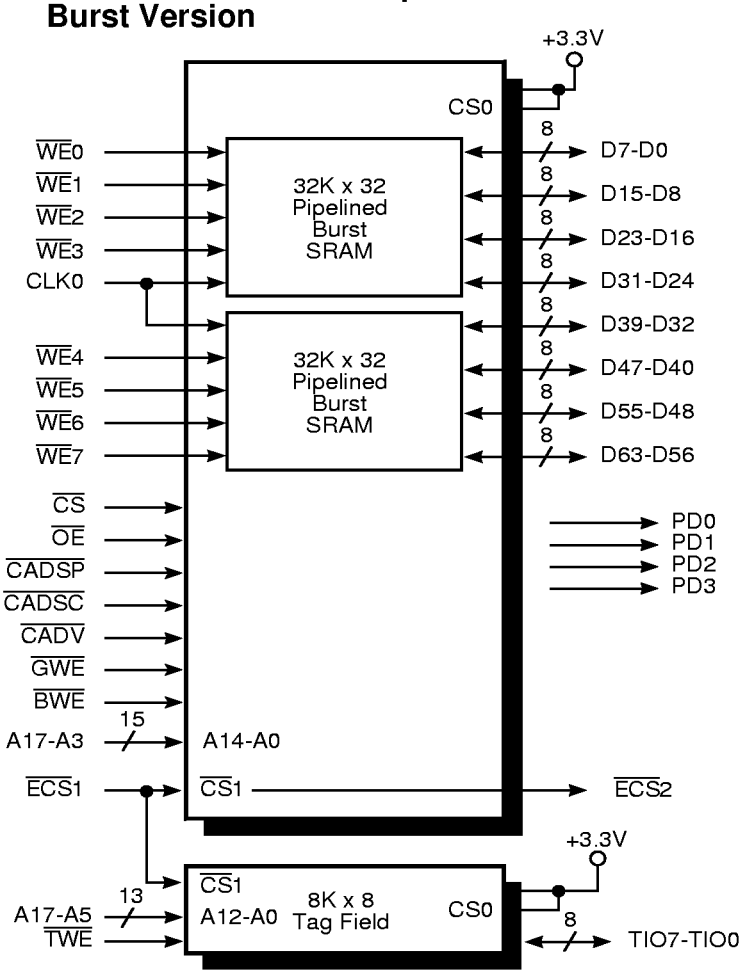
Description

The PDM4M6212 and PDM4M6213 are high-performance CMOS static RAM modules. They are designed for use as second level cache for Intel Pentium™ class CPUs. These modules are compatible with the VLSI Lynx chipset and the COASt specification from Intel. The PDM4M6212 provides 256KB of second level cache by using two (2) 32K x 32 pipelined burst SRAMs. The PDM4M6213 provides 512KB of second level cache by using four (4) 32K x 32 pipelined burst SRAMs.

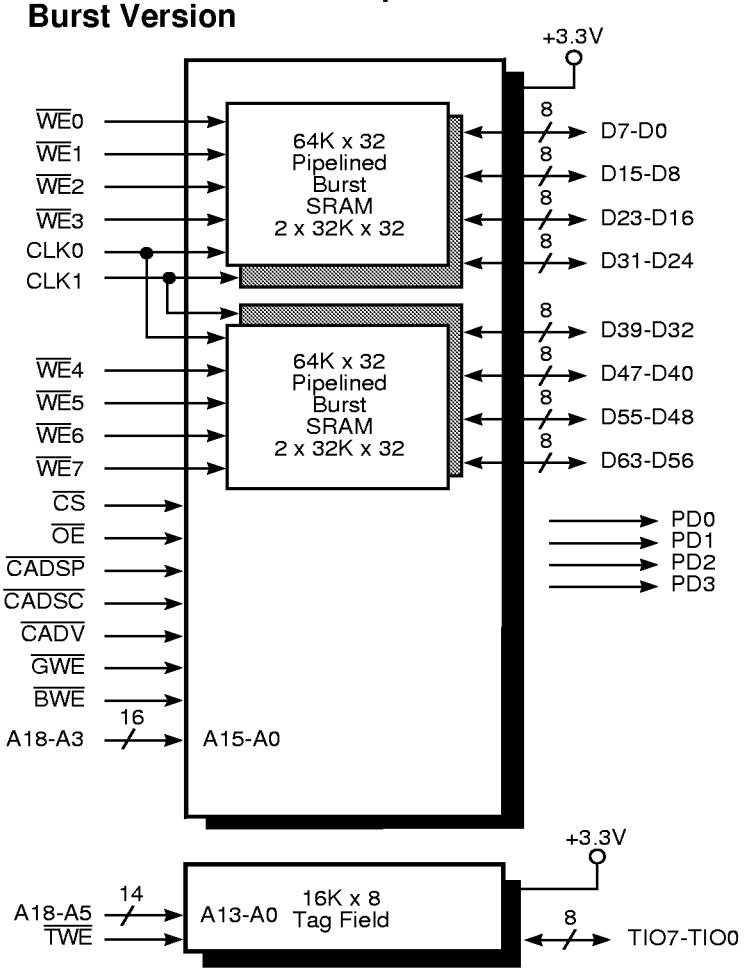
The design of these modules include 3.3V data SRAM and a 3.3V 8-bit tag field as specified in the VLSI specification for cache modules used with the Lynx chipset the COASt specification from Intel. The presence detect pins allow the system to determine the cache configuration.

The PDM4M6212 and PDM4M6213 are all available in a 160-pin DIMM package. This low profile package allows for modules with a maximum height of 1.140", a maximum length of 4.350", and a maximum thickness of 0.310". Equal clock line trace lengths ensure minimum clock skew. Multiple ground pins and decoupling capacitors ensure maximum protection from noise.

Functional Block Diagram PDM4M6212 - 256KB Pipelined Burst Version



Functional Block Diagram PDM4M6213 - 512KB Pipelined Burst Version



Pin Names

Pin	Signal
A18-A5	Address Inputs
A4-A3	Address Inputs
D63-D0	Cache Data Inputs/Outputs
PD3-PD0	Presence Detect Pins
CLK0-CLK1	Clock Inputs
TIO7-TIO0	Tag Inputs/Outputs
$\overline{OE}$	Cache Data Output Enable Input
$\overline{TWE}$	Tag Write Enable Input
$\overline{WE7}$-$\overline{WE0}$	Cache Data Write Enable Input
$\overline{CS}$	Cache Data Chip Enable Input
$\overline{CADSC}$	Cache Address Status Input
$\overline{CADSP}$	Processor Address Status Input
$\overline{CADV}$	Burst Address Advance
$\overline{GWE}$	Global Write Input
$\overline{BWE}$	Byte Write Enable Input
$\overline{ECS1}$	Expansion Chip Select Input (PDM4M6212 Only)
$\overline{ECS2}$	Expansion Chip Select Output (PDM4M6212 Only)
V_{CC3}	3.3V Power Supply
V_{CC5}	5.0V Power Supply

Pin Assignment[1]

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	41	D58	81	Vss	121	D59
2	TIO0	42	D56	82	TIO1	122	D57
3	TIO2	43	Vss	83	TIO7	123	Vss
4	TIO6	44	D54	84	TIO5	124	D55
5	TIO4	45	D52	85	TIO3	125	D53
6	NC[3]	46	D50	86	NC[3]	126	D51
7	Vcc3	47	D48	87	Vcc5	127	D49
8	$\overline{\text{TWE}}$	48	Vss	88	NC[3]	128	Vss
9	$\overline{\text{CADSC}}$/CAA3	49	D46	89	$\overline{\text{CADV}}$	129	D47
10	Vss	50	D44	90	Vss	130	D45
11	$\overline{\text{WE4}}$	51	D42	91	$\overline{\text{OE}}$	131	D43
12	$\overline{\text{WE6}}$	52	Vcc3	92	$\overline{\text{WE5}}$	132	Vcc5
13	$\overline{\text{WE0}}$	53	D40	93	$\overline{\text{WE7}}$	133	D41
14	$\overline{\text{WE2}}$	54	D38	94	$\overline{\text{WE1}}$	134	D39
15	Vcc3	55	D36	95	Vcc5	135	D37
16	$\overline{\text{CCS}}$/CAB4	56	Vss	96	$\overline{\text{WE3}}$	136	Vss
17	$\overline{\text{GWE}}$	57	D34	97	CAB3	137	D35
18	$\overline{\text{BWE}}$	58	D32	98	CALE	138	D33
19	Vss	59	D30	99	Vss	139	D31
20	A3	60	Vcc3	100	NC[1]	140	Vcc5
21	A7	61	D28	101	A4	141	D29
22	A5	62	D26	102	A6	142	D27
23	A11	63	D24	103	A8	143	D25
24	A16	64	Vss	104	A10	144	Vss
25	Vcc3	65	D22	105	Vcc5	145	D23
26	A18	66	D20	106	A17	146	D21
27	Vss	67	D18	107	Vss	147	D19
20	A12	68	Vcc3	108	A9	148	Vcc5
29	A13	69	D16	109	A14	149	D17
30	$\overline{\text{CADSP}}$	70	D14	110	A15	150	D15
31	$\overline{\text{ECS1}}$ ($\overline{\text{CS}}$)	70	D12	111	NC[1]	151	D13
32	$\overline{\text{ECS2}}$	72	Vss	112	PD0	152	Vss
33	PD1	73	D10	113	PD2	153	D11
34	PD3	74	D8	114	NC/BOSEL[2]	154	D9
35	Vss	75	D6	115	Vss	155	D7
36	CLK1	76	Vcc3	116	CLK0	156	Vcc5
37	Vss	77	D4	117	Vss	157	D5
38	D62	78	D2	118	D63	158	D3
39	Vcc3	79	D0	119	Vcc5	159	D1
40	D60	80	Vss	120	D61	160	Vss

NOTES: 1. These pins are reserved for future use.
2. Pin 114 default is a no connect for Intel processor designs. Module may have pin 114 pulled up with a 4.7 ohm resistor.
3. These pins are used as No Connect for PDM4M6202/6203 and PDM4M6212/6213.
They are used as additional tag bits for PDM4M6222/6223 and PDM4M6224/6225.

Presence Detection Code

Part No.	Description	PD3	PD2	PD1	PD0
	No Cache Present	NC	NC	NC	NC
PDM4M6212	256KB Pipelined Burst	NC	V_{SS}	NC	NC
PDM4M6213	512KB Pipelined Burst	V_{SS}	NC	V_{SS}	V_{SS}

SRAM Access Times

Module Speed	Burst[1]	Tag
66 MHz	8 ns	15 ns
60 MHz	10 ns	20 ns
50 MHz	12 ns	20 ns

NOTE: 1. Burst SRAMs are measured by clock data out (t_{CD}).

Absolute Maximum Ratings[1]

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
V_{TERM} for V_{CC3}	Terminal Voltage with Respect to V_{SS}	–0.5 to +4.6	–0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	–10 to +85	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC3}	Supply Voltage	3.0	3.3	3.6	V
V_{CC5}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0.0	V
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Address)	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	20	µA
I_{LI}	Input Leakage Current (Data and Control)	V_{CC} = MAX., V_{IN} = V_{SS} to V_{CC}	—	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4 mA, V_{CC} = Min.	2.4	—	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V

NOTE: 1. V_{IL} (Min.) = –3.0V for pulse widths less than 20 ns.

Power Supply Characteristics (V_{CC5} = 5.0V ± 5%, V_{CC3} = 3.3V ± 10%)

Symbol	Parameter	Max.	Unit
I_{CC3}	Operating Current 3.3V $\overline{CS} \le V_{IL}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	900	mA
I_{CC5}	Operating Current 5V $\overline{CS} \le V_{IL}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	180	mA
I_{SB3}	Full Standby Current $\overline{CE} \ge V_{IH}$ f = f_{MAX}, Outputs Open	—	mA

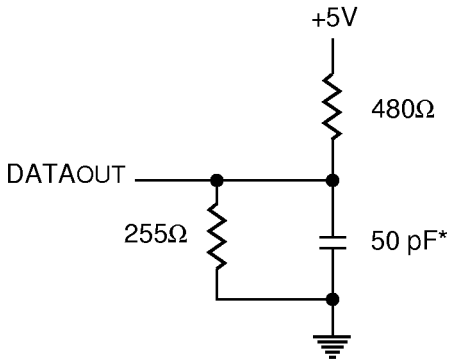
Capacitance[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max	Unit
C_{IN1}	Input Capacitance, V_{IN} = 0V (Address)	15	pF
C_{IN2}	Input Capacitance, V_{IN} = 0V (CA3-CA4)	25	pF
C_{IN3}	Input Capacitance, V_{IN} = 0V ($\overline{OE}$)	45	pF
C_{IN4}	Input Capacitance, V_{IN} = 0V ($\overline{WE}$, $\overline{TWE}$)	8	pF
CI/O	I/O Capacitance, V_{OUT} = 0V	10	pF

NOTES: 1. This parameter is determined by device characteristics but is not production tested.

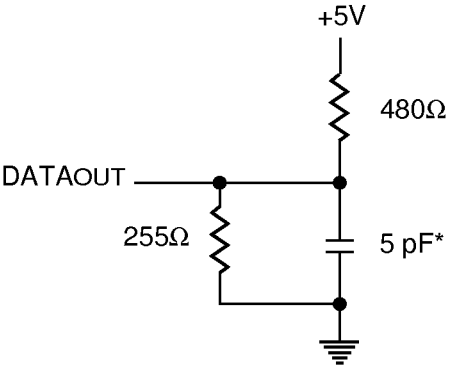
AC Test Conditions

Input Pulse Levels	Vss to 5.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



* Including scope and jig capacitances

Figure 1. Output Load

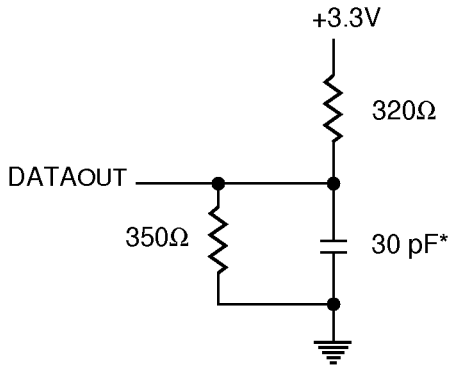


* Including scope and jig capacitances

Figure 2. Output Load
(for tOHZ, tCHZ, tOLZ, and tCLZ)

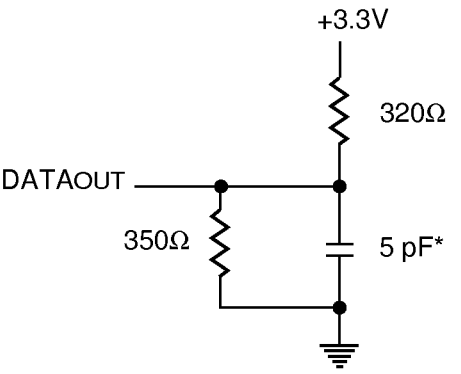
AC Test Conditions

Input Pulse Levels	Vss to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 3 and 4



* Including scope and jig capacitances

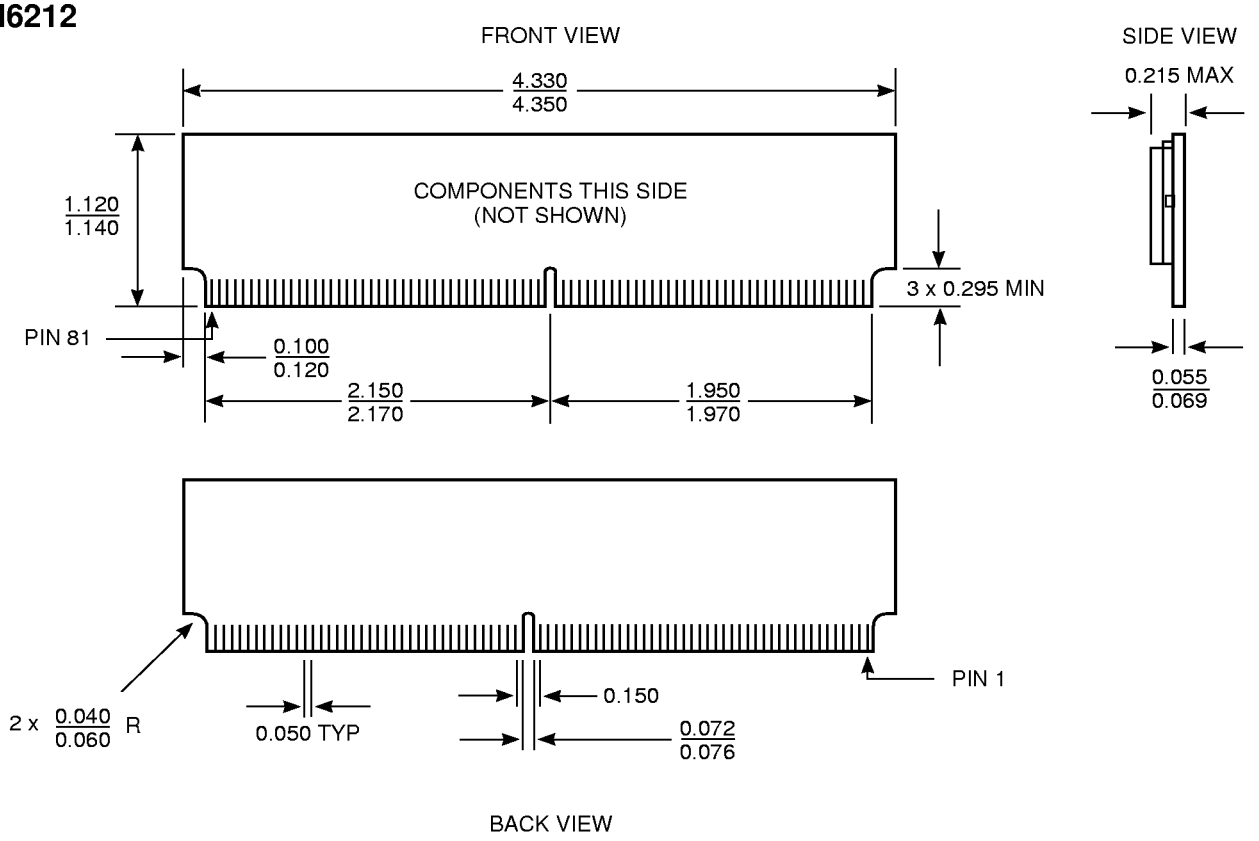
Figure 3. Output Load



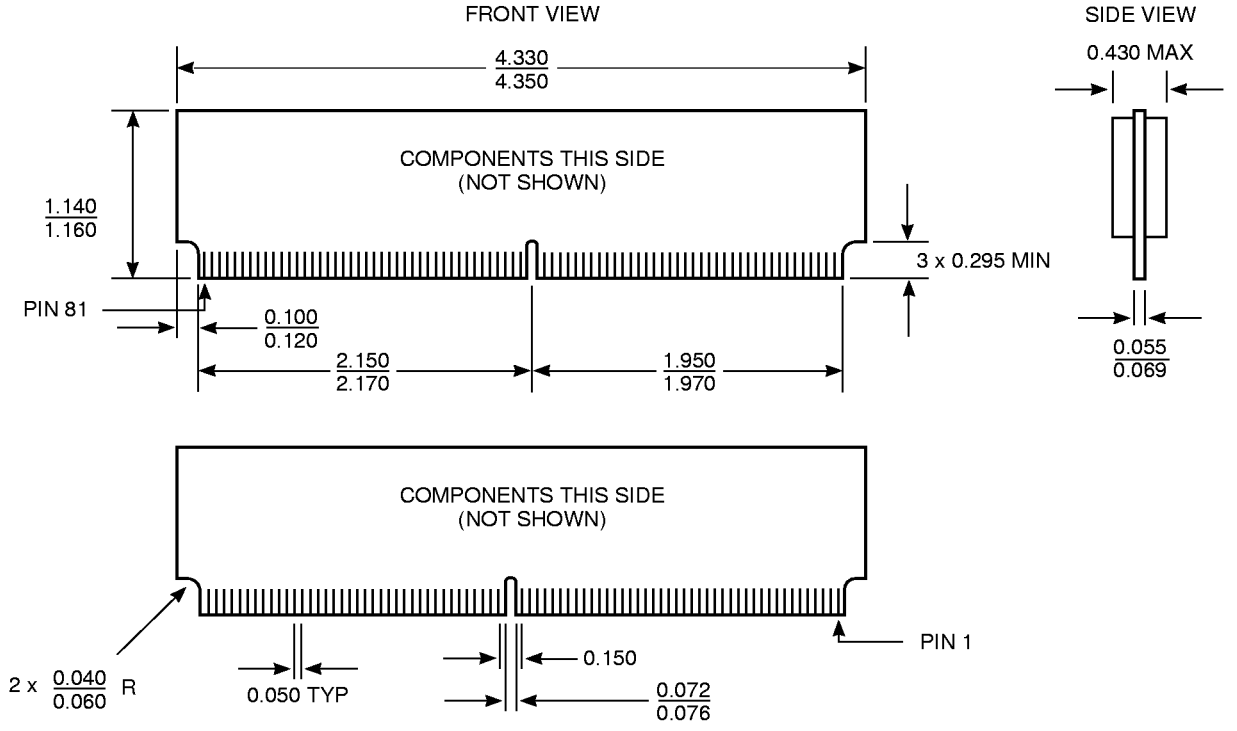
* Including scope and jig capacitances

Figure 4. Output Load
(for tOHZ, tCHZ, tOLZ, and tCLZ)

Package Dimensions
PDM4M6212



Package Dimensions
PDM4M6213



Ordering Information