Features

- 2 independent high gain op amps
- On-chip window comparator
- On-chip voltage reference (3.6V)
- Internal 16kHz oscillator
- Low battery detector
- Built-in noise rejection circuit for PIR sensor applications
- 16-pin DIP package

General Description

PT8A260P is a mixed-signal base chip consists of 2 high gain front end amplifier, window comparators, voltage reference, oscillator and low battery detector. All the analog modules are well proven and fully characterized. With another external digital ASIC such as FPGA, customers can verify their mixed-signal system faster and with minimum risk.

PT8A260P is packaged in 16-pin PDIP. The outputs from op amps, comparator, voltage reference, oscillator, noise rejection circuit and low battery detector are provided.

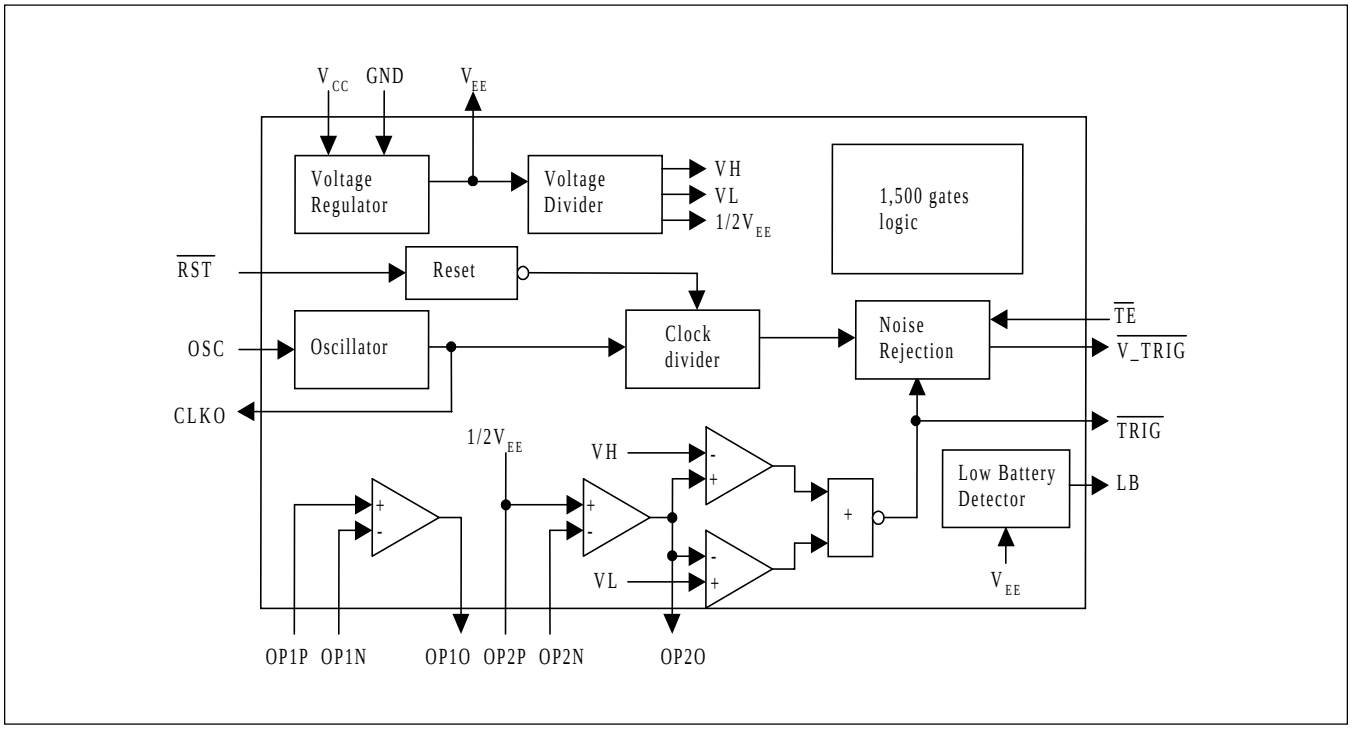
1,500 gates of digital gate are also available inside PT8A260P. Once customers verify their mixed-mode application/system, a single chip solution can be integrated by PTI's factory within 8 weeks after sign off.

Applications

- PIR sensor controller
- Special sensor control
- Mixed-signal ASIC with analog front end

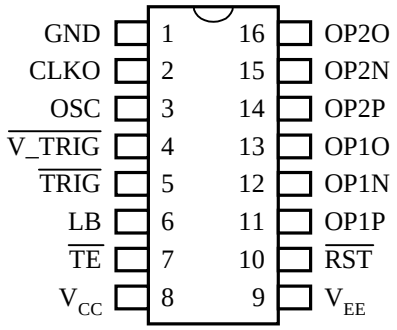
Block Diagram

Figure 1



Pin Assignment

Figure 2



Top view

Pin Description

Table 1

Pin	Name	Type	Description
1	GND	Ground	Ground
2	CLKO	O	Output from oscillator
3	OSC	I	Input of oscillator, external resistor or capacitor changeable, resistor pull down, capacitor pull up, 16kHz for normal application
4	$\overline{\text{V\_TRIG}}$	O	Output from noise rejection circuit (active low)
5	$\overline{\text{TRIG}}$	O	Output from window comparator (active low)
6	LB	O	Output from low battery detector (active high)
7	$\overline{\text{TE}}$	I	Input to enable noise rejection circuit to trigger (active low)
8	V_{CC}	Power	Power supply
9	V_{EE}	O	Internal voltage regulator output, 3.6V with respect to ground. Connected to the drain of PIR sensor
10	$\overline{\text{RST}}$	I	Chip reset input, active low
11	OP1P	I	Non-inverted input of first operational amplifier, connected directly to source of PIR sensor
12	OP1N	I	Inverted input of first operational amplifier
13	OP1O	O	Output of first operational amplifier
14	OP2P	I	Non-inverted input of second operational amplifier.
15	OP2N	I	Inverted input of second operational amplifier
16	OP2O	O	Output of second operational amplifier

Notes

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