

# TUA 6039-2, TUA 6039, TUA 6037

3 Band Digital / Hybrid Tuner IC with  
integrated IF AGC amplifier

OmniTune™ TUA 6039-2,

OmniTune™ TUA 6039,

OmniTune™ TUA 6037

Communication Solutions



Never stop thinking

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|                          |   |                                 |
|--------------------------|---|---------------------------------|
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| Page                     | Subjects (major changes since last revision)  |                                 |
| all                      | Branding name changed to OmniTune™.<br>OmniTune™ TUA 6039-2 included in data sheet.<br>Formatting of document cross-references updated.                           |                                 |
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| <b>19 - 22</b>           | Average DC voltage corrected for X_TAL_CAP, OSCLOWOUT and OSCLOWIN.   |                                 |
| <b>25</b>                | Functional Block Diagram updated. Functional Block Diagram for TUA 6037 added. Functional Description of PLL block updated. Functional Description added for ADC. |                                 |
| <b>37 - 48</b>           | Tuning voltage leakage current, maximum limit added.<br>Phase Noise Parameter, maximum limit added.<br>Footnotes of <b>Table 7</b> updated                        |                                 |
|                          |   |                                 |
|                          |   |                                 |

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# 1 Product Info

## General Description

The **TUA 6039-2, TUA 6039, TUA 6037** device combines a mixer-oscillator function and an IF AGC amplifier with a digitally programmable phase locked loop (PLL) for use in analog and digital terrestrial applications.

## Features

### General

- Supply voltage 3 to 5.5 Volt
- Narrowband RF AGC detector for internal tuner with
  - 5 programmable take over points
  - 2 programmable time constants
  - RF AGC buffer output
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

### Mixer/Oscillator

- Three band tuner
- Unbalanced highohmic LOW input
- Balanced lowohmic MID input
- Balanced lowohmic HIGH input
- Two pin oscillators for LOW/MID band
- Four pin oscillator for HIGH band

### SAW filter driver and IF-Amplifier

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical SAW filter driver
- Fully balanced IF AGC amplifier

### PLL

- I<sup>2</sup>C bus
- 4 pin-programmable I<sup>2</sup>C addresses
- High voltage VCO tuning output
- 4 PNP ports, 1 NPN port/ADC input<sup>1)</sup>
- Internal LOW/MID/HIGH band switch
- X\_TAL 4 MHz, X\_TAL buffer output
- 6 reference divider ratios
- 4 charge pump currents

### Power management

- Bus controlled power down mode

### Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-C, DVB-T, T-DMB, DMB-TH, DAB, ISDB-T, Open Cable and ATSC tuners.

1) ADC function is only available in TUA 6039-2.

## Ordering Information

| Type       | Ordering Code | Package    |
|------------|---------------|------------|
| TUA 6039-2 | SP000279216   | PG-VQFN-48 |
| TUA 6039   | SP000259230   | PG-VQFN-48 |
| TUA 6037   | SP000274731   | PG-VQFN-48 |

## 2 Product Description

The **TUA 6039-2, TUA 6039, TUA 6037 'OmniTune™ TUA 6039-2, OmniTune™ TUA 6039, OmniTune™ TUA 6037'** device combines a mixer-oscillator block with a digitally programmable phase locked loop (PLL) and a variable gain IF AGC amplifier for use in TV and VCR tuners, set-top-box and mobile applications. Integrated narrow band RF AGC functions with output buffer are provided.

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, a reference voltage and a band switch. The mixer output signal passes a SAW filter driver and an IF AGC amplifier to provide constant output level ready for A/D sampling.

The PLL block with four pin programmable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5, 125, 142.86 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I<sup>2</sup>C bus. A flag is set when the loop is locked. The lock flag can be read by the processor via the I<sup>2</sup>C bus. The device has 5 output ports and a X\_TAL output buffer. One of the ports (P4) can be also used as input for a 5-level A to D converter (only available in TUA 6039-2).

### 2.1 Features

#### 2.1.1 General

- Supply voltage range 3 to 5.5 V
- Narrowband RF AGC detector for internal tuner with
  - 5 programmable take over points
  - 2 programmable time constants
  - RF AGC buffer output
- Low phase noise
- Full ESD protection
- Qualified according to JEDEC for consumer applications

#### 2.1.2 Mixer/Oscillator

- High impedance mixer input (common emitter) for LOW band
- Low impedance mixer input (common base) for MID band
- Low impedance mixer input (common base) for HIGH band
- 2 pin oscillator for LOW band
- 2 pin oscillator for MID band
- 4 pin oscillator for HIGH band

### 2.1.3 SAW Filter Driver

- 4 IF pins to connect a 2 pole bandpass
- Symmetrical IF preamplifier with low output impedance able to drive a compensated SAW filter (500  $\Omega$ /40 pF)

### 2.1.4 IF AGC Amplifier

- Symmetrical variable gain IF output amplifier with low noise, high linearity, high dynamic range.

### 2.1.5 PLL

- 4 pin-programmable I<sup>2</sup>C addresses
- I<sup>2</sup>C bus protocol compatible with 3.3 V and 5 V micro-controllers up to 400 kHz
- High voltage VCO tuning output
- 4 PNP ports
- 1 NPN port/ADC input<sup>1)</sup>
- Power down mode
- Internal LOW/MID/HIGH band switch
- Lock-in flag
- 6 programmable reference divider ratios (24, 28, 32, 64, 80, 128)
- 4 programmable charge pump currents

## 2.2 Application

- The IC is suitable for PAL, NTSC, SECAM, DVB-C, DVB-T, T-DMB, DMB-TH, DAB, ISDB-T, Open Cable and ATSC tuners. The focus is on digital terrestrial.
- The AGC stage makes the tuner AGC independent of the Video-IF AGC.

### 2.2.1 Recommended band limits in MHz

**Table 1 ATSC tuners**

| Band | RF input |        | Oscillator |     |
|------|----------|--------|------------|-----|
|      | min      | max    | min        | max |
| LOW  | 55.25    | 157.25 | 101        | 203 |
| MID  | 163.25   | 451.25 | 209        | 497 |
| HIGH | 457.25   | 861.25 | 503        | 907 |

1) ADC function is only available in TUA 6039-2.

**Table 2 DVB-T and analog tuners**

| Band | RF input |        | Oscillator |        |
|------|----------|--------|------------|--------|
|      | min      | max    | min        | max    |
| LOW  | 48.25    | 154.25 | 87.15      | 193.15 |
| MID  | 161.25   | 439.25 | 200.15     | 478.15 |
| HIGH | 447.25   | 863.25 | 486.15     | 902.15 |

**Table 3 ISDB-T tuners**

| Band | RF input |     | Oscillator |     |
|------|----------|-----|------------|-----|
|      | min      | max | min        | max |
| LOW  | 93       | 167 | 150        | 224 |
| MID  | 173      | 467 | 230        | 524 |
| HIGH | 473      | 767 | 530        | 824 |

*Note: Tuning margin of 3 MHz not included.*

### 3 Functional Description

#### 3.1 Pin Configuration

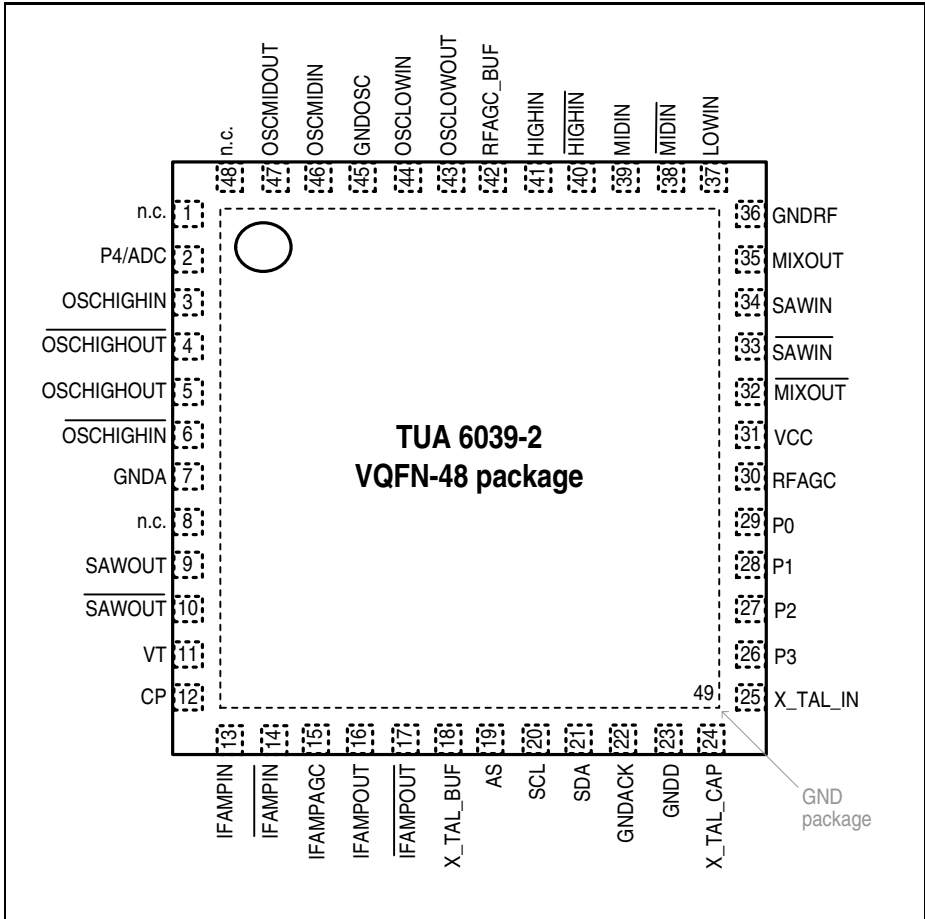
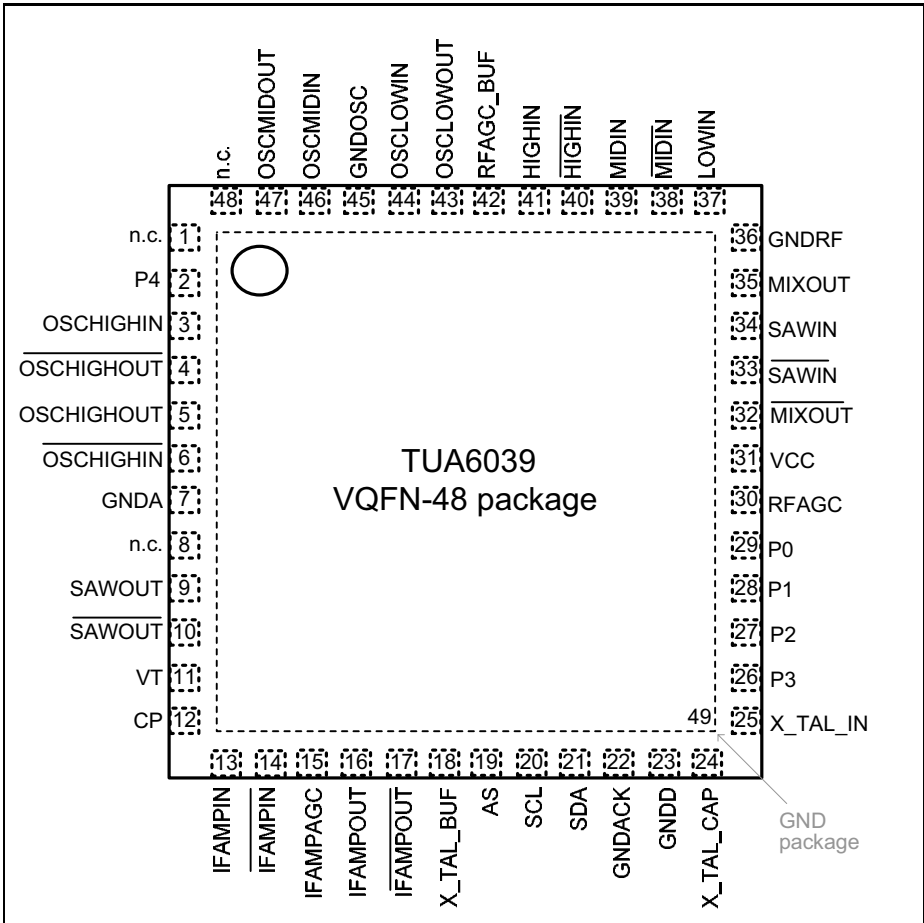
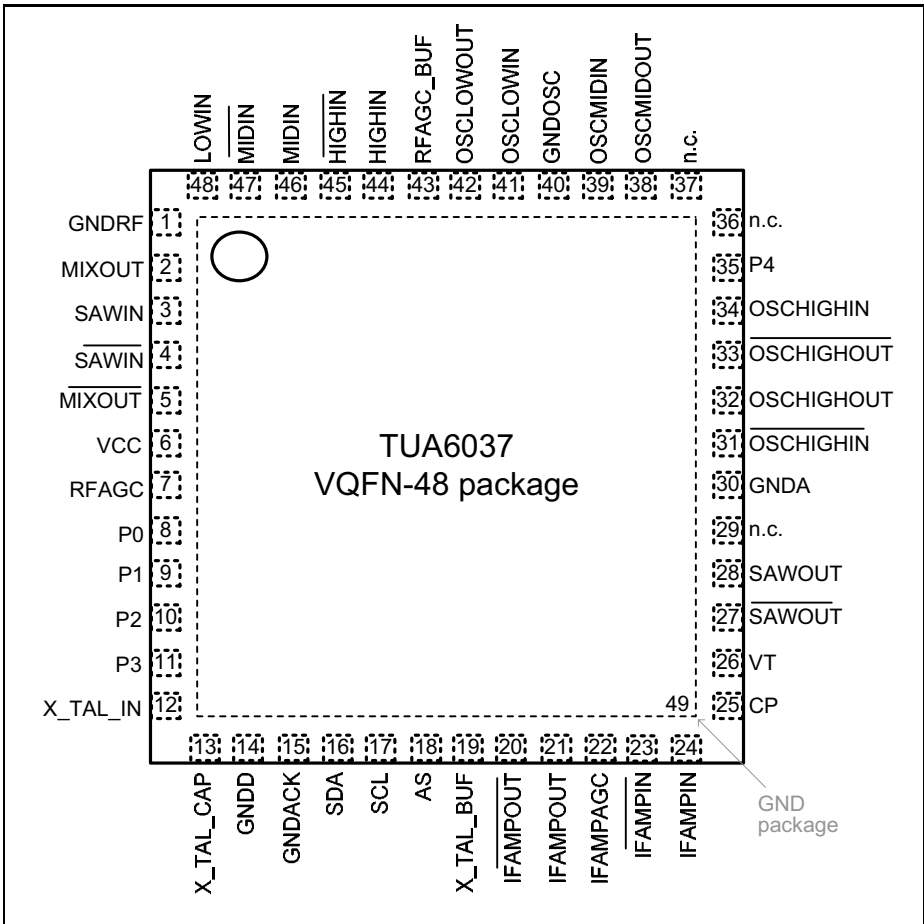


Figure 1 Pin Configuration of TUA 6039-2



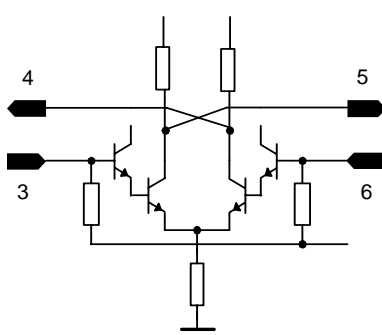
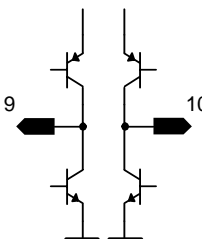
**Figure 2** Pin Configuration of TUA 6039



**Figure 3 Pin Configuration of TUA 6037**

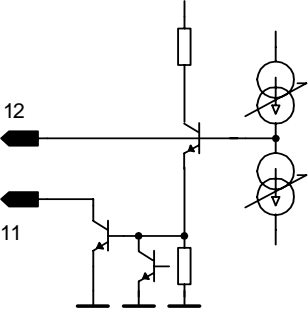
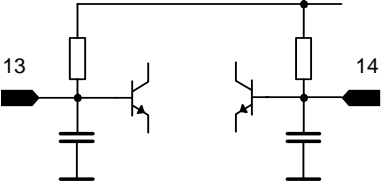
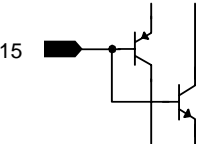
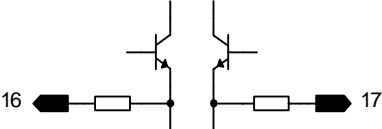
### 3.2 Pin Definition and Functions

**Table 4 Pin Definition and Functions**

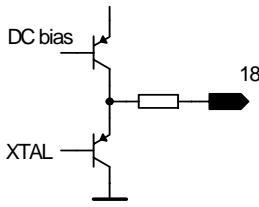
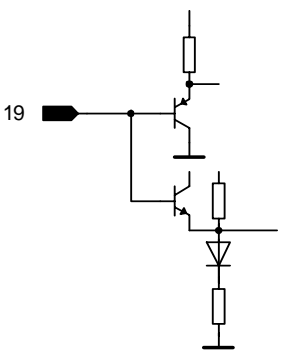
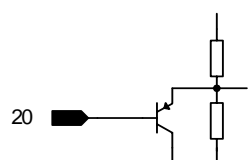
| Pin No. <sup>1)</sup> | Symbol                     | Equivalent I/O Schematic  | Average DC voltage at $V_{CC} = 3.3V$ |                            |                            |
|-----------------------|----------------------------|---|---------------------------------------|----------------------------|----------------------------|
|                       |                            |   | LOW                                   | MID                        | HIGH                       |
| 1 (36)                | n.c.                       |   |                                       |                            |                            |
| 2 <sup>2)</sup>       | P4/ADC input <sup>2)</sup> | P4/ADC input <sup>2)</sup>  | $0 V + V_{CE}$ or $V_{CC}$            | $0 V + V_{CE}$ or $V_{CC}$ | $0 V + V_{CE}$ or $V_{CC}$ |
| 2 (35)                | P4                         | P4  |                                       |                            |                            |
| 3 (34)                | OSCHIGHIN                  |   |                                       |                            | 2.3 V                      |
| 4 (33)                | OSCHIGHOUT                 |   |                                       |                            | 2.25 V                     |
| 5 (32)                | OSCHIGHOUT                 |   |                                       |                            | 2.25 V                     |
| 6 (31)                | OSCHIGHIN                  |   |                                       |                            | 2.3 V                      |
| 7 (30)                | GNDA                       |   | Analog ground                         | 0 V                        | 0 V                        |
| 8 (29)                | n.c.                       |   |                                       |                            |                            |
| 9 (28)                | SAWOUT                     |  | 1.6 V                                 | 1.6 V                      | 1.6 V                      |
| 10 (27)               | SAWOUT                     |   | 1.6 V                                 | 1.6 V                      | 1.6 V                      |



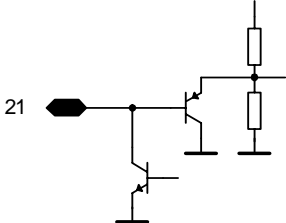
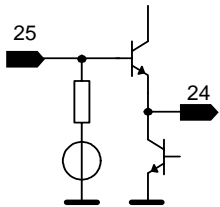
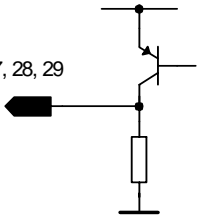
## Functional Description

| Pin No. <sup>1)</sup> | Symbol   | Equivalent I/O Schematic  | Average DC voltage at $V_{CC} = 3.3V$ |       |       |
|-----------------------|----------|---|---------------------------------------|-------|-------|
|                       |          |   | LOW                                   | MID   | HIGH  |
| 11 (26)               | VT       |    | VT                                    | VT    | VT    |
| 12 (25)               | CP       |   | 1.4 V                                 | 1.4 V | 1.4 V |
| 13 (24)               | IFAMPIN  |    | 2.6 V                                 | 2.6 V | 2.6 V |
| 14 (23)               | IFAMPIN  |   | 2.6 V                                 | 2.6 V | 2.6 V |
| 15 (22)               | IFAMPAGC |  | n.a.                                  | n.a.  | n.a.  |
| 16 (21)               | IFAMPOUT |  | 1.6 V                                 | 1.6 V | 1.6 V |
| 17 (20)               | IFAMPOUT |   | 1.6 V                                 | 1.6 V | 1.6 V |

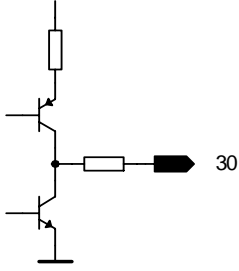
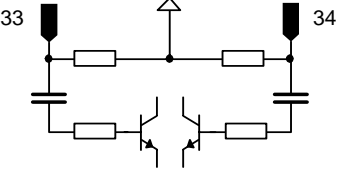
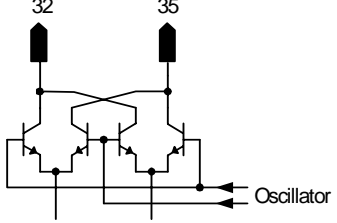
Functional Description

| Pin No. <sup>1)</sup> | Symbol    | Equivalent I/O Schematic  | Average DC voltage at $V_{CC} = 3.3V$ |       |       |
|-----------------------|-----------|---|---------------------------------------|-------|-------|
|                       |           |   | LOW                                   | MID   | HIGH  |
| 18 (19)               | X_TAL_BUF |    | 2.4 V                                 | 2.4 V | 2.4 V |
| 19 (18)               | AS        |    | n.a.                                  | n.a.  | n.a.  |
| 20 (17)               | SCL       |  | n.a.                                  | n.a.  | n.a.  |

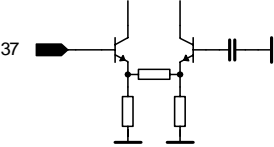
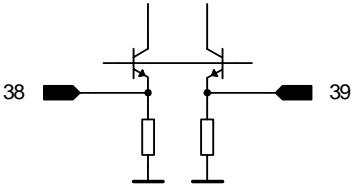
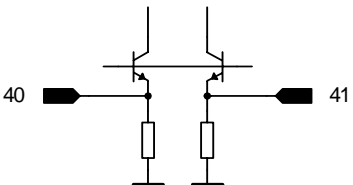
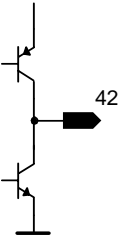
## Functional Description

| Pin No. <sup>1)</sup> | Symbol    | Equivalent I/O Schematic  | Average DC voltage at $V_{CC} = 3.3V$ |                          |                          |
|-----------------------|-----------|---|---------------------------------------|--------------------------|--------------------------|
|                       |           |   | LOW                                   | MID                      | HIGH                     |
| 21 (16)               | SDA       |    | n.a                                   | n.a                      | n.a                      |
| 22 (15)               | GNDACK    | Acknowledge ground  | 0                                     | 0                        | 0                        |
| 23 (14)               | GNDD      | Digital ground  | 0                                     | 0                        | 0                        |
| 24 (13)               | X_TAL_CAP |    | 0.6 V                                 | 0.6 V                    | 0.6 V                    |
| 25 (12)               | X_TAL_IN  |   | 1.2 V                                 | 1.2 V                    | 1.2 V                    |
| 26 (11)               | P3        |  | 0 V or $V_{CC} - V_{CE}$              | 0 V or $V_{CC} - V_{CE}$ | 0 V or $V_{CC} - V_{CE}$ |
| 27 (10)               | P2        |   | 0 V or $V_{CC} - V_{CE}$              | 0 V or $V_{CC} - V_{CE}$ | 0 V or $V_{CC} - V_{CE}$ |
| 28 (9)                | P1        |   | 0 V or $V_{CC} - V_{CE}$              | 0 V or $V_{CC} - V_{CE}$ | 0 V or $V_{CC} - V_{CE}$ |
| 29 (8)                | P0        |   | 0 V or $V_{CC} - V_{CE}$              | 0 V or $V_{CC} - V_{CE}$ | 0 V or $V_{CC} - V_{CE}$ |

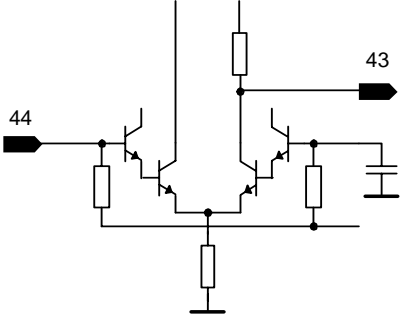
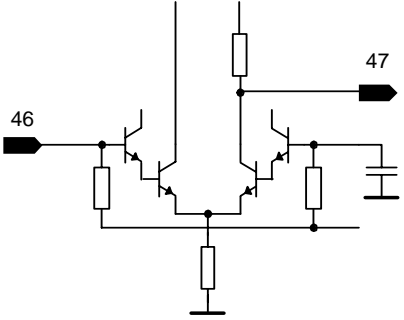
## Functional Description

| Pin No. <sup>1)</sup> | Symbol | Equivalent I/O Schematic  | Average DC voltage at $V_{CC} = 3.3V$ |             |             |
|-----------------------|--------|---|---------------------------------------|-------------|-------------|
|                       |        |   | LOW                                   | MID         | HIGH        |
| 30 (7)                | RFAGC  |    | $V_{RFAGC}$                           | $V_{RFAGC}$ | $V_{RFAGC}$ |
| 31 (6)                | VCC    | supply voltage  | $V_{CC}$                              | $V_{CC}$    | $V_{CC}$    |
| 33 (4)                | SAWIN  |    | $V_{CC}$                              | $V_{CC}$    | $V_{CC}$    |
| 34 (3)                | SAWIN  |   | $V_{CC}$                              | $V_{CC}$    | $V_{CC}$    |
| 32 (5)                | MIXOUT |  | $V_{CC}$                              | $V_{CC}$    | $V_{CC}$    |
| 35 (2)                | MIXOUT |   | $V_{CC}$                              | $V_{CC}$    | $V_{CC}$    |
| 36 (1)                | GNDRF  | RF ground   | 0.0 V                                 | 0.0 V       | 0.0 V       |

## Functional Description

| Pin No. <sup>1)</sup> | Symbol    | Equivalent I/O Schematic  | Average DC voltage at $V_{CC} = 3.3V$ |             |             |
|-----------------------|-----------|---|---------------------------------------|-------------|-------------|
|                       |           |   | LOW                                   | MID         | HIGH        |
| 37 (48)               | LOWIN     |    | 2 V                                   |             |             |
| 38 (47)               | MIDIN     |    |                                       | 1 V         |             |
| 39 (46)               | MIDIN     |   |                                       | 1 V         |             |
| 40 (45)               | HIGHIN    |   |                                       |             | 1 V         |
| 41 (44)               | HIGHIN    |   |                                       |             | 1 V         |
| 42 (43)               | RFAGC_BUF |  | $V_{RFAGC}$                           | $V_{RFAGC}$ | $V_{RFAGC}$ |

## Functional Description

| Pin No. <sup>1)</sup> | Symbol      | Equivalent I/O Schematic   | Average DC voltage at $V_{CC} = 3.3V$ |       |       |
|-----------------------|-------------|--|---------------------------------------|-------|-------|
|                       |             |  | LOW                                   | MID   | HIGH  |
| 43 (42)               | OSLOWOUT    |   | 1.8 V                                 |       |       |
| 44 (41)               | OSLOWIN     |  | 2.3 V                                 |       |       |
| 45 (40)               | GNDOSC      | Oscillator ground  | 0.0 V                                 | 0.0 V | 0.0 V |
| 46 (39)               | OSCMIDIN    |  |                                       | 2.3 V |       |
| 47 (38)               | OSCMIDOUT   |  | 1.8 V                                 |       |       |
| 48 (37)               | n.c.        |  |                                       |       |       |
| 49 (49)               | GND package | Exposed pad ground   | 0.0 V                                 | 0.0 V | 0.0 V |

1) Pin numbering for TUA 6039-2 and TUA 6039 (Pin numbering for TUA 6037 in parentheses).

2) ADC function is only available in TUA 6039-2.

### 3.3 Functional Block Diagram

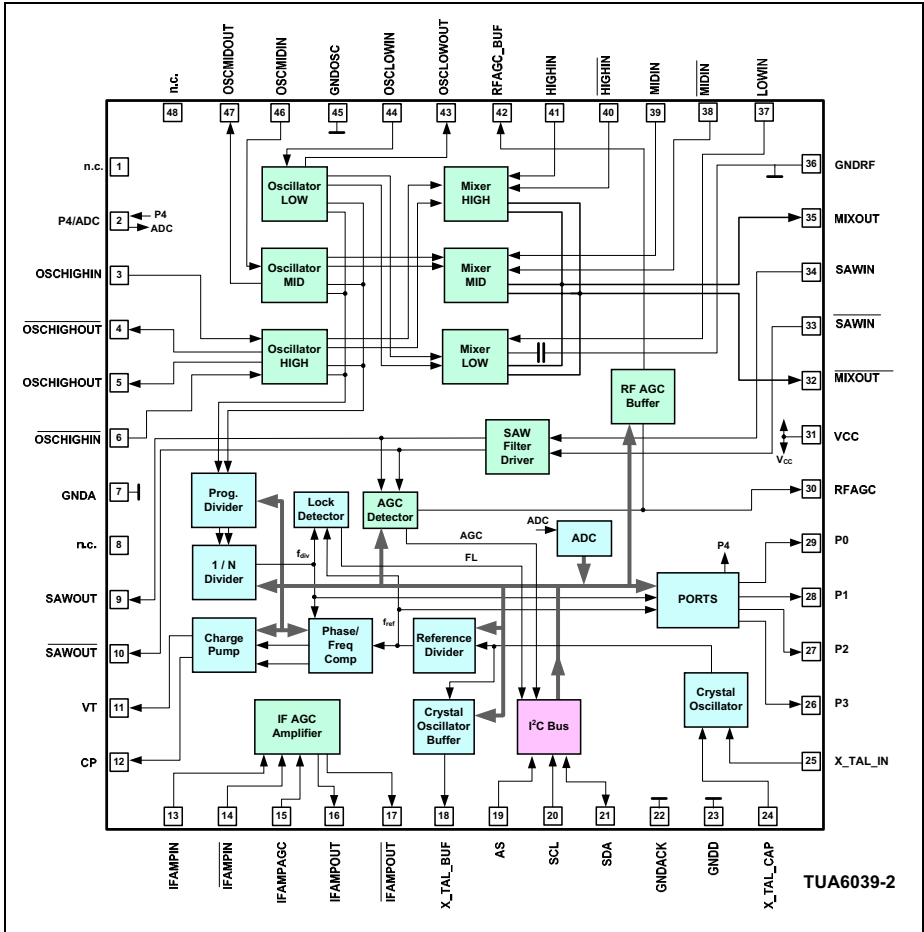


Figure 4 Functional Block Diagram of TUA 6039-2

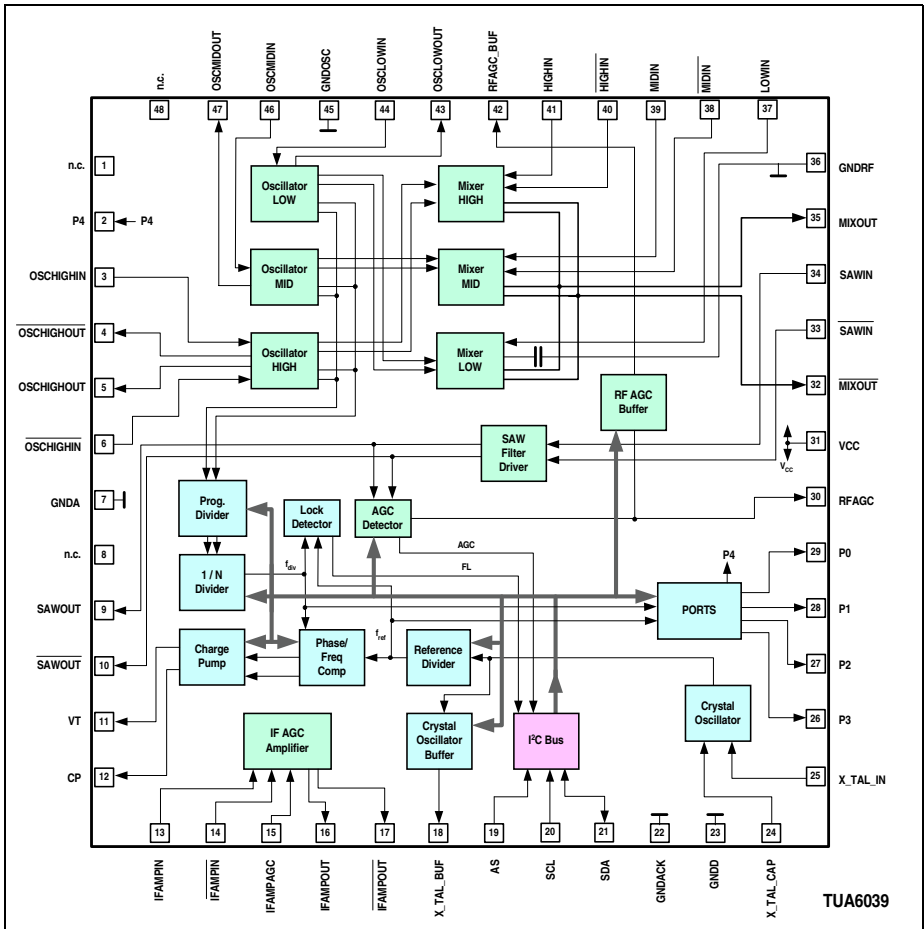


Figure 5 Functional Block Diagram of TUA 6039



Functional Description

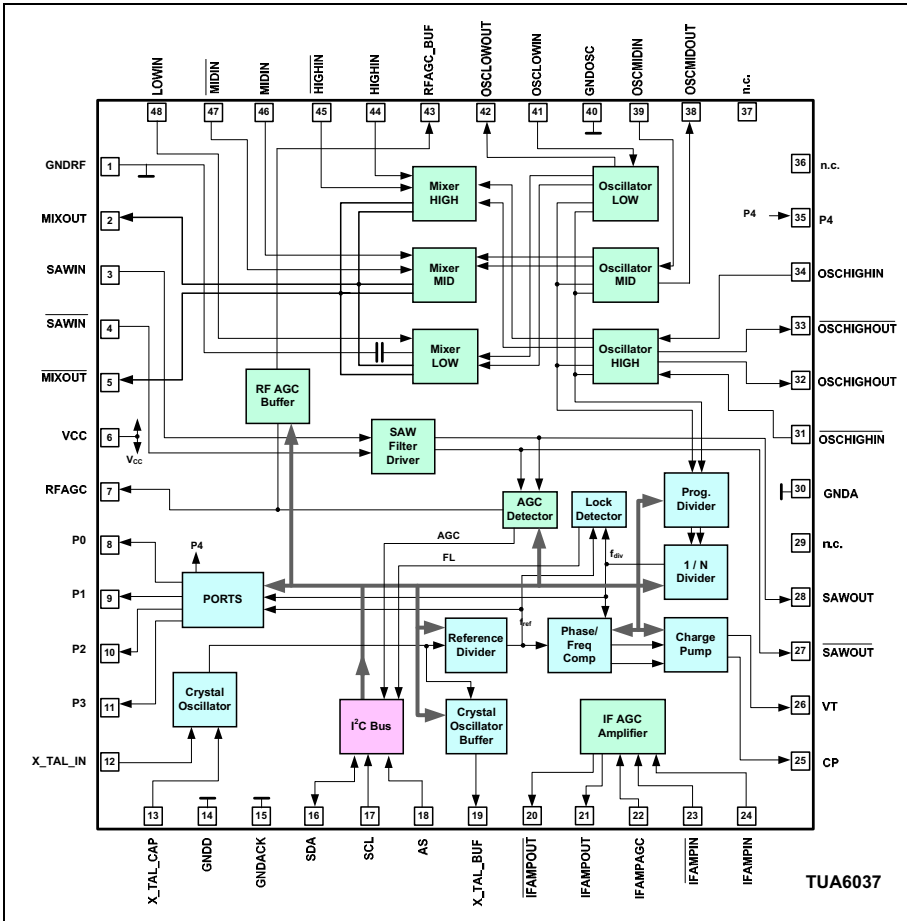


Figure 6 Functional Block Diagram of TUA 6037

### 3.4 Circuit Description

#### 3.4.1 Mixer-Oscillator block with SAW filter driver

The mixer-oscillator block includes three balanced mixers (one mixer with an unbalanced high-impedance input and two mixers with a balanced low-impedance input), two 2-pin asymmetrical oscillators for the LOW and the MID band, one 4-pin symmetrical oscillator for the HIGH band, an SAW filter driver, a reference voltage and a band switch.

Filters between tuner input and IC separate the TV frequency signals into three bands. The band switching in the tuner front-end is done by using three PNP port outputs. In the selected band the signal passes a tuner input stage with a MOSFET amplifier, a double-tuned bandpass filter and is then fed to the mixer input of the IC which has in case of LOW band a high-impedance input and in case of MID or HIGH band a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency. The IF is filtered by means of an IF filter in between the 2 mixer output pins and the 2 input pins of the following SAW filter driver. The SAW filter driver has a low output impedance to drive the SAW filter directly.

#### 3.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio  $N = 256$  through 32767 and is then compared in a digital frequency/phase detector with a reference frequency  $f_{ref} = 31.25, 50, 62.5, 125, 142.86$  or  $166.67$  kHz. This frequency is derived from a low-impedance 4 MHz crystal oscillator (pins XTALIN, XTALCAP) divided by 128, 80, 64, 32, 28 or 24. The reference frequencies will be different with a quartz other than 4 MHz.

The phase detector has two outputs which drive four current sources of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the negative current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at  $V_T$  and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits  $T_2, T_1, T_0 = 0, 1, 0$ . Here it should be noted, however, that the tuning voltage can alter over a long period in the high impedance state as a result of self discharge in the peripheral circuitry.  $V_T$  may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V ( $V_{TH}$ ).

By means of control bits CP, T0, T1 and T2 the pump current can be switched between four values by software. This programmability permits alteration of the control response

**Functional Description**

of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example. Furthermore, in order to obtain best results for phase noise, reference frequency rejection and PLL stability especially in a wideband system like a digital tuner, it is necessary to set the charge pump current to different values depending on the band and frequency used. This is to cope with the variations of the different parameters that set the bandwidth. The selection can be done in the application and requires for each frequency to program not only the divider ratios, but also the band and the best charge pump current.

The software controlled ports P0 to P4 are general purpose open-collector outputs. The test bits T2, T1, T0, OS = 0, 1, 0, 1 switch the test signals  $f_{div} / 2$  (divided input signal) and  $f_{ref}$  (i.e. 4 MHz / 64) to P0 and P1 respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is greater than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P * (K_{VCO} / f_{XTAL}) * (C1 + C2) / (C1 * C2)$$

where  $I_P$  is the charge pump current,  $K_{VCO}$  the VCO gain,  $f_{XTAL}$  the crystal oscillator frequency and  $C_1, C_2$  the capacitances in the loop filter (see [Section 4.2](#)). As the charge pump pulses at i.e. 62.5 kHz (=  $f_{ref}$ ), it takes a maximum of 16  $\mu$ s for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive  $f_{ref}$  periods. Therefore it takes between 128 and 144  $\mu$ s for FL to be set after the loop regains lock.

### 3.4.3 RF AGC

The RF AGC stage detects the level of the SAW filter driver output signal. If the detected level is below the RF AGC take-over point, an external capacity will be charged with the source current of 300 nA or 9  $\mu$ A (release current). If the detected level is above the RF AGC take-over point, the external capacity will be discharged with the sink current of 100  $\mu$ A (attack current). The integrated current generates the AGC voltage for gain control of the tuners input transistors. The RF AGC take-over and the time constant are selectable by the I<sup>2</sup>C bus (see [Table 13](#)).

An integrated RF AGC buffer allows to monitor the AGC voltage without any influence on the tuner gain control.

### 3.4.4 IF AGC amplifier

Coming out of the SAW filter the IF signal is sent through a VGA (Variable Gain Amplifier) which will set the differential IF output signal to the desired level (preferably 1 Vpp). The gain of the VGA is determined by the DC-voltage at pin IFAMPAGC

### 3.4.5 I<sup>2</sup>C-Bus Interface

Data is exchanged between the processor and the PLL via the I<sup>2</sup>C bus. The clock is generated by the processor (input SCL). Pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have a hysteresis and a low-pass characteristic, which enhance the noise immunity of the I<sup>2</sup>C bus.

The data from the processor pass through an I<sup>2</sup>C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are high). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes low, while SCL remains high. Stop condition: SDA goes high while SCL remains high. All further information transfer takes place during SCL = low, and the data is forwarded to the control logic on the positive clock edge.

The table 'Bit Allocation' (see [Table 8](#)) should be referred to for the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to low (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (address select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte. Appropriate setting of the test bits will decide whether the band-switch byte or the auxiliary byte will be transmitted (see [Table 11](#)).

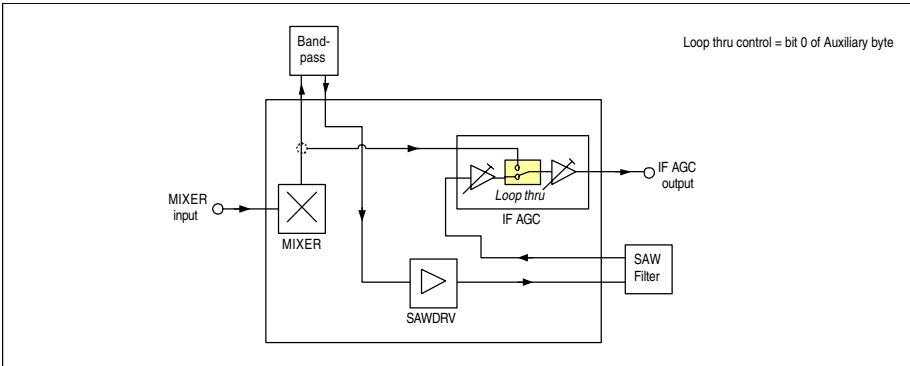
If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists of three bits from the A/D converter, the lock flag and the power-on flag.

Four different chip addresses can be set by an appropriate DC level at pin AS (see [Table 10](#)).

While the supply voltage is applied, a power-on reset circuit prevents the PLL from setting the SDA line to low, which would block the bus. The power-on reset flag POR is set at power-on and if  $V_{CC}$  falls below 2 V. It will be reset at the end of a READ operation.

### 3.4.6 Loop thru

For the tuner prestage alignment a programmable switch is integrated to bypass the bandpass, the SAW filter driver and the SAW filter. If "Loop thru" is active the mixer output signal in front of the external bandpass is fed into the IF AGC amplifier as shown in [Figure 7](#).



**Figure 7 Functional Block Diagram of Loop thru**

This results in a flat frequency response from the mixer input to the IF amplifier output and allows tuner alignment without the need of an external resistor.

### 3.4.7 ADC<sup>1)</sup>

A built-in 5 level Analog to Digital converter is available on P4/ADC pin. This converter can be used to read out an external AFC information via the I2C-BUS interface. The relationship between the external voltage at P4/ADC pin and the bits A2, A1 and A0 is given in **Table 14**. P4 output port cannot be used and the corresponding bit needs to be programmed to logic 0 when the ADC is in use.

1) ADC function is only available in TUA 6039-2.

## 4 Application

### 4.1 Tuner application block diagram

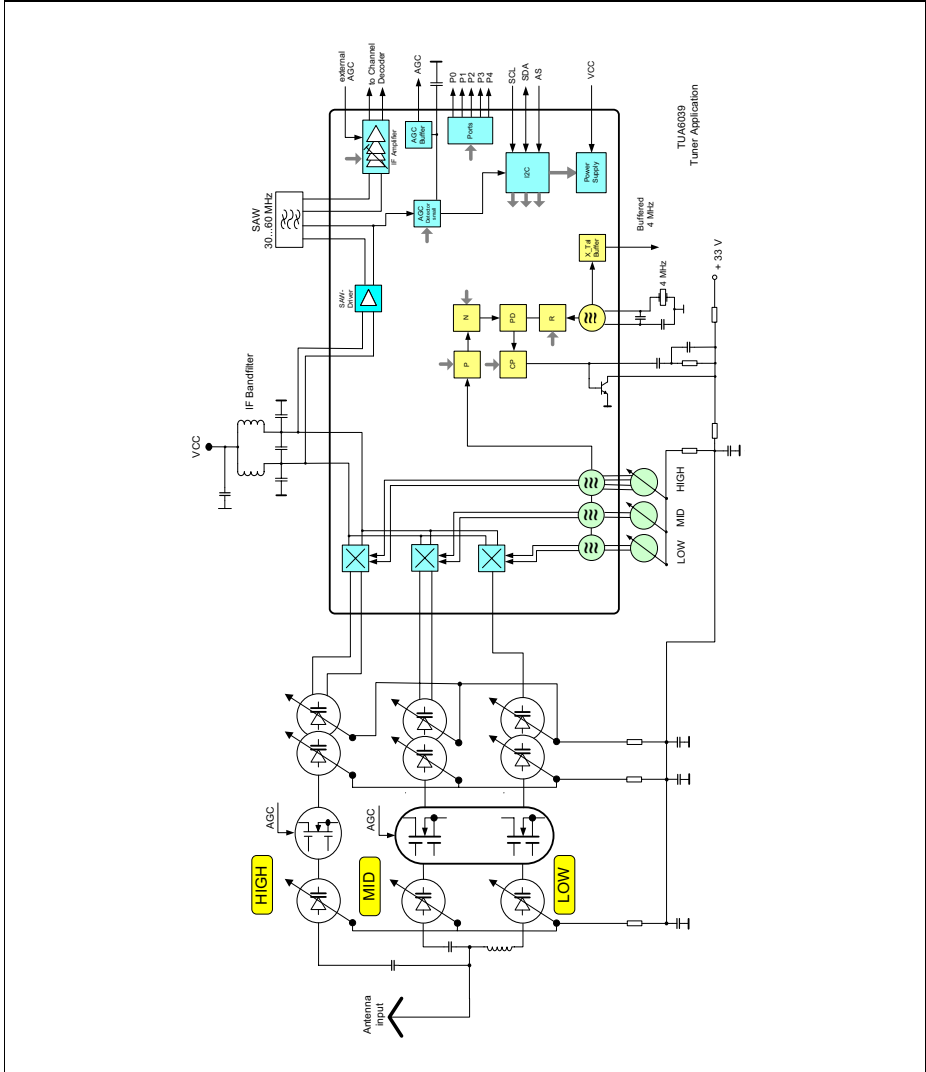
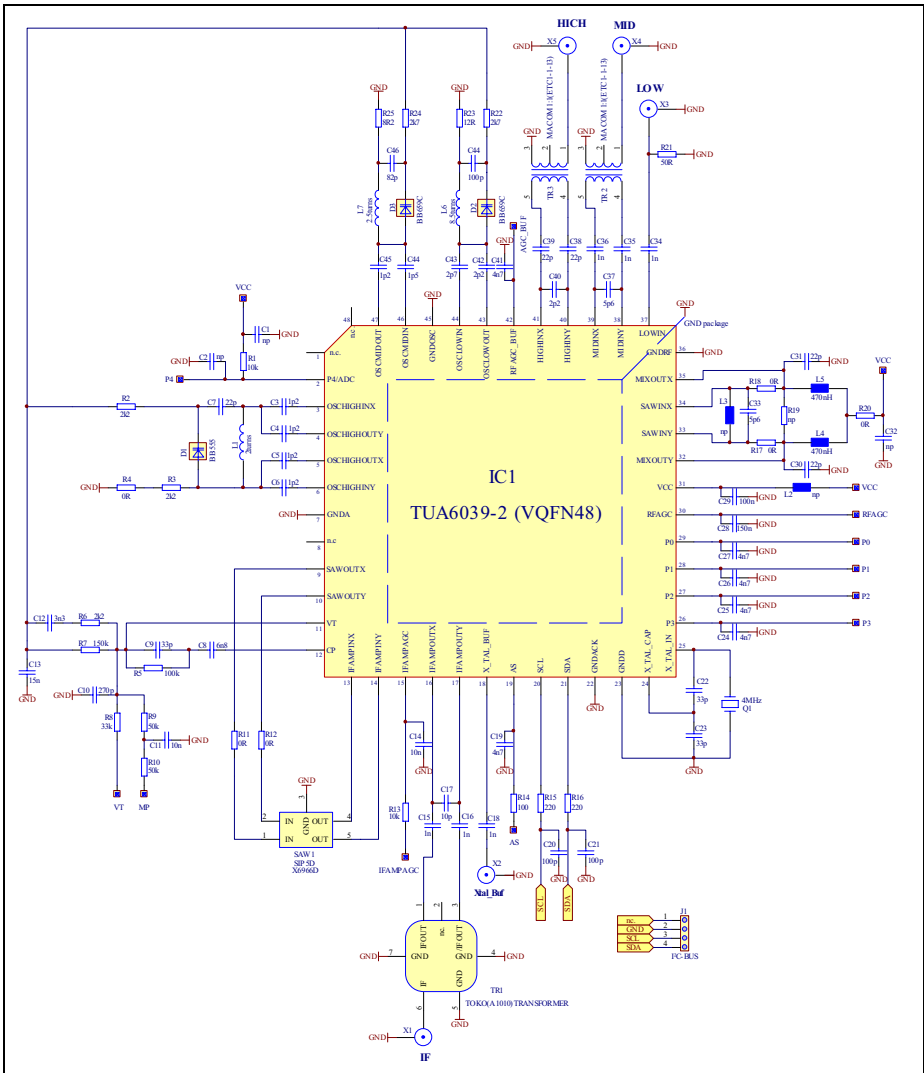


Figure 8 Tuner application block diagram

### 4.2 Application circuit for hybrid application



**Figure 9** Circuit diagram for hybrid application (DVB-T / PAL)

Note: TUA 6039 and TUA 6037 have no ADC function. TUA 6037 has different pinning.

### 4.3 Application circuit for ATSC

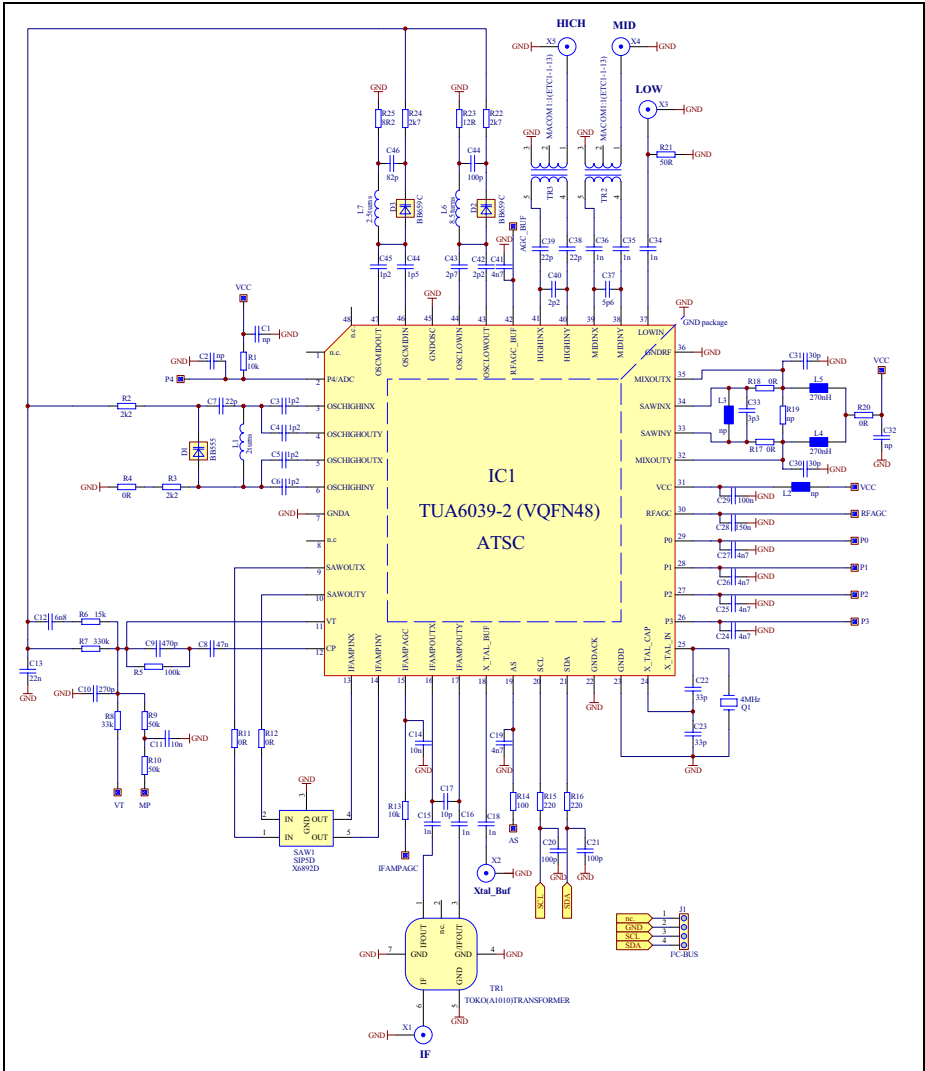


Figure 10 Circuit diagram for ATSC

Note: TUA 6039 and TUA 6037 have no ADC function. TUA 6037 has different pinning.



### 4.4 Application circuit for DVB-T

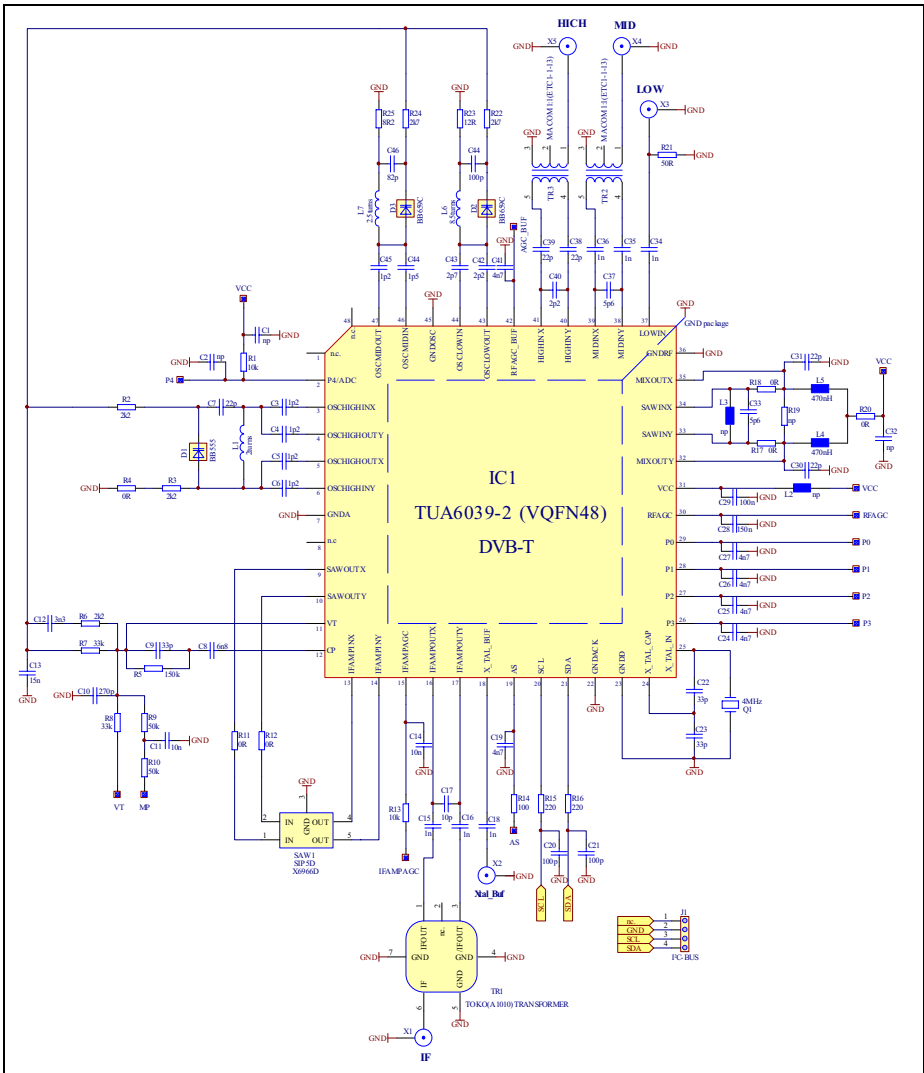


Figure 11 Circuit diagram for DVB-T

Note: TUA 6039 and TUA 6037 have no ADC function. TUA 6037 has different pinning.

4.5 Application circuit for ISDB-T

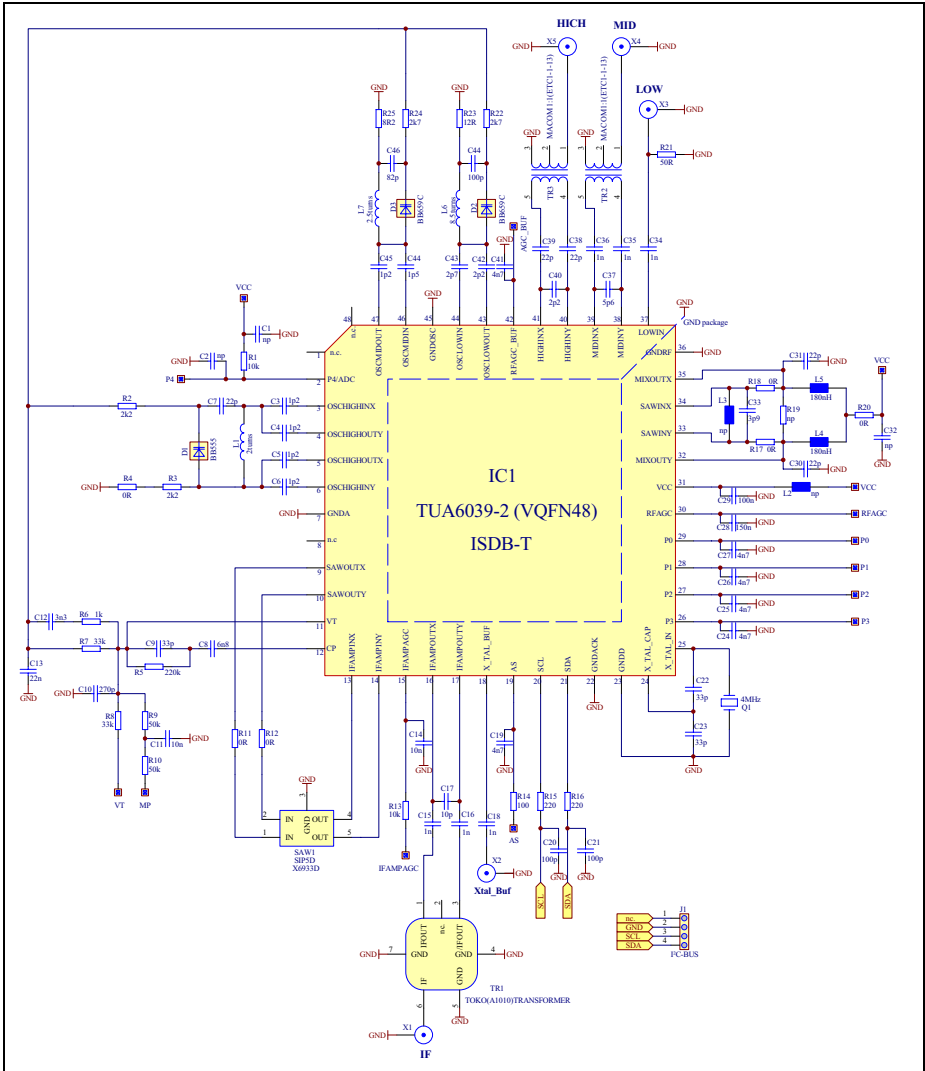


Figure 12 Circuit diagram for ISDB-T

Note: TUA 6039 and TUA 6037 have no ADC function. TUA 6037 has different pinning.

## 5 Reference

### 5.1 Electrical Data

#### 5.1.1 Absolute Maximum Ratings

**Attention:** *The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.*

**Table 5 Absolute Maximum Ratings**

| #   | Parameter <sup>1)</sup>                               | Symbol          | Limit Values |      | Unit | Remarks                                     |
|-----|---|-----------------|--------------|------|------|---|
|     |   |                 | min.         | max. |      |   |
| 1.  | Supply voltage  | $V_{CC}$        | -0.3         | 6    | V    |   |
| 2.  | Ambient temperature                                   | $T_A$           | -40          | +85  | °C   | exposed GND pad soldered                    |
| 3.  | Junction temperature                                  | $T_J$           |              | +125 | °C   |   |
| 4.  | Storage temperature                                   | $T_{Stg}$       | -40          | +125 | °C   |   |
| 5.  | Thermal resistance junction to ambient <sup>2)</sup>  | $R_{THJA}$      |              | 39   | K/W  | exposed GND pad soldered                    |
| 6.  | Temperature difference junction to case <sup>3)</sup> | $T_{JC}$        |              | 3    | K    | exposed GND pad soldered                    |
| PLL |   |                 |              |      |      |   |
| 7.  | CP  | $V_{CP}$        | -0.3         | 3    | V    |   |
| 8.  |   | $I_{CP}$        |              | 1    | mA   |   |
| 9.  | Bus input/output SDA                                  | $V_{SDA}$       | -0.3         | 6    | V    |   |
| 10. | Bus output current SDA during acknowledge             | $I_{SDA(L)}$    |              | 10   | mA   | open collector                              |
| 11. | Bus input SCL   | $V_{SCL}$       | -0.3         | 6    | V    |   |
| 12. | Chip address switch AS                                | $V_{AS}$        | -0.3         | 6    | V    |   |
| 13. | VCO tuning output (loop filter)                       | $V_{VT}$        | -0.3         | 35   | V    |   |
| 14. | PNP port output current of P0,P1,P2,P3                | $I_{PP}$        | -5           | 0    | mA   | open collector                              |
| 15. | Total port output current of PNP ports                | $\Sigma I_{PP}$ | -20          | 0    | mA   | $t_{max} = 0.1 \text{ s at } 5.5 \text{ V}$ |

| #   | Parameter <sup>1)</sup>       | Symbol   | Limit Values |      | Unit | Remarks        |
|-----|-------------------------------|----------|--------------|------|------|----------------|
|     |                               |          | min.         | max. |      |                |
| 16. | NPN port output current of P4 | $I_{PN}$ | 0            | 5    | mA   | open collector |

**Mixer-Oscillator**

|     |                       |                |      |   |    |                                    |
|-----|-----------------------|----------------|------|---|----|------------------------------------|
| 17. | Mix inputs LOW band   | $V_{LOW}$      | -0.3 | 3 | V  |                                    |
| 18. | Mix inputs MID/HIGH   | $V_{MID/HIGH}$ | -0.3 | 2 | V  |                                    |
| 19. | band                  | $I_{MID/HIGH}$ | -5   | 6 | mA |                                    |
| 20. | VCO base voltage      | $V_B$          | -0.3 | 3 | V  | LOW, MID and HIGH band oscillators |
| 21. | VCO collector voltage | $V_C$          |      | 6 | V  | LOW, MID and HIGH band oscillators |

|     |  |             |      |          |    |                |
|-----|--|-------------|------|----------|----|----------------|
| 22. | RF AGC output  | $V_{RFAGC}$ | -0.3 | $V_{CC}$ | V  | $V_{CC} < 4 V$ |
| 23. |  |             | -0.3 | 4        | V  | $V_{CC} > 4 V$ |
| 24. |  | $I_{RFAGC}$ |      | 1        | mA |                |
| 25. | Voltage on all other input and output pins except GNDs | $V_{max}$   | -0.3 | $V_{CC}$ | V  |                |

**ESD-Protection<sup>4)</sup>**

|     |          |           |  |   |    |  |
|-----|----------|-----------|--|---|----|--|
| 26. | all pins | $V_{ESD}$ |  | 2 | kV |  |
|-----|----------|-----------|--|---|----|--|

- 1) All values are referred to ground (pin), unless stated otherwise.  
Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.
- 2) Measured in a multi layer board as defined by JEDEC standard.  
The thermal resistance depends on the PCB board design.
- 3) Referred to top center of package in free air condition.
- 4) According to EIA/JESD22-A114-B (HBM incircuit test), as a single device incircuit contact discharge test.

### 5.1.2 Operating Range

**Table 6 Operating Range**

| #  | Parameter                                     | Symbol     | Limit Values |       | Unit | Remarks                  |
|----|---|------------|--------------|-------|------|--------------------------|
|    |   |            | min.         | max.  |      |                          |
| 1. | Supply voltage                                | $V_{CC}$   | 3.0          | 5.5   | V    | nominal 3.3 V            |
| 2. | Ambient temperature                           | $T_A$      | -20          | +85   | °C   | exposed GND pad soldered |
| 3. | Programmable divider factor                   | N          | 256          | 32767 |      |                          |
| 4. | LOW mixer input frequency range               | $f_{MIXV}$ | 30           | 200   | MHz  |                          |
| 5. | MID and HIGH band mixer input frequency range | $f_{MIXU}$ | 130          | 1000  | MHz  |                          |
| 6. | LOW oscillator frequency range                | $f_{OH}$   | 65           | 250   | MHz  |                          |
| 7. | MID band oscillator frequency range           | $f_{OU}$   | 165          | 530   | MHz  |                          |
| 8. | HIGH band oscillator frequency range          | $f_{OU}$   | 400          | 950   | MHz  |                          |

### 5.1.3 AC/DC Characteristics

**Table 7 AC/DC Characteristics,  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.3\text{ V}$** 

| #      | Parameter <sup>1)</sup>    | Symbol    | Limit Values |      |      | Unit | Test Conditions | ■ |
|--------|----------------------------|-----------|--------------|------|------|------|-----------------|---|
|        |                            |           | min.         | typ. | max. |      |                 |   |
| Supply |                            |           |              |      |      |      |                 |   |
| 1.     | Supply voltage             | $V_{CC}$  | 3.0          | 3.3  | 5.5  | V    |                 |   |
| 2.     | Current                    | $I_{VCC}$ | 80           | 100  | 120  | mA   | LOW band        |   |
| 3.     | consumption in active mode | $I_{VCC}$ | 80           | 100  | 120  | mA   | MID band        |   |
| 4.     |                            | $I_{VCC}$ | 80           | 100  | 120  | mA   | HIGH band       |   |

| #  | Parameter <sup>1)</sup>                | Symbol   | Limit Values |      |      | Unit | Test Conditions | ■ |
|----|--|----------|--------------|------|------|------|-----------------|---|
|    |  |          | min.         | typ. | max. |      |                 |   |
| 5. | Current consumption in power down mode | $I_{pd}$ |              | 12   |      | mA   |                 |   |

**Digital Part**
**PLL**
**Crystal oscillator connections XTAL**

|     |                                       |              |     |       |      |                  |                    |  |
|-----|---------------------------------------|--------------|-----|-------|------|------------------|--------------------|--|
| 6.  | Crystal frequency                     | $f_{XTAL}$   | 3.2 | 4.0   | 4.8  | MHz              |                    |  |
| 7.  | Crystal resistance                    | $R_{XTAL}$   |     | 30    | 300  | $\Omega$         |                    |  |
| 8.  | Crystal oscillator startup capability | $Z_{XTAL}$   |     | -1000 | -650 | $\Omega$         | $f_{XTAL} = 4$ MHz |  |
| 9.  | XTAL Buffer output frequency          | $f_{XTALIO}$ |     | 4.0   |      | MHz              | $f_{XTAL} = 4$ MHz |  |
| 10. | XTAL Buffer Signal voltage            | $V_{AC}$     |     | 400   |      | mV <sub>pp</sub> |                    |  |

**Charge pump output CP**

|     |  |            |           |           |           |         |                                       |  |
|-----|--|------------|-----------|-----------|-----------|---------|---------------------------------------|--|
| 11. | Output current, see <a href="#">Table 15</a> | $I_{CPDH}$ | $\pm 455$ | $\pm 650$ | $\pm 845$ | $\mu A$ | $V_{CP} = 1.4$ V                      |  |
| 12. |  | $I_{CPH}$  | $\pm 175$ | $\pm 250$ | $\pm 325$ | $\mu A$ | $V_{CP} = 1.4$ V                      |  |
| 13. |  | $I_{CPDL}$ | $\pm 87$  | $\pm 125$ | $\pm 163$ | $\mu A$ | $V_{CP} = 1.4$ V                      |  |
| 14. |  | $I_{CPL}$  | $\pm 35$  | $\pm 50$  | $\pm 65$  | $\mu A$ | $V_{CP} = 1.4$ V                      |  |
| 15. | Tristate current                             | $I_{CPZ}$  |           |           | $\pm 10$  | nA      | $V_{CP} = 1.4$ V,<br>T2,T1,OS = 1,0,1 |  |
| 16. | Output voltage                               | $V_{CP}$   | 0.9       | 1.4       | 1.9       | V       | loop locked                           |  |

**Tuning voltage output VT (open collector)**

|     |   |          |     |  |      |         |   |  |
|-----|---|----------|-----|--|------|---------|---|--|
| 17. | Leakage current   | $I_{TH}$ |     |  | 10   | $\mu A$ | $V_{TH} = 33$ V,<br>T2,T1,OS = 0,0,1                            |  |
| 18. | Output voltage when the loop is closed, (test mode in normal operation) | $V_{TL}$ | 0.4 |  | 32.7 | V       | OS = 0,<br>$R_{Load} = 33$ k $\Omega$ ,<br>tuning supply = 33 V |  |

**I<sup>2</sup>C-Bus**
**Bus inputs SCL, SDA**

| #   | Parameter <sup>1)</sup>  | Symbol   | Limit Values |      |      | Unit    | Test Conditions                        | ■ |
|-----|--------------------------|----------|--------------|------|------|---------|--|---|
|     |                          |          | min.         | typ. | max. |         |  |   |
| 19. | High-level input voltage | $V_{IH}$ | 2.5          |      | 5.5  | V       | $V_{CC} = 3.0$ to $5.5$ V              |   |
| 20. | Low-level input voltage  | $V_{IL}$ | 0            |      | 1    | V       | $V_{CC} = 3.0$ to $5.5$ V              |   |
| 21. | High-level input current | $I_{IH}$ |              |      | 10   | $\mu$ A | $V_{bus} = 5.5$ V,<br>$V_{CC} = 0$ V   |   |
| 22. |                          | $I_{IH}$ |              |      | 10   | $\mu$ A | $V_{bus} = 5.5$ V,<br>$V_{CC} = 5.5$ V |   |
| 23. | Low-level input current  | $I_{IL}$ |              |      | 10   | $\mu$ A | $V_{bus} = 1.5$ V,<br>$V_{CC} = 0$ V   |   |
| 24. |                          | $I_{IL}$ | -10          |      |      | $\mu$ A | $V_{bus} = 0$ V,<br>$V_{CC} = 5.5$ V   |   |

**Bus output SDA (open collector)**

|     |                          |          |  |  |     |         |                  |  |
|-----|--------------------------|----------|--|--|-----|---------|------------------|--|
| 25. | Leakage current          | $I_{OH}$ |  |  | 10  | $\mu$ A | $V_{OH} = 5.5$ V |  |
| 26. | Low-level output voltage | $V_{OL}$ |  |  | 0.4 | V       | $I_{OL} = 3$ mA  |  |

**Edge speed SCL,SDA**

|     |           |       |  |  |     |    |  |  |
|-----|-----------|-------|--|--|-----|----|--|--|
| 27. | Rise time | $t_r$ |  |  | 300 | ns |  |  |
| 28. | Fall time | $t_f$ |  |  | 300 | ns |  |  |

**Clock timing SCL**

|     |                  |           |     |     |     |         |  |  |
|-----|------------------|-----------|-----|-----|-----|---------|--|--|
| 29. | Frequency        | $f_{SCL}$ | 0   | 100 | 400 | kHz     |  |  |
| 30. | High pulse width | $t_H$     | 0.6 |     |     | $\mu$ s |  |  |
| 31. | Low pulse width  | $t_L$     | 1.3 |     |     | $\mu$ s |  |  |

**Start condition**

|     |             |             |     |  |  |         |  |  |
|-----|-------------|-------------|-----|--|--|---------|--|--|
| 32. | Set-up time | $t_{susta}$ | 0.6 |  |  | $\mu$ s |  |  |
| 33. | Hold time   | $t_{hsta}$  | 0.6 |  |  | $\mu$ s |  |  |

**Stop condition**

|     |  |             |     |  |  |         |  |  |
|-----|--|-------------|-----|--|--|---------|--|--|
| 34. | Set up time                                      | $t_{susto}$ | 0.6 |  |  | $\mu$ s |  |  |
| 35. | Bus free time between a STOP and START condition | $t_{buf}$   | 1.3 |  |  | $\mu$ s |  |  |

**Data transfer**

| #   | Parameter <sup>1)</sup>                          | Symbol             | Limit Values |      |      | Unit          | Test Conditions | ■ |
|-----|--|--------------------|--------------|------|------|---------------|-----------------|---|
|     |  |                    | min.         | typ. | max. |               |                 |   |
| 36. | Set-up time                                      | $t_{\text{sudat}}$ | 0.1          |      |      | $\mu\text{s}$ |                 |   |
| 37. | Hold time  | $t_{\text{hdat}}$  | 0            |      |      | $\mu\text{s}$ |                 |   |
| 38. | Input hysteresis<br>SCL, SDA                     | $V_{\text{hys}}$   |              | 200  |      | mV            |                 |   |
| 39. | Pulse width of<br>spikes which are<br>suppressed | $t_{\text{sp}}$    | 0            |      | 50   | ns            |                 |   |
| 40. | Capacitive load for<br>each bus line             | $C_L$              |              |      | 400  | pF            |                 |   |

**Ports**

|     |                                     |   |  |      |     |               |                                |  |
|-----|-------------------------------------|---|--|------|-----|---------------|--------------------------------|--|
| 41. | PNP Output<br>saturation<br>voltage | $V_{\text{PP,sat}} =$<br>$V_{\text{CC}} -$<br>$V_{\text{CE,sat}}$ |  | 0.25 | 0.4 | V             | $I_{\text{PP}} = 5 \text{ mA}$ |  |
| 42. | NPN Output<br>saturation<br>voltage | $V_{\text{PN,sat}}$   |  | 0.25 | 0.4 | V             | $I_{\text{PN}} = 5 \text{ mA}$ |  |
| 43. | Port Output<br>leakage current      | $I_{\text{LEAK,Port}}$  |  |      | 10  | $\mu\text{A}$ |                                |  |

**ADC input (only available in TUA 6039-2)**

|     |                             |                   |     |  |                 |               |  |  |
|-----|-----------------------------|-------------------|-----|--|-----------------|---------------|--|--|
| 44. | ADC input voltage           | $V_{\text{ADC}}$  | 0   |  | $V_{\text{CC}}$ | V             |  |  |
| 45. | High-level input<br>current | $I_{\text{ADCH}}$ |     |  | 10              | $\mu\text{A}$ |  |  |
| 46. | Low-level input<br>current  | $I_{\text{ADCL}}$ | -10 |  |                 | $\mu\text{A}$ |  |  |

**Analog Part**
**LOW band mixer and SAW filter driver**

|     |              |                 |       |    |        |     |   |  |
|-----|--------------|-----------------|-------|----|--------|-----|---|--|
| 47. | RF frequency | $f_{\text{RF}}$ | 44.25 |    | 170.25 | MHz | picture carrier <sup>2)</sup>   |  |
| 48. | Voltage gain | $G_V$           | 21    | 24 | 27     | dB  | $f_{\text{RF}} = 48.25 \text{ MHz}$ to<br>154.25 MHz<br>see <a href="#">Section 5.5.1</a> |  |
| 49. | Noise figure | NF              |       | 8  | 10     | dB  | $f_{\text{RF}} = 48.25 \text{ MHz}$ to<br>154.25 MHz<br>see <a href="#">Section 5.5.4</a> |  |



| #   | Parameter <sup>1)</sup>  | Symbol      | Limit Values |      |      | Unit       | Test Conditions   | ■ |
|-----|--|-------------|--------------|------|------|------------|---|---|
|     |  |             | min.         | typ. | max. |            |   |   |
| 50. | SAWOUT output voltage causing 0.8% of crossmodulation in channel | $V_o$       |              | 120  |      | dB $\mu$ V | $f_{RF} = 48.25$ MHz to 154.25 MHz<br>see <a href="#">Section 5.5.6</a>                   |   |
| 51. | Input IP3  | IIP3        |              | 117  |      | dB $\mu$ V | $f_{RF1} = 48.25$ MHz,<br>$f_{RF2} = 49.25$ MHz,<br>$P_{RF1} = P_{RF2}$                   |   |
| 52. |  | IIP3        |              | 117  |      | dB $\mu$ V | $f_{RF1} = 154.25$ MHz,<br>$f_{RF2} = 155.25$ MHz,<br>$P_{RF1} = P_{RF2}$                 |   |
| 53. | Local oscillator FM caused by I <sup>2</sup> C communication     | $FM_{I2C}$  |              |      | 2.12 | kHz        | $f_{RF} = 154.25$ MHz <sup>3)</sup>   |   |
| 54. | (N+5) - 1 MHz pulling  | N+5 - 1 MHz | 77           | 80   |      | dB $\mu$ V | $f_{RFW} = 69.25$ MHz,<br>$f_{OSC} = 108.15$ MHz,<br>$f_{RFU} = 108.25$ MHz <sup>4)</sup> |   |
| 55. | Input impedance  | $R_p$       |              | 1    |      | k $\Omega$ | parallel equivalent circuit at 100 MHz <sup>5)</sup><br>see <a href="#">Section 5.4.1</a> |   |
| 56. | $Z_i = (R_p \parallel 1/j\omega C_p)$                            | $C_p$       |              | 2    |      | pF         |   |   |

## Mid band mixer and SAW filter driver

|     |  |          |        |     |        |            |  |  |
|-----|--|----------|--------|-----|--------|------------|--|--|
| 57. | RF frequency   | $f_{RF}$ | 154.25 |     | 454.25 | MHz        | picture carrier <sup>2)</sup>  |  |
| 58. | Voltage gain   | $G_V$    | 31     | 34  | 37     | dB         | $f_{RF} = 161.25$ MHz to 439.25 MHz<br>see <a href="#">Section 5.5.2</a> |  |
| 59. | Noise figure (not corrected for image)                           | NF       |        | 6   | 8      | dB         | $f_{RF} = 161.25$ MHz to 439.25 MHz<br>see <a href="#">Section 5.5.5</a> |  |
| 60. | SAWOUT output voltage causing 0.8% of crossmodulation in channel | $V_o$    |        | 120 |        | dB $\mu$ V | $f_{RF} = 161.25$ MHz to 439.25 MHz<br>see <a href="#">Section 5.5.7</a> |  |

| #   | Parameter <sup>1)</sup>                                      | Symbol            | Limit Values |      |      | Unit | Test Conditions   | ■ |
|-----|--|-------------------|--------------|------|------|------|---|---|
|     |  |                   | min.         | typ. | max. |      |   |   |
| 61. | Input IP3  | IIP3              |              | 106  |      | dBμV | $f_{RF1} = 161.25 \text{ MHz}$<br>$f_{RF2} = 162.25 \text{ MHz}$ ,<br>$P_{RF1} = P_{RF2}$                   |   |
| 62. |  | IIP3              |              | 105  |      | dBμV | $f_{RF1} = 439.25 \text{ MHz}$<br>$f_{RF2} = 440.25 \text{ MHz}$ ,<br>$P_{RF1} = P_{RF2}$                   |   |
| 63. | Local oscillator FM caused by I <sup>2</sup> C communication | FM <sub>I2C</sub> |              |      | 2.12 | kHz  | $f_{RF} = 439.25 \text{ MHz}^{3)}$  |   |
| 64. | (N+5) - 1 MHz pulling  | N+5 - 1 MHz       | 77           | 80   |      | dBμV | $f_{RFW} = 359.25 \text{ MHz}$ ,<br>$f_{OSC} = 398.15 \text{ MHz}$ ,<br>$f_{RFU} = 398.25 \text{ MHz}^{4)}$ |   |
| 65. | Input impedance  | R <sub>s</sub>    |              | 22   |      | Ω    | series equivalent circuit at 300 MHz <sup>5)</sup>  |   |
| 66. | Z <sub>i</sub> = (R <sub>s</sub> + jωL <sub>s</sub> )        | L <sub>s</sub>    |              | 2.7  |      | nH   | see <a href="#">Section 5.4.2</a>   |   |

## HIGH band mixer and SAW filter driver

|     |  |                 |        |     |        |      |   |  |
|-----|--|-----------------|--------|-----|--------|------|---|--|
| 67. | RF frequency   | f <sub>RF</sub> | 399.25 |     | 863.25 | MHz  | picture carrier <sup>2)</sup>   |  |
| 68. | Voltage gain   | G <sub>V</sub>  | 31     | 34  | 37     | dB   | $f_{RF} = 447.25 \text{ MHz}$<br>to 863.25 MHz<br>see <a href="#">Section 5.5.2</a>     |  |
| 69. | Noise figure (not corrected for image)                           | NF              |        | 6   | 8      | dB   | $f_{RF} = 447.25 \text{ MHz}$<br>to 863.25 MHz<br>see <a href="#">Section 5.5.5</a>     |  |
| 70. | SAWOUT output voltage causing 0.8% of crossmodulation in channel | V <sub>o</sub>  |        | 120 |        | dBμV | $f_{RF} = 447.25 \text{ MHz}$<br>to 863.25 MHz<br>see <a href="#">Section 5.5.7</a>     |  |
| 71. | Input IP3  | IIP3            |        | 105 |        | dBμV | $f_{RF1} = 447.25 \text{ MHz}$<br>$f_{RF2} = 448.25 \text{ MHz}$<br>$P_{RF1} = P_{RF2}$ |  |
| 72. |  | IIP3            |        | 105 |        | dBμV | $f_{RF1} = 863.25 \text{ MHz}$<br>$f_{RF2} = 864.25 \text{ MHz}$<br>$P_{RF1} = P_{RF2}$ |  |

| #   | Parameter <sup>1)</sup>                                      | Symbol            | Limit Values |      |      | Unit | Test Conditions   | ■ |
|-----|--|-------------------|--------------|------|------|------|---|---|
|     |  |                   | min.         | typ. | max. |      |   |   |
| 73. | Local oscillator FM caused by I <sup>2</sup> C communication | FM <sub>I2C</sub> |              |      | 2.12 | kHz  | f <sub>RF</sub> = 863.25 MHz <sup>3)</sup>  |   |
| 74. | (N+5) - 1 MHz pulling  | N+5<br>- 1 MHz    | 77           | 80   |      | dBμV | f <sub>RFw</sub> = 823.25 MHz,<br>f <sub>OSC</sub> = 862.15 MHz,<br>f <sub>RFu</sub> = 862.25 MHz <sup>4)</sup> |   |
| 75. | Input impedance  | R <sub>s</sub>    |              | 25   |      | Ω    | series equivalent circuit at 650 MHz <sup>5)</sup><br>see <a href="#">Section 5.4.3</a>                         |   |
| 76. | Z <sub>i</sub> = (R <sub>s</sub> + jωL <sub>s</sub> )        | L <sub>s</sub>    |              | 2.5  |      | nH   |   |   |

## LOW band oscillator

|     |   |                  |    |      |      |        |   |   |  |
|-----|---|------------------|----|------|------|--------|---|---|--|
| 77. | Oscillator frequency                    | f <sub>OSC</sub> | 80 |      | 210  | MHz    | <sup>6)</sup>   |   |  |
| 78. | Phase noise, carrier to noise sideband  | Φ <sub>OSC</sub> |    | -85  | -77  | dBc/Hz | ±1 kHz frequency offset, worst case in the frequency range <sup>7)</sup>      |   |  |
| 79. |   |                  |    | -92  | -88  | dBc/Hz |   | ±10 kHz frequency offset, worst case in the frequency range <sup>8)</sup> |  |
| 80. |   |                  |    | -112 | -108 | dBc/Hz |   | ±100 kHz frequency offset, worst case in the frequency range              |  |
| 81. | Ripple susceptibility of V <sub>p</sub> | RSC              |    | -50  |      | dBc    | V <sub>Ripple</sub> = 20 mVpp,<br>f <sub>Ripple</sub> = 100 kHz <sup>9)</sup> |   |  |

## MID band oscillator

|     |                      |                  |     |  |     |     |               |  |
|-----|----------------------|------------------|-----|--|-----|-----|---------------|--|
| 82. | Oscillator frequency | f <sub>OSC</sub> | 201 |  | 493 | MHz | <sup>6)</sup> |  |
|-----|----------------------|------------------|-----|--|-----|-----|---------------|--|

| #                           | Parameter <sup>1)</sup>                | Symbol              | Limit Values |      |      | Unit   | Test Conditions  | ■      |        |  |
|-----------------------------|--|---------------------|--------------|------|------|--------|--|--------|--------|--|
|                             |  |                     | min.         | typ. | max. |        |  |        |        |  |
| 83.                         | Phase noise, carrier to noise sideband | $\Phi_{\text{OSC}}$ |              | -80  | -73  | dBc/Hz | $\pm 1$ kHz frequency offset, worst case in the frequency range <sup>7)</sup>  |        |        |  |
| 84.                         |  |                     |              | -92  | -88  |        |  |        | dBc/Hz | $\pm 10$ kHz frequency offset, worst case in the frequency range <sup>8)</sup> |
| 85.                         |  |                     |              | -112 | -108 |        |  |        |        |  |
| 86.                         | Ripple susceptibility of $V_P$         | RSC                 |              | -60  |      | dBc    | $V_{\text{Ripple}} = 20$ mVpp, $f_{\text{Ripple}} = 100$ kHz <sup>9)</sup>     |        |        |  |
| <b>HIGH band oscillator</b> |  |                     |              |      |      |        |  |        |        |  |
| 87.                         | Oscillator frequency                   | $f_{\text{OSC}}$    | 435          |      | 905  | MHz    | <sup>6)</sup>  |        |        |  |
| 88.                         | Phase noise, carrier to noise sideband | $\Phi_{\text{OSC}}$ |              | -77  | -70  |        |  |        | dBc/Hz | $\pm 1$ kHz frequency offset, worst case in the frequency range <sup>7)</sup>  |
| 89.                         |  |                     |              | -90  | -86  | dBc/Hz | $\pm 10$ kHz frequency offset, worst case in the frequency range <sup>8)</sup> |        |        |  |
| 90.                         |  |                     |              | -110 | -106 |        |  | dBc/Hz |        |  |
| 91.                         | Ripple susceptibility of $V_P$         | RSC                 |              | -60  |      | dBc    | $V_{\text{Ripple}} = 20$ mVpp, $f_{\text{Ripple}} = 100$ kHz <sup>9)</sup>     |        |        |  |
| <b>SAW filter driver</b>    |  |                     |              |      |      |        |  |        |        |  |
| 92.                         | Voltage gain                           | $G_V$               |              | 20   |      | dB     | $f_{\text{IF}} = 36$ MHz to 54 MHz   |        |        |  |

| #   | Parameter <sup>1)</sup>                 | Symbol | Limit Values |      |      | Unit       | Test Conditions  | ■ |
|-----|---|--------|--------------|------|------|------------|--|---|
|     |   |        | min.         | typ. | max. |            |  |   |
| 93. | Output voltage causing 1 dB compression | $V_o$  |              | 126  |      | dB $\mu$ V |  |   |
| 94. | Input impedance                         | $R_p$  |              | 470  |      | $\Omega$   | parallel equivalent circuit at 36 MHz <sup>5)</sup><br>see <a href="#">Section 5.4.5</a> |   |
| 95. | $Z_i = (R_p \parallel 1/j\omega C_p)$   | $C_p$  |              | 6    |      | pF         |  |   |
| 96. | Output impedance                        | $R_s$  |              | 25   |      | $\Omega$   | series equivalent circuit at 36 MHz <sup>5)</sup><br>see <a href="#">Section 5.4.6</a>   |   |
| 97. | $Z_o = (R_s + j\omega L_s)$             | $L_s$  |              | 50   |      | nH         |  |   |

## Rejection at the SAW driver outputs

|      |   |              |  |     |     |     |  |  |
|------|---|--------------|--|-----|-----|-----|--|--|
| 98.  | Level of divider interferences in the IF signal | $INT_{DIV}$  |  | -66 | -60 | dBc | $V_{OUT} = 100 \text{ dB}\mu\text{V}^{10)}$  |  |
| 99.  | Crystal oscillator interferences rejection      | $INT_{XTAL}$ |  | -66 | -60 | dBc | $V_{OUT} = 100 \text{ dB}\mu\text{V}^{11)}$  |  |
| 100. | Reference frequency rejection                   | $INT_{REF}$  |  | -66 | -60 | dBc | $V_{OUT} = 100 \text{ dB}\mu\text{V}^{12)}$  |  |
| 101. | Channel S02 beat                                | $INT_{S02}$  |  | -66 | -60 | dBc | $f_{RFpix} = 76.25 \text{ MHz}$ ,<br>$V_{RFpix} = 80 \text{ dB}\mu\text{V}$ ,<br>$f_{IF} = 38.9 \text{ MHz}^{13)}$ |  |

## RF AGC output

|      |   |                       |     |     |      |            |   |  |
|------|---|-----------------------|-----|-----|------|------------|---|--|
| 102. | RF AGC output   | $AGC_{TOP}$<br>narrow | 103 |     | 115  | dB $\mu$ V |   |  |
| 103. | Source current 1  | $I_{AGCfast}$         |     | 9.0 |      | $\mu$ A    |   |  |
| 104. | Source current 2  | $I_{AGCslow}$         |     | 300 |      | nA         |   |  |
| 105. | Peak sink to ground   | $I_{AGCpeak}$         |     | 100 |      | $\mu$ A    |   |  |
| 106. | RF AGC output voltage   | $V_{AGCmax}$          |     | 3   |      | V          | maximum level,<br>$I_{AGC} = 9 \mu\text{A}$ |  |
| 107. |   | $V_{AGCmin}$          | 0   |     | 0.25 | V          | minimum level                               |  |
| 108. | RF voltage range to switch the AGC from active to inactive mode | $AGC_{SLIP}$          |     |     | 0.5  | dB         |   |  |

| #               | Parameter <sup>1)</sup>                           | Symbol              | Limit Values |      |      | Unit       | Test Conditions  | ■ |
|-----------------|---|---------------------|--------------|------|------|------------|--|---|
|                 |   |                     | min.         | typ. | max. |            |  |   |
| 109.            | RF AGC leakage current                            | $AGC_{LEAK}$        | -50          |      | 50   | nA         | $0 < V_{AGC} < V_{CC}$ ,<br>AL2, AL1, AL0 =<br>1, 1, 0   |   |
| 110.            | RF AGC output voltage                             | $AGC_{OFF}$         |              | 3    |      | V          | AGC is disabled,<br>$I_{AGC} = 9 \mu A$  |   |
| RF AGC buffer   |   |                     |              |      |      |            |  |   |
| 111.            | RF AGC buffer output current                      | $I_{max}$           |              |      | 1    | mA         |  |   |
| 112.            | RF AGC buffer output saturation voltage low       | $V_{low}$           |              | 120  | 200  | mV         | $I_{load} = 1 \text{ mA}$  |   |
| 113.            | RF AGC buffer output saturation voltage high      | $V_{CC} - V_{high}$ |              | 170  | 300  | mV         | $I_{load} = 1 \text{ mA}$  |   |
| IFAGC amplifier |   |                     |              |      |      |            |  |   |
| 114.            | Voltage gain                                      | $G_{max}$           |              | 65   |      | dB         | $V_{IFAGC} \geq 2.0 \text{ V}$   |   |
| 115.            |   | $G_{min}$           |              | 9    |      | dB         | $V_{IFAGC} \leq 0.2 \text{ V}$   |   |
| 116.            | Maximum IF input level                            | $V_{IF/IF}$         |              | 102  |      | dB $\mu$ V | min. gain,<br>$f_{IF/IF} = 36 \text{ MHz}$<br>(sine),<br>$V_{IFAGC} = 0.2 \text{ V}$ ,<br>$V_{OUT/OUT} = 1 \text{ V}_{pp}$   |   |
| 117.            | Minimum IF input level                            | $V_{IF/IF}$         |              | 46   |      |            | max. gain,<br>$f_{IF/IF} = 36 \text{ MHz}$<br>(sine),<br>$V_{IFAGC} = 2 \text{ V}$ ,<br>$V_{OUT/OUT} = 1 \text{ V}_{pp}$   |   |
| 118.            | Input impedance                                   | $R_{IF/IF}$         |              | 2    |      | k $\Omega$ | parallel equivalent circuit at 36 MHz <sup>5)</sup><br>see <a href="#">Section 5.4.7</a>   |   |
| 119.            | $Z_i = (R_{IF/IF} \parallel 1/j\omega C_{IF/IF})$ | $C_{IF/IF}$         |              | 1.5  |      | pF         |  |   |
| 120.            | Low end cutoff frequency (-1 dB)                  | $f_L$               |              |      | 25   | MHz        | $V_{IF/IF} = 60 \text{ dB}\mu\text{V}$ ,<br>$R_{LOAD} \geq 5 \text{ k}\Omega$ ,<br>$C_{LOAD} \leq 1.5 \text{ pF}$ ,<br>$V_{OUT/OUT} = 1 \text{ V}_{pp}$ at<br>$f_{IF/IF} = 36 \text{ MHz}$<br>(sine) |   |
| 121.            | High end cutoff frequency (-1 dB)                 | $f_H$               | 65           |      |      | MHz        |  |   |

| #    | Parameter <sup>1)</sup>                 | Symbol      | Limit Values |      |      | Unit                   | Test Conditions  | ■ |
|------|---|-------------|--------------|------|------|------------------------|--|---|
|      |   |             | min.         | typ. | max. |                        |  |   |
| 122. | Intermodulation                         | C/IM3       |              | -56  |      | dBc                    | $f_{IF/IF1} = 37 \text{ MHz}$ ,<br>$f_{IF/IF2} = 38 \text{ MHz}$ ,<br>$V_{IF/IF1} = 90 \text{ dB}\mu\text{V}$ ,<br>$V_{IF/IF2} = 90 \text{ dB}\mu\text{V}$ ,<br>$R_{LOAD} \geq 5 \text{ k}\Omega$ ,<br>$C_{LOAD} \leq 10 \text{ pF}$ ,<br>$V_{OUT/OUT} = 1 \text{ V}_{pp}$ |   |
| 123. | Third order output intercept point      | OIP3        |              | 138  |      | $\text{dB}\mu\text{V}$ | $f_{IF/IF1} = 37 \text{ MHz}$ ,<br>$f_{IF/IF2} = 38 \text{ MHz}$ ,<br>$V_{IF/IF1} = 90 \text{ dB}\mu\text{V}$ ,<br>$V_{IF/IF2} = 90 \text{ dB}\mu\text{V}$ ,<br>$R_{LOAD} \geq 5 \text{ k}\Omega$ ,<br>$C_{LOAD} \leq 10 \text{ pF}$ ,<br>$V_{OUT/OUT} = 1 \text{ V}_{pp}$ |   |
| 124. | Signal to noise ratio                   | SNR         |              | 43   |      | dB                     | $f_{IF/IF} = 36 \text{ MHz}$<br>(sine),<br>$V_{IF/IF} = 60 \text{ dB}\mu\text{V}$ ,<br>$V_{OUT/OUT} = 1 \text{ V}_{pp}$ ,<br>$BW = 8 \text{ MHz}$  |   |
| 125. | Noise figure                            |             |              | 9    |      | dB                     | max. gain  |   |
| 126. | Output impedance                        | $R_{IF/IF}$ |              | 90   | 150  | $\Omega$               | series equivalent circuit at 36 MHz <sup>5)</sup><br>see <a href="#">Section 5.4.8</a>   |   |
| 127. | $Z_o = (R_{IF/IF} + j\omega L_{IF/IF})$ | $L_{IF/IF}$ |              | 120  |      | nH                     |  |   |

- 1) Values are referred to the application given in [Figure 9](#) and  $f_{IF} = 36 \text{ MHz}$ , unless stated otherwise.
- 2) The RF frequency range is defined by the oscillator frequency range and the intermediate frequency (IF).
- 3) Local oscillator FM modulation resulting from I<sup>2</sup>C communication is measured at the IF output using a modulation analyzer with a peak to peak detector  $((P_+ + P_-) / 2)$  and a post detection filter 20 Hz - 100 kHz. The I<sup>2</sup>C messages are sent to the tuner in such a way that the tuner is addressed but the content of the PLL registers are not altered. The refresh interval between each data set shall be 20 ms to 1 s.
- 4) (N+5) -1 MHz is defined as the input level of channel N+5, at frequency 1 MHz lower, causing 100 kHz FM sidebands 30 dB below the wanted carrier.
- 5) Impedance measured with differential 2-port measurement at input or output. Input and output pins directly connected to measurement equipment with 50  $\Omega$  strip lines.
- 6) Limits are related to the tank circuit used in the application board (see [Figure 9](#)). Frequency bands may be adjusted by the choice of external components.
- 7) For wide loop filter application (see [Figure 11](#)).
- 8) For narrow loop filter application (see [Figure 10](#)).

- 9) The supply ripple susceptibility is a sideband measurement using a spectrum analyzer connected to the IF output. An unmodulated RF signal with a level of 80 dB $\mu$ V is applied to the test board RF input. A sinusoidal signal with a defined frequency is superposed onto the supply voltage (see [Figure 21](#)). The specified value is the worst case in the frequency range.
- 10) This is the level of divider interferences close to the IF frequency. For example channel S3:  $f_{OSC} = 158.15$  MHz,  $1/4 f_{OSC} = 39.5375$  MHz. The rejection has to be greater than 60 dB for an SAW driver output of 100 dB $\mu$ V.
- 11) Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator. The rejection has to be greater than 60 dB for an SAW driver output of 100 dB $\mu$ V.
- 12) The reference frequency rejection is the level of reference frequency sidebands according to the application circuit (166.67 kHz for DVB-T standard, 142.86 kHz for ISDB-T standard or 62.5 kHz for ATSC standard) related to the carrier. The rejection has to be better than 60 dB for a SAW driver output level of 100 dB $\mu$ V. In hybrid application the rejection is valid for the digital reference frequency (166.67 kHz for DVB-T/PAL standard, or 142.86 kHz for ISDB-T/NTSC standard), but any lower analog reference frequency may reduce this rejection.
- 13) Channel S02 beat is the interfering product of  $f_{RFpix}$ ,  $f_{IF}$  and  $f_{OSC}$  of channel S02,  $f_{BEAT} = 37.35$  MHz. The possible mechanisms are  $f_{OSC} - 2 \times f_{IF}$  or  $2 \times f_{RFpix} - f_{OSC}$ .

## 5.2 Bus Interface

**Table 8 Bit Allocation Read/Write**

| Name  | Byte | Bits |      |      |      |      |      |      |       | Ack |
|---|------|------|------|------|------|------|------|------|-------|-----|
|   |      | MSB  | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | LSB   |     |
| Write Data (for TUA 6039-2, TUA 6039, TUA 6037) |      |      |      |      |      |      |      |      |       |     |
| Address Byte                                    | ADB  | 1    | 1    | 0    | 0    | 0    | MA1  | MA0  | R/W=0 | A   |
| Divider Byte 1                                  | DB1  | 0    | N14  | N13  | N12  | N11  | N10  | N9   | N8    | A   |
| Divider Byte 2                                  | DB2  | N7   | N6   | N5   | N4   | N3   | N2   | N1   | N0    | A   |
| Control byte                                    | CB   | 1    | CP   | T2   | T1   | T0   | RSA  | RSB  | OS    | A   |
| Bandswitch byte                                 | BB   | XTB  |      |      | P4   | P3   | P2   | P1   | P0    | A   |
| Auxiliary byte <sup>1)</sup>                    | AB   | ATC  | AL2  | AL1  | AL0  | 0    | 0    | 0    | LP    | A   |
| Read data (for TUA 6039-2)                      |      |      |      |      |      |      |      |      |       |     |
| Address byte                                    | ADB  | 1    | 1    | 0    | 0    | 0    | MA1  | MA0  | R/W=1 | A   |
| Status byte                                     | SB   | POR  | FL   | 1    | NBD  | AGC  | A2   | A1   | A0    | A   |
| Read data (for TUA 6039, TUA 6037)              |      |      |      |      |      |      |      |      |       |     |
| Address byte                                    | ADB  | 1    | 1    | 0    | 0    | 0    | MA1  | MA0  | R/W=1 | A   |
| Status byte                                     | SB   | POR  | FL   | 1    | 1    | AGC  | NBD  | 1    | 1     | A   |

1) AB replaces BB when T2, T1, T0 = 0, 1, 1, see [Table 11](#).



**Table 9 Description of Symbols**

| <b>Symbol</b>  | <b>Description</b>  |
|----------------|---|
| A              | Acknowledge   |
| MA0, MA1       | Address selection bits, see <a href="#">Table 10</a>  |
| N14 to N0      | programmable divider bits:<br>$N = 2^{14} \times N14 + 2^{13} \times N13 + \dots + 2^3 \times N3 + 2^2 \times N2 + 2^1 \times N1 + N0$  |
| CP             | charge pump current bit:<br>bit = 0: charge pump current = 50 $\mu$ A or 125 $\mu$ A<br>bit = 1: charge pump current = 250 $\mu$ A (default) or 650 $\mu$ A, see <a href="#">Table 15</a> |
| T0, T1, T2     | test bits, <a href="#">Table 11</a>   |
| RSA, RSB       | reference divider bits, see <a href="#">Table 12</a>  |
| OS             | tuning amplifier control bit:<br>bit = 0: enable $V_T$ ; bit = 1: disable $V_T$ (default)   |
| XTB            | disable XTAL buffer control bit:<br>bit = 0: enable XTAL buffer (default); bit = 1: disable XTAL buffer   |
| P0, P1, P2, P3 | PNP ports control bits:<br>bit = 0: Port is inactive, high impedance state (default)<br>bit = 1: Port is active, $V_{OUT} = V_{CC} - V_{CE,sat}$  |
| P4             | NPN port control bit:<br>bit = 0: Port is inactive, high impedance state (default)<br>bit = 1: Port is active, $V_{OUT} = V_{CE,sat}$   |
| ATC            | RF AGC time constant bit:<br>bit = 0: $I_{AGC} = 300$ nA; $\Delta t = 2$ s with C = 160 nF (default)<br>bit = 1: $I_{AGC} = 9$ $\mu$ A; $\Delta t = 50$ ms with C = 160 nF                |
| AL0, AL1, AL2  | RF AGC take-over point bits, see <a href="#">Table 13</a>   |
| LP             | Loop through:<br>bit = 0: disable loop through (default); bit = 1: enable loop through  |
| POR            | Power-on reset flag, bit = 1 at power-on  |
| FL             | PLL lock flag, bit = 1: loop is locked  |
| NBD            | Narrow Band detector flag, bit =1 when SAWOUT level is above RF AGC take-over point   |
| AGC            | internal AGC flag, bit = 1 when internal AGC is active (level below 3V)   |
| A0, A1, A2     | digital output of the 5-level ADC (only available in TUA 6039-2)  |

**Table 10 Address selection**

| Voltage at AS   | MA1 | MA0 |
|---|-----|-----|
| $(0 \text{ to } 0.1) \times V_{CC}$                   | 0   | 0   |
| open circuit or $(0.2 \text{ to } 0.3) \times V_{CC}$ | 0   | 1   |
| $(0.4 \text{ to } 0.6) \times V_{CC}$                 | 1   | 0   |
| $(0.9 \text{ to } 1) \times V_{CC}$                   | 1   | 1   |

**Table 11 Test modes**

| Mode  | T2 | T1 | T0 | OS |
|---|----|----|----|----|
| Normal mode (XMODE = 0 <sup>1)</sup> ,<br>charge pump currents 50 $\mu$ A and 250 $\mu$ A selectable      | 0  | 0  | 0  | 0  |
| Normal mode (XMODE = 0),<br>charge pump currents 50 $\mu$ A and 250 $\mu$ A selectable (default)          | 0  | 0  | 1  | 0  |
| Normal mode (XMODE = 0),<br>CP test tristate, CP currents off, $V_T$ disabled                             | 0  | 0  | x  | 1  |
| Port test output: P0 = NB   | 0  | 1  | 0  | 0  |
| Port test output: P0 = $f_{div} / 2$ , P1 = $f_{ref}$   | 0  | 1  | 0  | 1  |
| byte AB will follow (otherwise byte BB will follow)   | 0  | 1  | 1  | 0  |
| byte AB will follow (otherwise byte BB will follow),<br>CP test tristate, CP currents off, $V_T$ disabled | 0  | 1  | 1  | 1  |
| CP test sink  | 1  | 0  | 0  | 0  |
| CP test source  | 1  | 0  | 1  | 0  |
| CP test tristate, CP currents off, $V_T$ active   | 1  | 0  | x  | 1  |
| Extended mode (XMODE = 1),<br>charge pump currents 50 $\mu$ A and 250 $\mu$ A selectable                  | 1  | 1  | 0  | 0  |
| Extended mode (XMODE = 1),<br>charge pump currents 125 $\mu$ A and 650 $\mu$ A selectable                 | 1  | 1  | 1  | 0  |
| Extended mode (XMODE = 1),<br>CP test tristate, CP currents off, $V_T$ disabled                           | 1  | 1  | x  | 1  |

1) XMODE = internal flag for extended mode

**Table 12 Reference divider ratios**

| Reference divider ratio | $f_{\text{ref}}^{1)}$ | Mode     | T2 | T1 | RSA | RSB |
|-------------------------|-----------------------|----------|----|----|-----|-----|
| 80                      | 50 kHz                | normal   | 0  | 0  | 0   | 0   |
| 128                     | 31.25 kHz             | normal   | 0  | 0  | 0   | 1   |
| 24                      | 166.67 kHz            | x        | x  | x  | 1   | 0   |
| 64                      | 62.5 kHz              | x        | x  | x  | 1   | 1   |
| 32                      | 125 kHz               | extended | 1  | 1  | 0   | 0   |
| 28                      | 142.86 kHz            | extended | 1  | 1  | 0   | 1   |

1) With a 4 MHz quartz.

**Table 13 RF AGC take-over point**

| SAW driver output level, symmetrical mode | Remark   | AL2 | AL1 | AL0 |
|---|--|-----|-----|-----|
| 115 dB $\mu$ V                            |  | 0   | 0   | 0   |
| 115 dB $\mu$ V                            |  | 0   | 0   | 1   |
| 112 dB $\mu$ V                            | default mode at POR                                    | 0   | 1   | 0   |
| 109 dB $\mu$ V                            |  | 0   | 1   | 1   |
| 106 dB $\mu$ V                            |  | 1   | 0   | 0   |
| 103 dB $\mu$ V                            |  | 1   | 0   | 1   |
| $I_{\text{RFAGC}} = 0$                    | External RF AGC <sup>1)</sup><br>Disable RF AGC buffer | 1   | 1   | 0   |
| $V_{\text{RFAGC}} = \text{high}$          | Disabled <sup>2)</sup>                                 | 1   | 1   | 1   |

1) The RF AGC detector is disabled. Both the sinking and sourcing current from the IC is disabled. The RF AGC output goes into a high impedance state and an external RF AGC source can be connected in parallel and will not be influenced. The RF AGC buffer is disabled.

2) The RF AGC detector is disabled,  $V_{\text{RFAGC}}$  is set to high voltage  $V_{\text{CC}} - V_{\text{CE,sat}}$  for  $V_{\text{CC}} < 4 \text{ V}$  or  $V_{\text{RFAGC}} = 3.7 \text{ V}$  for  $V_{\text{CC}} > 4 \text{ V}$ .

**Table 14 A to D converter levels<sup>1)</sup>**

| Voltage at ADC <sup>1)</sup>    | A2 | A1 | A0 |
|---------------------------------|----|----|----|
| (0 to 0.15) * V <sub>CC</sub>   | 0  | 0  | 0  |
| (0.15 to 0.3) * V <sub>CC</sub> | 0  | 0  | 1  |
| (0.3 to 0.45) * V <sub>CC</sub> | 0  | 1  | 0  |
| (0.45 to 0.6) * V <sub>CC</sub> | 0  | 1  | 1  |
| (0.6 to 1) * V <sub>CC</sub>    | 1  | 0  | 0  |

1) No erratic codes in the transition.

**Table 15 Charge pump current**

| Charge pump current | Mode     | CP | T2 | T1 | T0              |
|---------------------|----------|----|----|----|-----------------|
| 50 µA               | normal   | 0  | 0  | 0  | x <sup>1)</sup> |
| 250 µA (default)    |          | 1  |    |    | x               |
| 50 µA               | extended | 0  | 1  | 1  | 0               |
| 125 µA              |          | 0  |    |    | 1               |
| 250 µA              |          | 1  |    |    | 0               |
| 650 µA              |          | 1  |    |    | 1               |

1) x = don't care.

**Table 16 Internal band selection**

| Band            | Mixer                             | Oscillator                        |
|-----------------|-----------------------------------|-----------------------------------|
| LOW             | P0, $\overline{P1}$ <sup>1)</sup> | P0, $\overline{P1}$               |
| MID             | P1, $\overline{P0}$               | P1, $\overline{P0}$               |
| HIGH (default)  | $\overline{P0}$ , $\overline{P1}$ | $\overline{P0}$ , $\overline{P1}$ |
| Power down mode | P0, P1                            | P0, P1                            |

1) Means: (P0 AND NOT P1); that is: LOW mixer is switched on if (P0 = 1 and P1 = 0).

1) ADC function is only available in TUA 6039-2.

**Table 17 Defaults at power-on reset**

| Name            | Byte | Bits |                 |      |      |      |      |      |       |
|-----------------|------|------|-----------------|------|------|------|------|------|-------|
|                 |      | MSB  | bit6            | bit5 | bit4 | bit3 | bit2 | bit1 | LSB   |
| Write Data      |      |      |                 |      |      |      |      |      |       |
| Address Byte    | ADB  | 1    | 1               | 0    | 0    | 0    | MA1  | MA0  | R/W=0 |
| Divider byte 1  | DB1  | 0    | x <sup>1)</sup> | x    | x    | x    | x    | x    | x     |
| Divider byte 2  | DB2  | x    | x               | x    | x    | x    | x    | x    | x     |
| Control byte    | CB   | 1    | 1               | 0    | 0    | 1    | 0    | 0    | 1     |
| Bandswitch byte | BB   | 0    | 0               | 0    | 0    | 0    | 0    | 0    | 0     |
| Auxiliary byte  | AB   | 0    | 0               | 1    | 0    | 0    | 0    | 0    | 0     |

1) x = don't care.

**Table 18 Description of modes**

| Mode     | Description  |
|----------|--|
| normal   | Reference divider ratios 24, 64, <b>80</b> , <b>128</b> selectable.<br>Charge pump currents 50, 250 $\mu$ A selectable.<br>Auxiliary byte to follow Control byte (T2 = 0, T1 = 1, T0 = 1),<br>otherwise Bandswitch byte to follow Control byte.                          |
| extended | Reference divider ratios 24, <b>28</b> , <b>32</b> , 64 selectable.<br>Charge pump currents 50, <b>125</b> , 250, <b>650</b> $\mu$ A selectable.<br>Auxiliary byte to follow Control byte (T2 = 0, T1 = 1, T0 = 1),<br>otherwise Bandswitch byte to follow Control byte. |

### 5.3 I<sup>2</sup>C Bus Timing Diagram

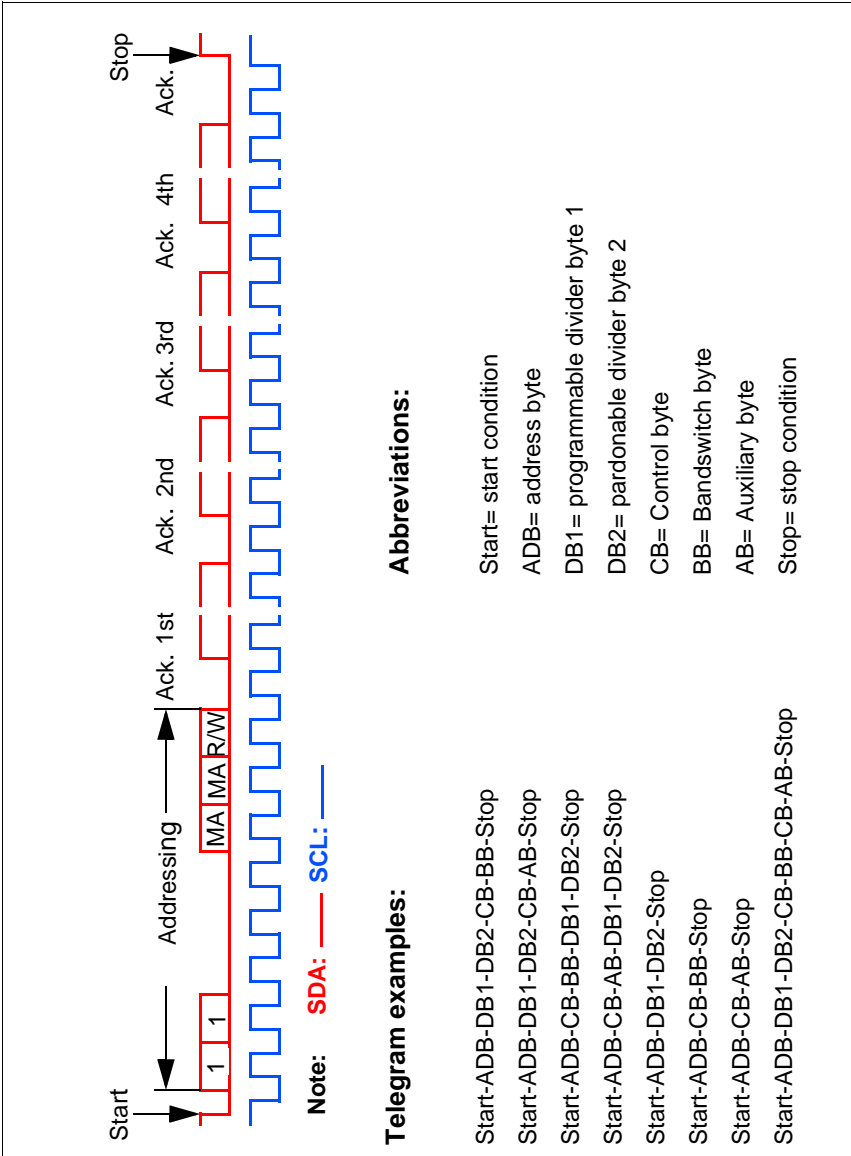
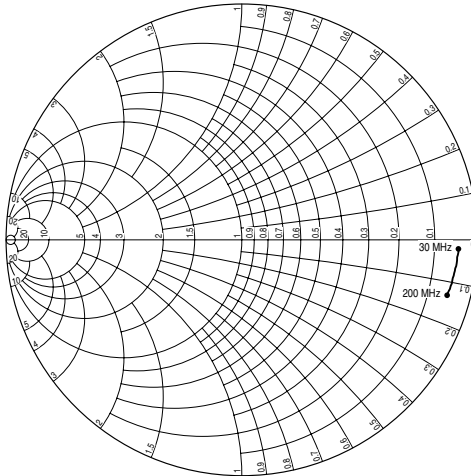


Figure 13 I<sup>2</sup>C Bus Timing Diagram

## 5.4 Electrical Diagrams

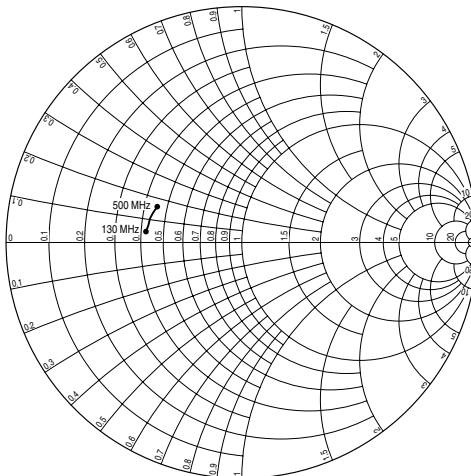
### 5.4.1 Input admittance (S11) of the LOW band mixer (30 to 200 MHz)

$Y_0 = 20 \text{ mA/V}$



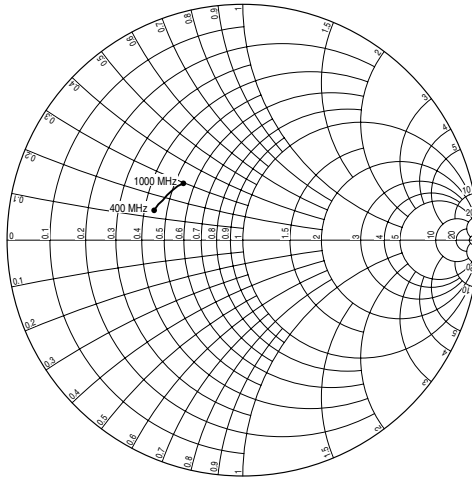
### 5.4.2 Input impedance (S11) of the MID band mixer (130 to 500 MHz)

$Z_0 = 50 \Omega$



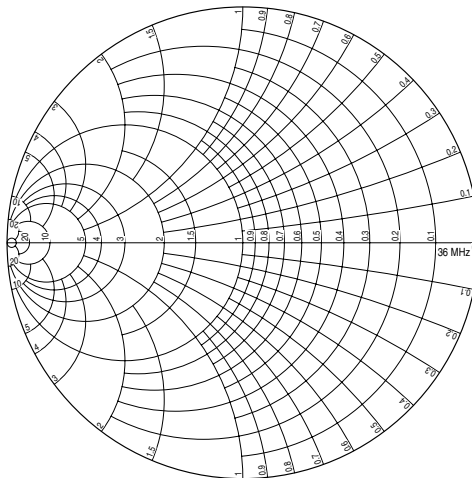
**5.4.3 Input impedance (S11) of the HIGH band mixer (400 to 1000 MHz)**

$Z_0 = 50 \Omega$



**5.4.4 Output admittance (S22) of the of the mixers (30 to 60 MHz)**

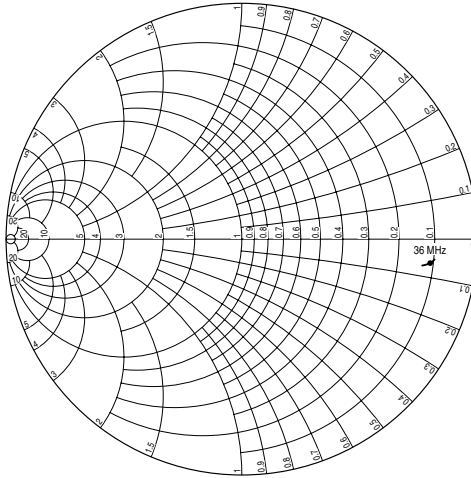
$Y_0 = 20 \text{ mA/V}$





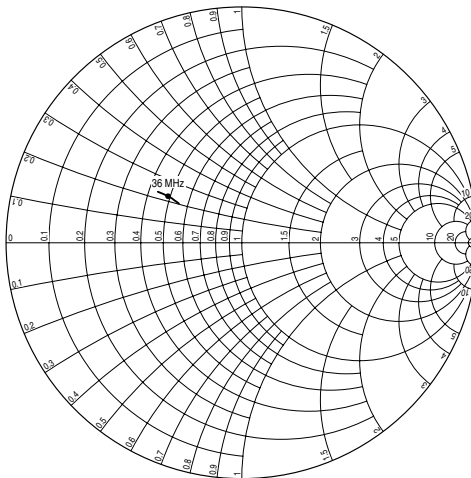
**5.4.5 Input admittance (S11) of the SAW filter driver (30 to 60 MHz)**

$Y_0 = 20 \text{ mA/V}$



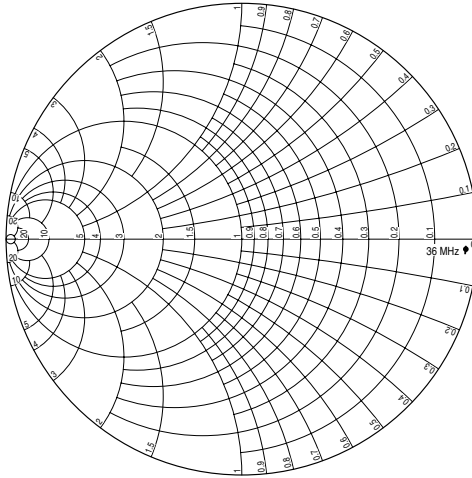
**5.4.6 Output impedance (S22) of the SAW filter driver (30 to 60 MHz)**

$Z_0 = 50 \Omega$



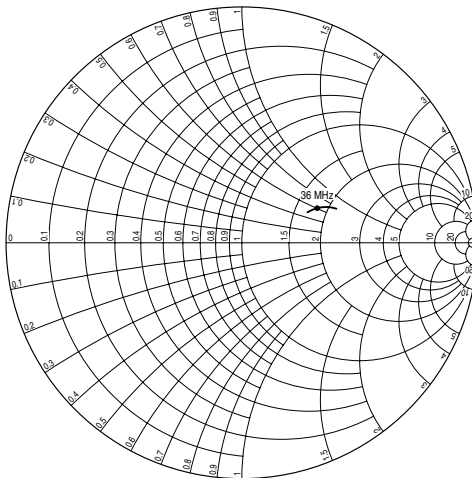
**5.4.7 Input admittance (S11) of the IF AGC amplifier (30 to 60 MHz)**

$Y_0 = 20 \text{ mA/V}$



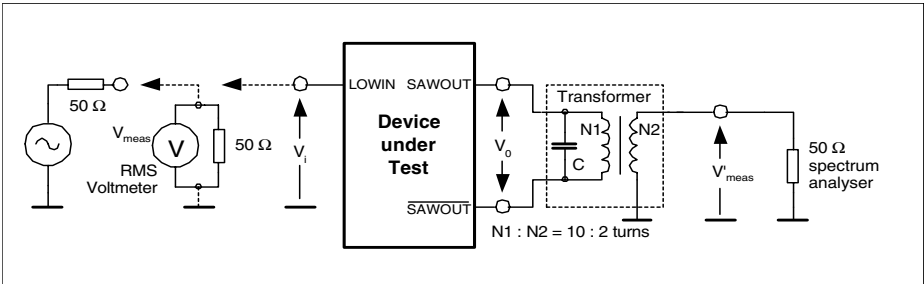
**5.4.8 Output impedance (S22) of the IF AGC amplifier (30 to 60 MHz)**

$Z_0 = 50 \Omega$



## 5.5 Measurement Circuits

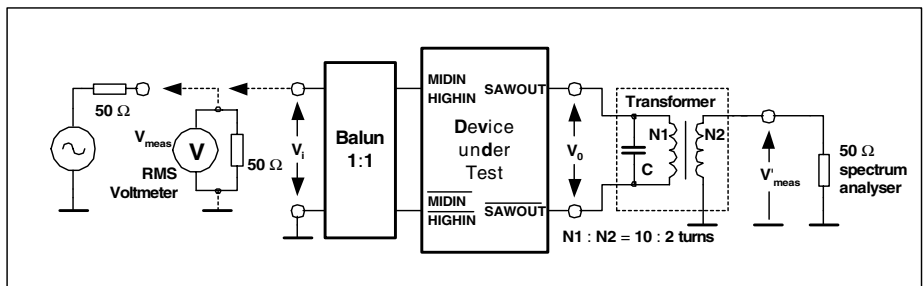
### 5.5.1 Gain ( $G_V$ ) measurement in LOW band



**Figure 14** Gain ( $G_V$ ) measurement in LOW band

- $Z_i \gg 50 \Omega \Rightarrow V_i = 2 \times V_{\text{meas}} = 80 \text{ dB}\mu\text{V}$
- $V_i = V_{\text{meas}} + 6\text{dB} = 80 \text{ dB}\mu\text{V}$
- $V_0 = V'_{\text{meas}} + 17 \text{ dB}$  (transformer ratio  $N1:N2$  and transformer loss)
- $G_V = 20 \log(V_0 / V_i)$

### 5.5.2 Gain ( $G_V$ ) measurement in MID and HIGH bands



**Figure 15** Gain ( $G_V$ ) measurement in MID and HIGH bands

- $V_i = V_{\text{meas}} = 70 \text{ dB}\mu\text{V}$
- $V_0 = V'_{\text{meas}} + 17 \text{ dB}$  (transformer ratio  $N1:N2$  and transformer loss)
- $G_V = 20 \log(V_0 / V_i) + 1 \text{ dB}$  (1 dB = insertion loss of balun)

### 5.5.3 Matching circuit for optimum noise figure in LOW band

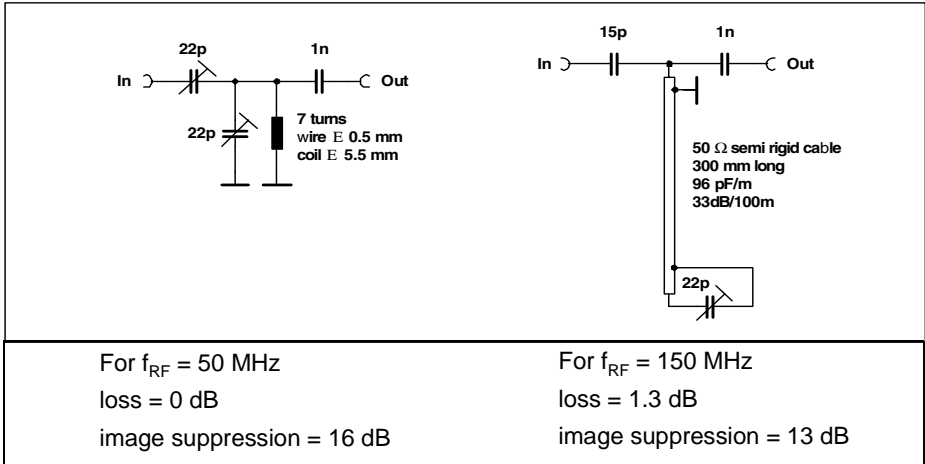


Figure 16 Matching circuit for optimum noise figure in LOW band

### 5.5.4 Noise figure (NF) measurement in LOW band

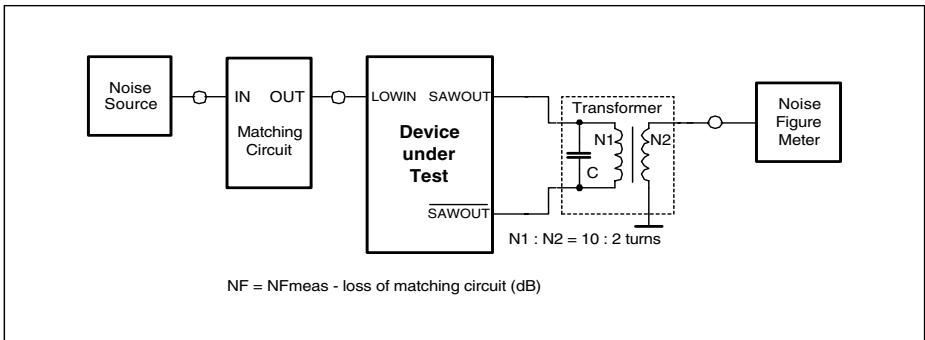


Figure 17 Noise figure (NF) measurement in LOW band

### 5.5.5 Noise figure (NF) measurement in MID and HIGH bands

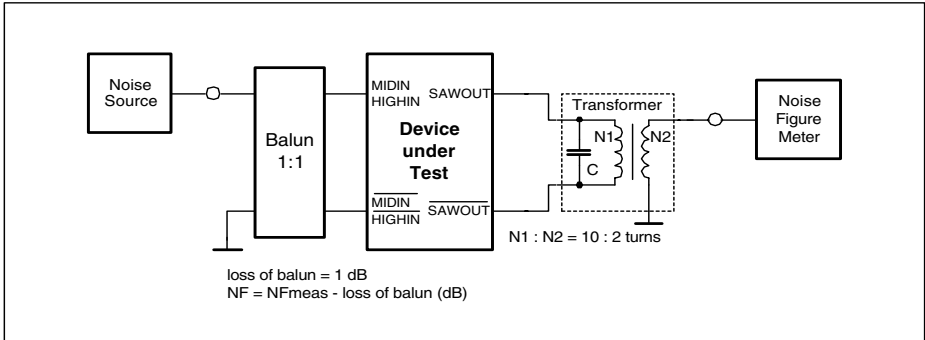


Figure 18 Noise figure (NF) measurement in MID and HIGH bands

### 5.5.6 Cross modulation measurement in LOW band

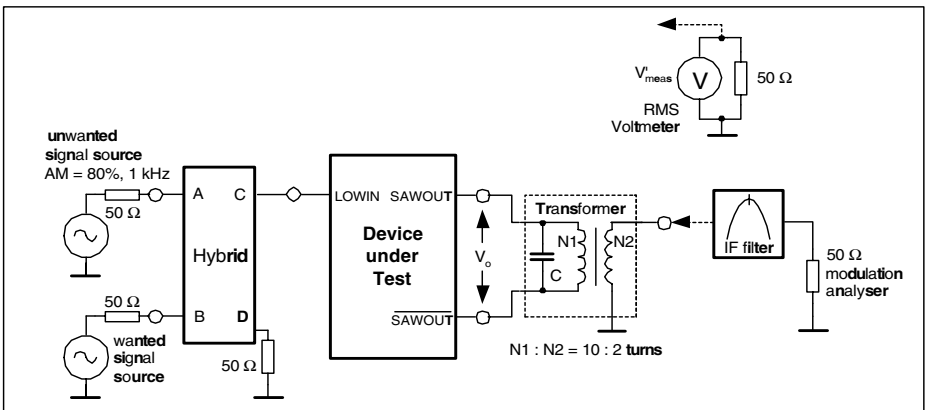
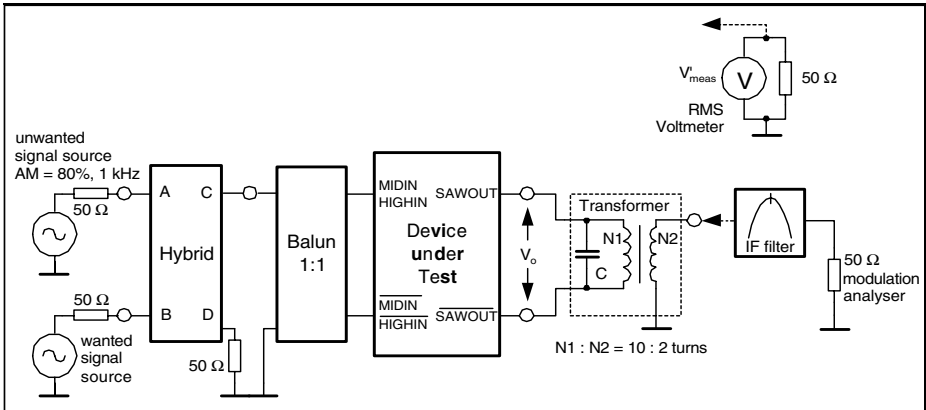


Figure 19 Cross modulation measurement in LOW band

- $V'_{\text{meas}} = V_0 - 17 \text{ dB}$  (transformer ratio  $N1:N2$  and transformer loss)
- wanted output signal at  $f_{\text{pix}}$ ,  $V_0 = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at  $f_{\text{snd}}$

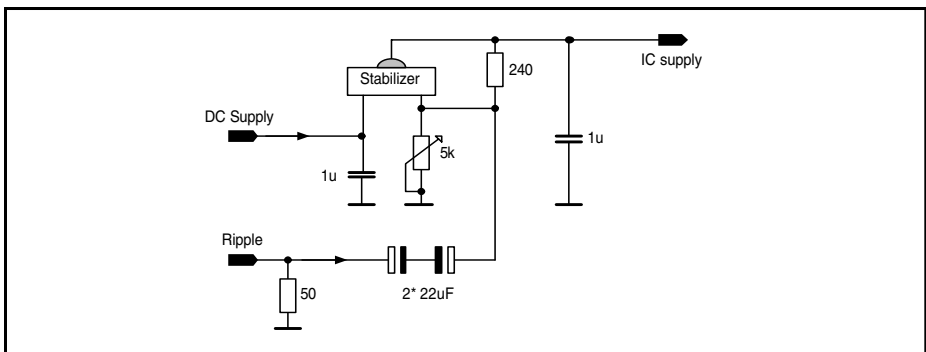
### 5.5.7 Cross modulation measurement in MID and HIGH bands



**Figure 20 Cross modulation measurement in MID and HIGH bands**

- $V'_{meas} = V_o - 17 \text{ dB}$  (transformer ratio  $N1:N2$  and transformer loss)
- wanted output signal at  $f_{pix}$ ,  $V_o = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at  $f_{snd}$

### 5.5.8 Ripple susceptibility (RSC) measurement



**Figure 21 Ripple susceptibility measurement**

## 6 Package VQFN-48

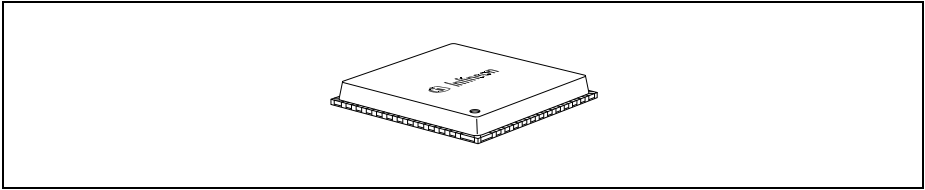


Figure 22 PG-VQFN-48 Vignette

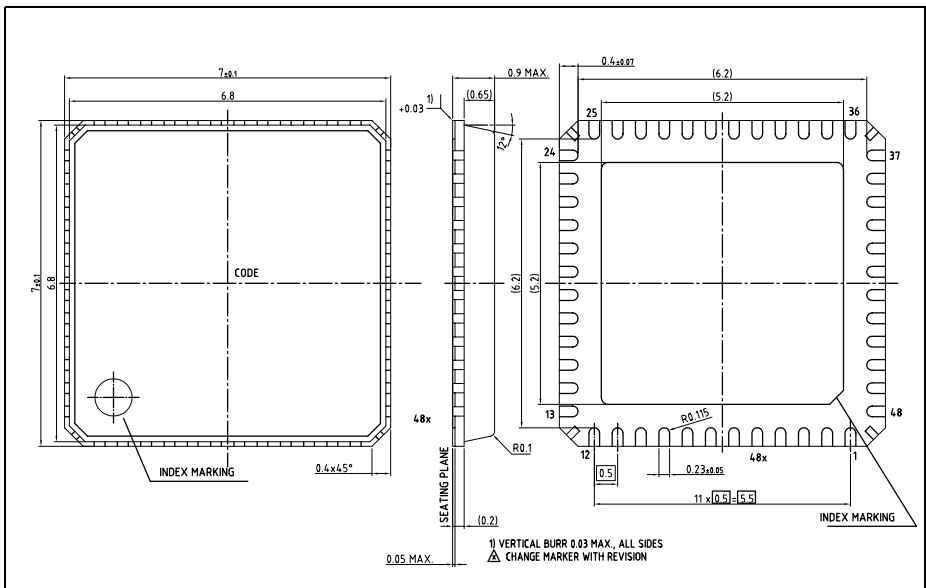


Figure 23 PG-VQFN-48 Outline Drawing

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