CY54/74FCT2543T
8-BIT LATCHED TRANSCEIVER

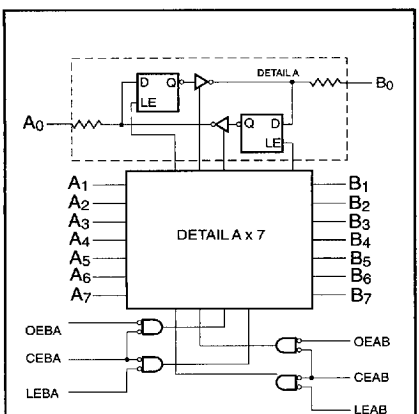
FEATURES

- Function and Pinout Compatible with the FCT and F Logic
- FCT-C speed at 5.3ns max. (Com'l) FCT-A speed at 6.5ns max. (Com'l)
- R25Ω output series resistors to reduce transmission line reflection noise
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 12 mA Sink Current (Com'l), 12 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)
- Separate Controls for Data Flow in Each Direction
- Back to Back Latches for Storage

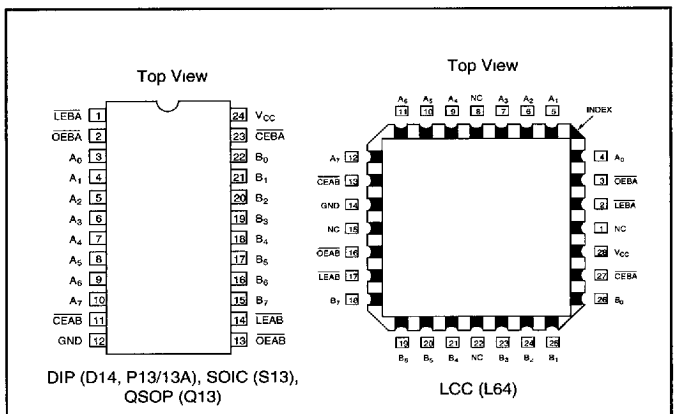
DESCRIPTION

The 'FCT2543T Octal Registered Transceiver contains two sets of eight D-type latches. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) controls permit each latch set to have independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW to enter data from A0–A7 or to take data from B0–B7, as indicated in the truth table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in storage mode and their output no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$ and $\overline{OEAB}$ inputs. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The 'FCT2543T can be used to replace the 'FCT543T to reduce noise in an existing design.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS[1,2]

Sym	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[5]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_{IH}	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current	Except I/O Pins			5	µA	MAX	V_{IN} = 2.7V
		I/O Pins			15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current	Except I/O Pins			–5	µA	MAX	V_{IN} = 0.5V
		I/O Pins			–15	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				15	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last
5. This parameter is guaranteed but not tested

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ.[6]	Max.	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[7], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[8]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{CEAB}$ + $\overline{OEAB}$ = Low, Outputs Open, $\overline{CEAB}$ = High, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[10]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[9]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[9]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND

Notes:

6. Typical values are at V_{CC} = 5.0V, +25°C ambient.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_1 = Input Frequency
    N_1 = Number of Inputs at f_1
    All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE FOR A-TO-B (Symmetric with B-to-A)

Inputs			Latch Status	Outputs 'FCT2543T
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B0–B7
H	–	–	Storing	High Z
–	H	–	Storing	–
–	–	H	–	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs

* = Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
– = Don't Care or Irrelevant
A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$

AC CHARACTERISTICS

Sym.	Parameter	'FCT2543T				'FCT2543AT				'FCT2543CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	2.5	6.1	2.5	5.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n $\overline{LEAB}$ to B_n	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	2.5	8.0	2.5	7.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	2.0	9.0	2.0	8.0	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	2.0	7.5	2.0	6.5	ns	1,7,8

AC OPERATING REQUIREMENTS

Sym.	Parameter	'FCT2543T				'FCT2543AT				'FCT2543CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_s (H) t_s (L)	Set-up Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	9
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	9
t_w	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	6

Note:
11. Minimum limits are guaranteed on Propagation Delays.
*Refer to the 'Parameter Measurement Information' section of this book.

ORDERING INFORMATION