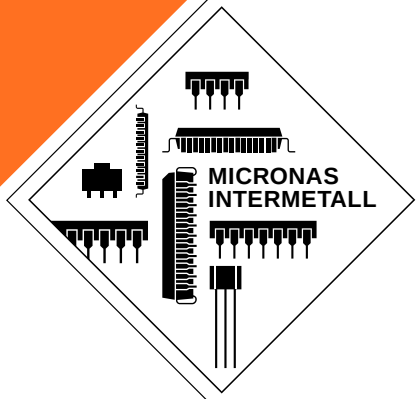


PRELIMINARY DATA SHEET

DDP 3300 A
Single-Chip Display and Deflection Processor

Edition June 19, 1996
6251-421-1PD

MICRONAS
INTERMETALL

Contents

Contents, continued

DDP 3300 A, Display and Deflection Processor 50/60 Hz (68-pin PLCC or 64-pin PSDIP Package)

Note:
Revision bars indicate significant changes to the previous version, ed. 6251-421-1AI, Advance Information, dated Feb. 9, 1996.

1. Introduction

The DDP 3300 A is a single-chip digital display and deflection processor in 0.8 µm CMOS technology for high quality back-end applications in 50/60 Hz TV sets with 4:3 or 16:9 picture tubes. It can be combined with members of the DIGIT 3000 IC family (VPC 3200 A, VPC 3201 B, TPU 3040) or it can be used with third party products. One IC contains the entire video component and deflection processing and forms the heart of a modern color TV. Its performance and complexity allow the user to standardize his product development. Hardware and software applications can profit from the modularity, as well as manufacturing, system support or maintenance. The main features are

– single 5 V power supply

– low cost, high performance all digital video processing

– black-level expander

– dynamic peaking

– soft limiter (gamma correction)

– color transient improvement

– programmable RGB matrix

– scan velocity modulation output

– picture frame generator

– additional analog RGB/fastblank input

– Prio interface

– various digital interfaces

– high performance H/V deflection

– separate ADC for tube measurements

1.1. System Architecture

Open architecture is the key word to the new DSP generation. Flexible standard building blocks have been defined that offer continuity and transparency of the entire system. Two main modules were defined:

– Video Processor and

– Display and Deflection Processor.

They were designed as separate ICs. Their partitioning permits a variety of IC configurations with the aim to satisfy the particular requirements of different applications. Both, analog and digital interfaces, support state-of-the art TV receivers as well as other environments. Fig. 1–1 shows the block diagram of the single-chip Display and Deflection Processor.

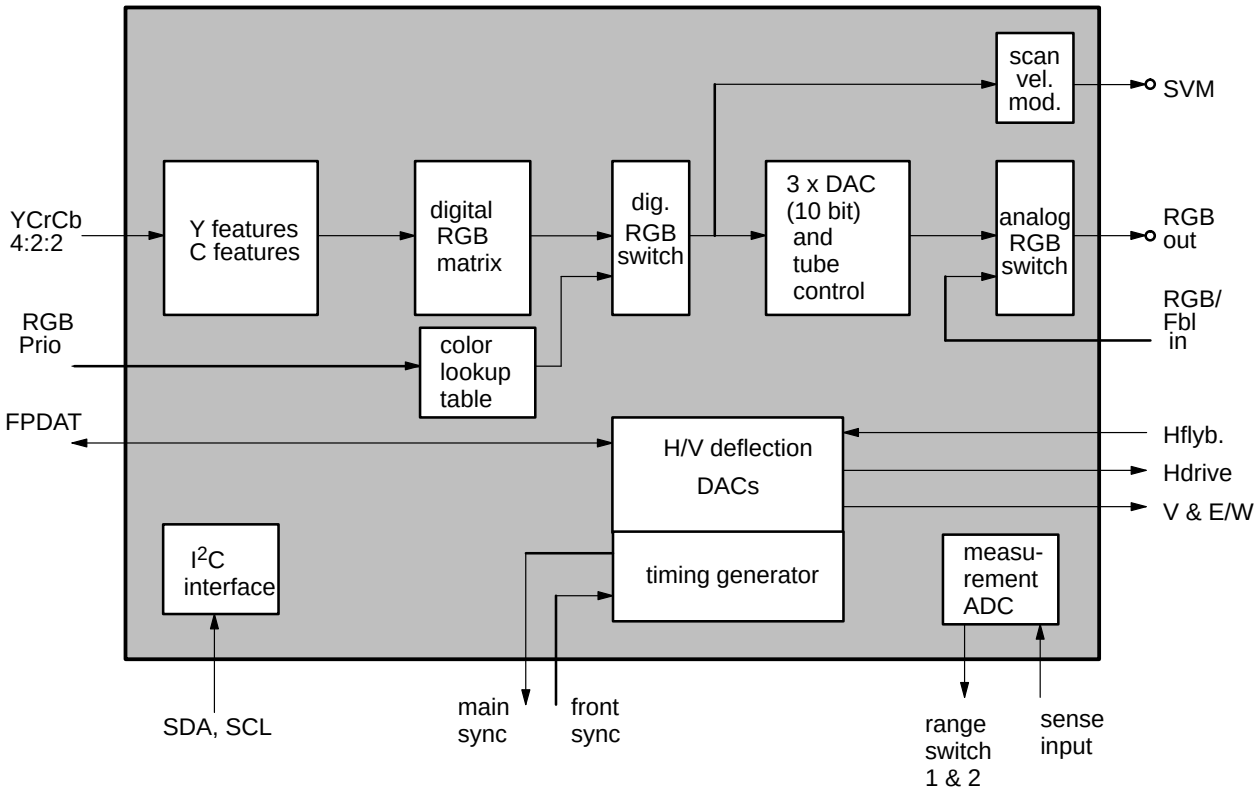


Fig. 1–1: Display and Deflection Processor

1.2. DDP Applications

Fig. 1–2 depicts several DDP applications. Since the DDP functions as a video back-end, it must be complemented with additional functionality to form a complete TV set.

The DDP 3310 B will be a further development of the DDP 3300 A. It is targeted for a system with a horizontal frequency of 32 kHz and a vertical frequency of 100 or 120 Hz.

The VPC3210A/3211B processes all worldwide analog video signals (including the European PALplus) and allows nonlinear Panorama aspect ratio conversion. Thus 4:3 and 16:9 systems can easily be configured by software. The aspect ratio scaling is also used as a sample rate converter to provide a line-locked digital component output bus (YCrCb) compliant to ITUR–601. All video processing and line-locked clock/data generation is derived from a single 20.25 MHz crystal. An optional adaptive 2-line combfilter (VPC3211B) performs Y/C separation for PAL and NTSC and all of their substandards. Both versions of the VPC are plug-in compatible.

The CIP 3250 A provides a high-quality analog RGB interface with character insertion capability. This allows appropriate processing of external sources such as MPEG2 set-top boxes in transparent (4:2:2) quality. Furthermore, it translates RGB/Fastblank signals to the common digital video bus and makes those signals available for 100 Hz processing. In some European countries (Italy), this feature is mandatory.

The IP indicates memory based image processing, such as scan rate conversion, vertical processing (Zoom), or PAL+ reconstruction.
Examples:

– Europe: 15 kHz/50 Hz → 32 kHz/100 Hz interlaced

– US: 15 kHz/60 Hz → 31 kHz/60 Hz non-interlaced

Note that the VPC supports memory based applications through line-locked clocks, syncs, and data. CIP may run either with the native DIGIT3000 clock but also with a line-locked clock system.

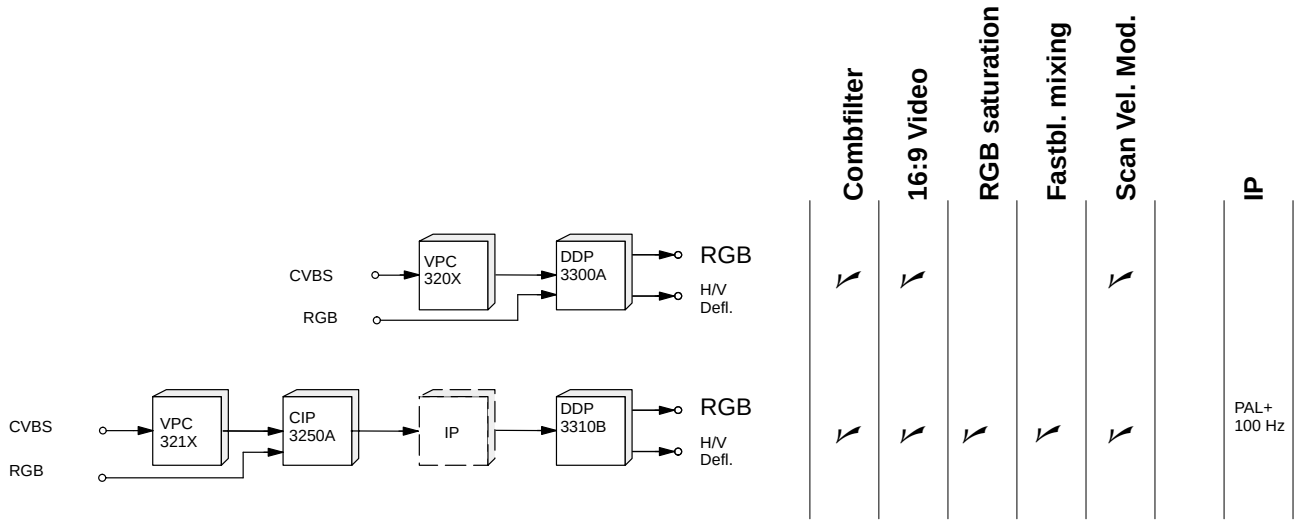


Fig. 1–2: DDP 3300 A Applications

1.3. Digital Video Interfaces

The digital video interface allows input of digital data in YC_rC_b format on the YC_rC_b data bus. The orthogonal data structure of this bus is the ideal interface point to external data sources and sinks. Furthermore, a host of formats are supported, e.g. support of level-2 teletext or the priority pixel bus concept.

Figure 1–3 shows all available digital interfaces:

YC_rC_b 16 bit 4:2:2
OSD 5 bit 4:4:4
PRIO 3 bit, source selection

The YCrCb bus is used for video input. The OSD interface is used for insertion of a Teletext or OSD picture. The priority bus allows to mix up to 8 sources on the YC_rC_b/OSD bus.

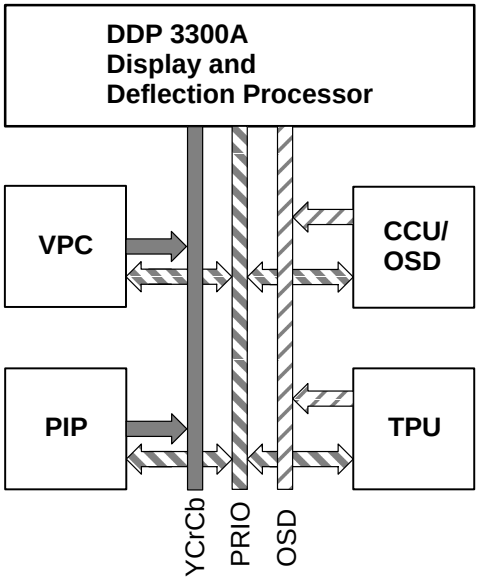


Fig. 1–3: DDP video interfaces

1.3.1. Picture Bus Interface

The video bus

The video bus format between all DIGIT3000 ICs is YCrCb with 20.25 Msamples/s. Only active video is transferred, synchronized by the system main sync signal (MSY), which indicates the start of valid data for each scan line. The number of active samples per line is 1080 for all standards (525 and 625).

Via the MSY line, serial data is transferred which contains information on the main picture, such as current line number, odd/even field etc. It is generated by the deflection circuitry and represents the orthogonal timebase for the entire system.

Feature ICs (e.g. PIP) will be synchronized to the main YC_rC_b bus. Digital insertion (boxing) is controlled by a priority system.

1.3.2. Digital OSD Interface

Digital OSD from text or on-screen-display is connected via the Picture bus. The OSD signal is 5 bits wide. The OSD signals are not subject to any post-filtering. The OSD signal provides 3-bit RGB (one bit per color), the 4th bit allows to display of half contrast colors. The 5^{th} bit enables a programmable color-look-up table with 16 entries and 4-bit resolution per color. This allows the support of a World System Teletext level-2 color display. Display contrast for OSD data can be adjusted separately by three contrast multipliers.

1.3.3. Priority Interface

Up to eight digital YC_rC_b or OSD sources (main decoder, PIP, OSD, text, etc.) may be selected in real-time by means of a 3-bit priority bus. Thus, a pixelwise bus arbitration and source switching is possible. It is essential that all YC_rC_b-sources are synchronous and orthogonal.

In general, each source (= master) has its own YC_rC_b bus request. This bus request may either be software or hardware-controlled, i.e. by a fast blank signal. Data collision is avoided by a bus arbiter that provides the individual bus acknowledge in accordance to a user-defined priority.

Each master sends a bus request with his individual priority ID onto the Prio-bus and immediately reads back the bus status. Only in case of positive arbitration (send-Prio-ID = read-Prio-ID) the bus acknowledge becomes active and the data is sent.

This treatment has many features that have impact on the appearance of a TV picture:

– real-time bus arbitration (PIP, OSD...)

– priority configuration by software

– different coefficients for different sources

2. Functional Description

2.1. Display Part

In the display part the conversion from digital YC_rC_b to analog RGB is carried out. A block diagram is shown in Figure 2–9. In the luminance processing, path contrast and brightness adjustments and a variety of features, such as black level expansion, dynamic peaking and soft limiting, are provided. In the chrominance path, the C_rC_b signals are converted to 20.25 MHz sampling rate and filtered by a color transient improvement circuit. The YC_rC_b signals are converted by a programmable matrix to RGB color space.

The signals inserted via the YC_rC_b bus are identified by their respective priority. The display processor provides separate control settings for two pictures, i.e. different coefficients for a 'main' and a 'side' picture.

The digital OSD insertion circuit allows the insertion of a 5-bit OSD signal. The color space for this signal is controlled by a partially programmable color look-up table (CLUT) and contrast adjustment.

The OSD signals and the display clock are synchronized to the horizontal flyback. For the display clock, a gate delay phase shifter is used. In the analog backend, three 10-bit digital-to-analog converters provide the analog output signals.

2.1.1. Luma Input

The luminance input is 8 bit wide. If noise shaping was applied to the luminance signal, a notch filter for an LSB shaping signal at 10.125 MHz reconstructs the real LSB. This increases the signal resolution to 9-bit data. The VPC 32XX A supports this noise shaping.

After this filter (gain = 2) from the 9-bit signal an offset of 32 is subtracted to shift the black level to zero. This assumes the black level of the input signal to be at 16 (ITUR 601 standard).

2.1.2. Luma Contrast Adjustment

The 9-bit luminance signal is multiplied by a factor of 0 ... 2 in 64 steps. An 11-bit output signal is used to increase the accuracy of the luma signal. The contrast can be adjusted separately for main picture and side picture.

2.1.3. Black Level Expander

The black level expander enhances the contrast of the picture. Therefore the luminance signal is modified with an adjustable, non-linear function. Dark areas of the picture are changed to black, while bright areas remain unchanged. The advantage of this black level expander is that the black expansion is performed only if it will be most noticeable to the viewer.

The black level expander works adaptively. Depending on the measured amplitudes 'L_{min}' and 'L_{max}' of the low-pass-filtered luminance and an adjustable coefficient BTLT, a tilt point 'L_t' is being established by

$$L_t = L_{min} + BTLT\ (L_{max} - L_{min}).$$

Above this value there is no expansion, while all luminance values below this point are expanded according to:

$$L_{out} = L_{in} + BAM\ (L_{in} - L_t)$$

A second threshold, L_{tr}, can be programmed, above which there is no expansion. The characteristics of the black level expander are shown in Fig. 2–1 and Fig. 2–2.

The tilt point L_t is a function of the dynamic range of the video signal. Thus, the black level expansion is only performed when the video signal has a large dynamic range. Otherwise, the expansion to black is zero. This allows the correction of the characteristics of the picture tube.

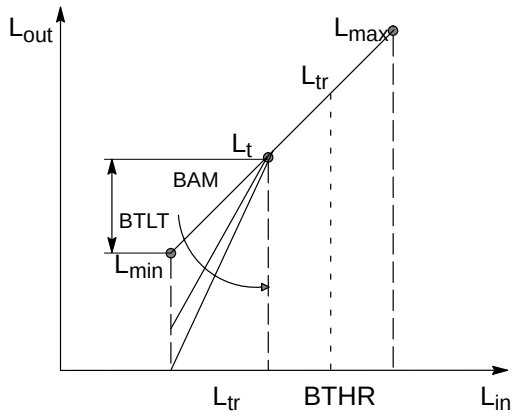


Fig. 2–1: Characteristics of the black level expander

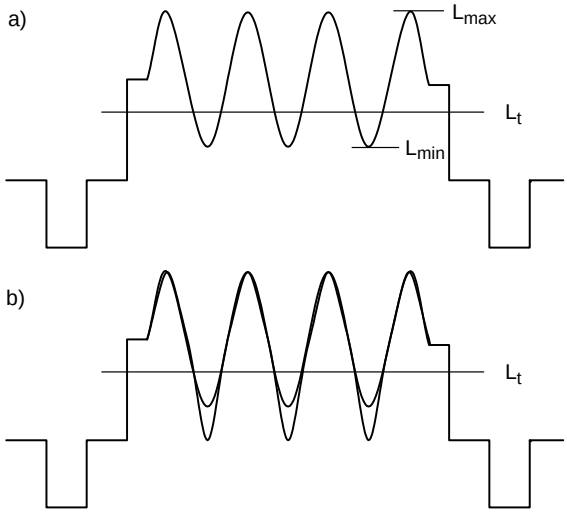


Fig. 2–2: Black-level-expansion
a) luminance input
b) luminance input and output

2.1.4. Dynamic Peaking

Especially with decoded composite signals and notch filter luminance separation, as input signals, it is necessary to improve the luminance frequency characteristics. With transparent, high-bandwidth signals, it is sometimes desirable to soften the image.

In the DDP 3300 A, the luma response is improved by ‘dynamic’ peaking. The algorithm has been optimized regarding step and frequency response. It adapts to the amplitude of the high frequency part. Small AC amplitudes are processed, while large AC amplitudes stay nearly unmodified.

The dynamic range can be adjusted from −14 to +14 dB for small high frequency signals. There is separate adjustment for signal overshoot and for signal undershoot. For large signals, the dynamic range is limited by a non-linear function that does not create any visible alias components. The peaking can be switched over to “softening” by inverting the peaking term by software.

The center frequency of the peaking filter is switchable from 2.5 MHz to 3.2 MHz. For S-VHS and for notch filter color decoding, the total system frequency responses for both PAL and NTSC are shown in figure 2–4.

Transients, produced by the dynamic peaking when switching video source signals, can be suppressed via the priority bus.

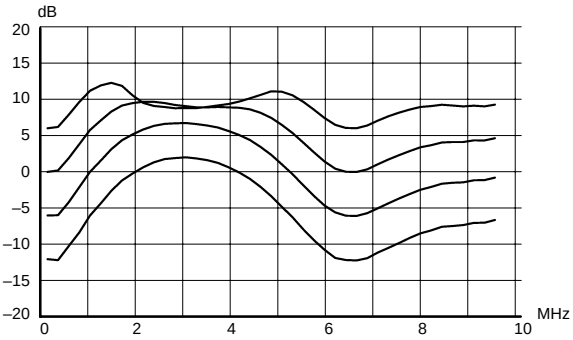


Fig. 2–3: Dynamic peaking frequency response

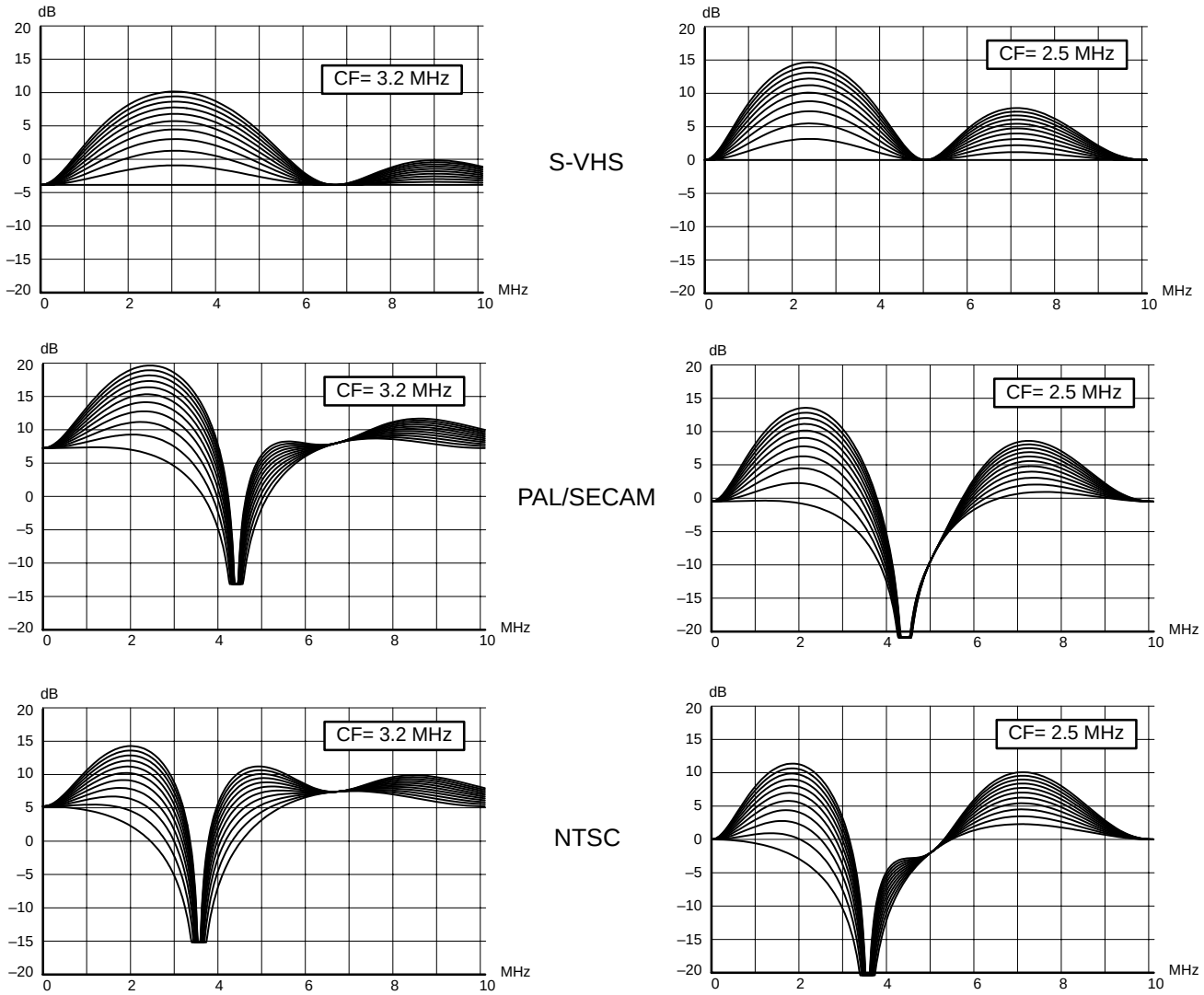


Fig. 2–4: Total frequency response for peaking filter and S-VHS, PAL, NTSC

2.1.5. Digital Brightness Adjustment

The DC-level of the luminance signal can be adjusted by adding an 8-bit number in the luminance signal path in front of the softlimiter.

With a contrast adjustment of 32 (gain = 1) the signal can be shifted by ± 100%. After the brightness addition, the negative going signals are limited to zero. It is desirable to keep a small positive offset with the signal to prevent undershoots produced by the peaking from being cut. The digital brightness adjustment is separate for main and side picture.

2.1.6. Soft Limiter

The dynamic range of the processed luma signal must be limited to prevent the CRT from overload. An appropriate headroom for contrast, peaking and brightness can be adjusted by the TV manufacturer according to the CRT characteristics. All signals above this limit will be 'soft'-clipped. A characteristic diagram of the soft limiter is shown in Fig. 2–5. The total limiter consists of three parts:

Part 1 includes adjustable tilt point and gain. The gain before the tilt value is 1. Above the tilt value, a part (0...15/16) of the input signal is subtracted from the input signal itself. Therefore the gain is adjustable from 16/16 to 1/16, when the slope value varies from 0 to 15. The tilt value can be adjusted from 0 to 511.

Part 2 has the same characteristics as part 1. The subtracting part is also relative to the input signal, so the total differential gain will become negative if the sum of slope 1 and slope 2 is greater than 16 and the input signal is above the both tilt values (see characteristics).

Finally, the output signal of the soft limiter will be clipped by a hard limiter adjustable from 256 to 511.

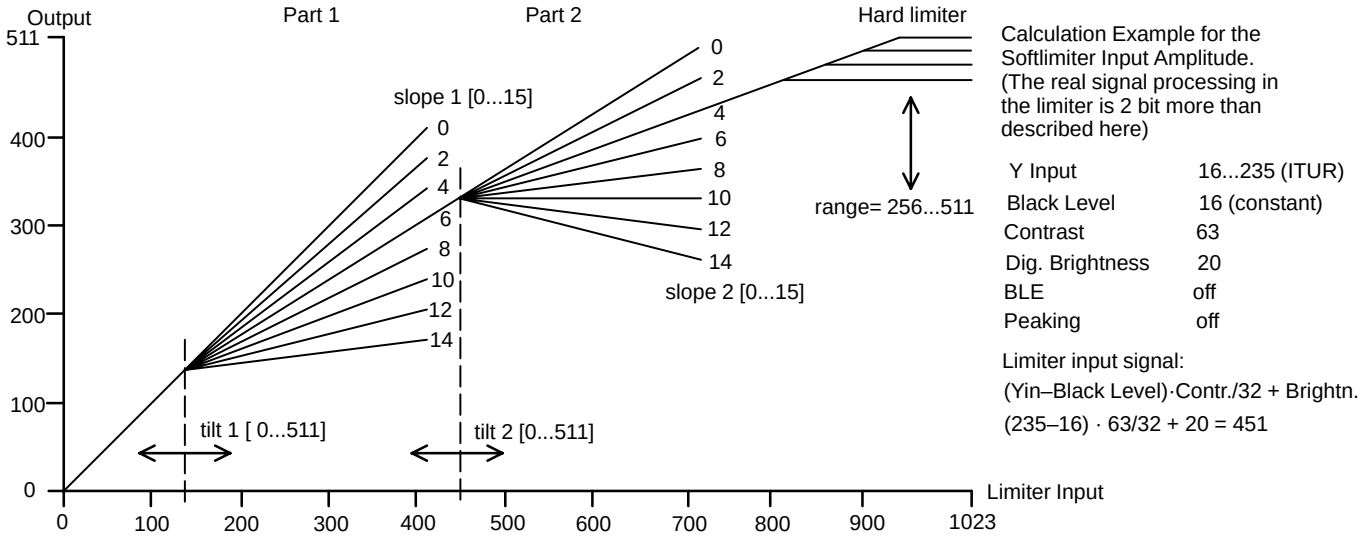


Fig. 2–5: Characteristic of soft limiter a and b and hard limiter

2.1.7. Chroma Input

The chroma input signal is typically a multiplexed C_R and C_B signal in 8-bit two's complement code. It can be switched between normal or inverted signal and between two's complement or binary offset (straight binary) code. Also the delay can be adjusted in 5 steps within a range of ± 2 clock periods.

2.1.8. Chroma Interpolation

A linear phase interpolator is used to convert the chroma sampling rate from 10.125 MHz (4:2:2) to 20.25 MHz (4:4:4). The frequency response of the interpolator is shown in Fig. 2–6. All further processing is carried out at the full sampling rate.

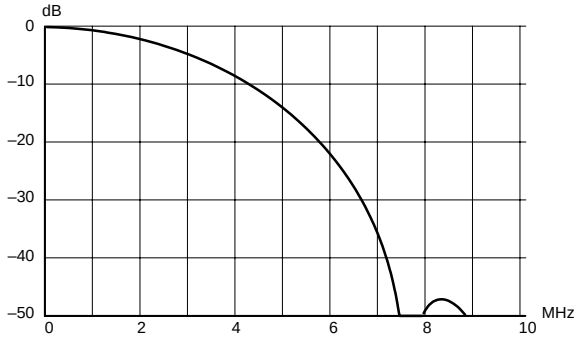
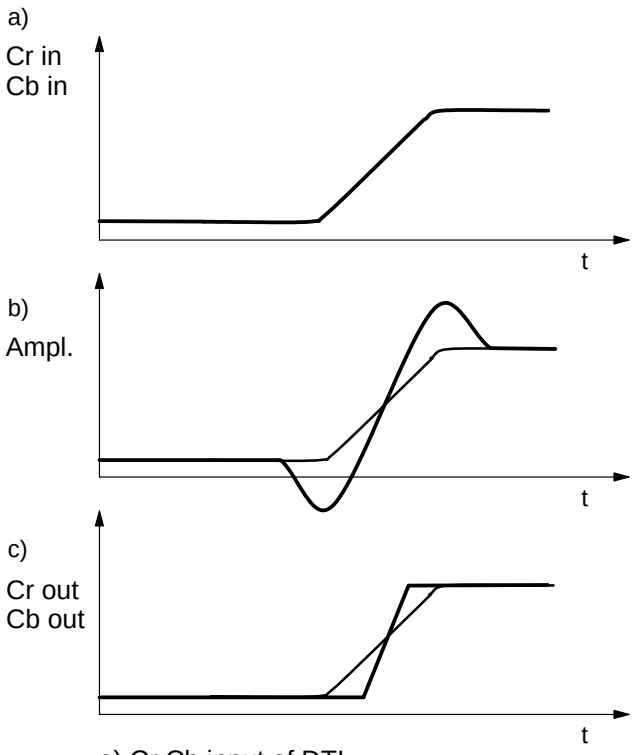


Fig. 2–6: Frequency response of the chroma interpolation filter

2.1.9. Chroma Transient Improvement

The intention of this block is to enhance the chroma resolution. A correction signal is calculated by differentiation of the color difference signals. The differentiation can be selected according to the signal bandwidth, e.g. for PAL/NTSC/SECAM or digital component signals, respectively. The amplitude of the correction signal is adjustable. Small noise amplitudes in the correction signal are suppressed by an adjustable coring circuit. To eliminate 'wrong colors', which are caused by over and undershoots at the chroma transition, the sharpened chroma signals are limited to a proper value automatically.



a) Cr Cb input of DTI
b) Cr Cb input + Correction signal
c) sharpened and limited Cr Cb

Fig. 2–7: Digital Color Transient Improvement

2.1.10. Inverse Matrix

A 6-multiplier matrix transcodes the Cr and Cb signals to R–Y, B–Y, and G–Y. The multipliers are also used to adjust color saturation in the range of 0 to 2. The coefficients are signed and have a resolution of 9 bits. There are separate matrix coefficients for main and side pictures. The matrix computes:

$$R–Y = MR1*Cb + MR2*Cr$$
$$G–Y = MG1*Cb + MG2*Cr$$
$$B–Y = MB1*Cb + MB2*Cr$$

The initialization values for the matrix are computed from the standard ITUR (CCIR) matrix:

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} 1 & 0 & 1.402 \\ 1 & -0.345 & -0.713 \\ 1 & 1.773 & 0 \end{pmatrix} \begin{pmatrix} Y \\ Cb \\ Cr \end{pmatrix}$$

For a contrast setting of CTM = 32, the matrix values are scaled by a factor of 64, see also table 3–1.

2.1.11. RGB Processing

After adding the post-processed luma, the digital RGB signals are limited to 10 bits. Three multipliers are used to digitally adjust the white drive. Using the same multipliers an average beam current limiter is implemented. See also section 2.2.1. 'CRT Measurement and Control'.

2.1.12. OSD Color Lookup Table

The DDP 3300 A has five input lines for an OSD signal. This signal forms a 5-bit address for a color look-up table (CLUT). The CLUT is a memory with 32 words where each word holds a RGB value.

Bits 0 to 3 (bit 4 = 0) form the addresses for the ROM part of the OSD, which generates full RGB signals (bit 0 to 2) and half-contrast RGB signals (bit 3).

Bit 4 addresses the RAM part of the OSD with 16 freely programmable colors, addressable with bit 0 to 3. The programming is done via the I^2C-bus.

The amplitude of the CLUT output signals can be adjusted separately for R, G and B via the I^2C-bus. The switchover between video RGB and OSD RGB is done via the Priority bus.

2.1.13. Picture Frame Generator

When the picture does not fill the total screen (height or width too small) it is surrounded with black areas. These areas (and more) can be colored with the picture frame generator. This is done by switching over the RGB signal from the matrix to the signal from the OSD color look-up table.

The width of each area (left, right, upper, lower) can be adjusted separately. The generator starts on the right, respectively lower side of the screen and stops on the left, respectively upper side of the screen. This means, it runs during horizontal, respectively vertical flyback. The color of the complete border can be stored in the programmable OSD color look-up table in a separate address. The format is 3×4 bit RGB. The contrast can be adjusted separately.

The picture frame generator includes a priority master circuit. Its priority is programmable and the border is generated only if the priority is higher than the priority at the PRIO bus. Therefore the border can be underlay or overlay depending on the picture source.

2.1.14. Priority Codec

The priority decoder has three input lines for up to eight priorities. The highest priority is all three lines at low level. A 5-bit information is attached to each priority (see table 3–1 'Priority Bus'). These bits are programmable via the I^2C-bus and have the following meanings:

– one of two contrast, brightness and matrix values for main and side picture

– RGB from video signal or color look-up table

– disable/enable black level expander

– disable/enable peaking transient suppression when signal is switched

– disable/enable analog fast blank

2.1.15. Scan Velocity Modulation

The RGB input signal of the SVM is converted to Y in a simple matrix. Then the Y signal is differentiated by a filter of the transfer function $1–Z^{–N}$, where N is programmable from 1 to 6. With a coring, some noise can be suppressed. This is followed by a gain adjustment and an adjustable limiter. The analog output signal is generated by an 8-bit D/A converter.

The signal delay can be adjusted by $\pm$ 3.5 clocks in half-clock steps. For the gain and filter adjustment there are two parameter sets. The switching between these two sets is done with the same RGB switch signal that is used for switching between video–RGB and OSD–RGB for the RGB outputs. (See Fig. 2–8).

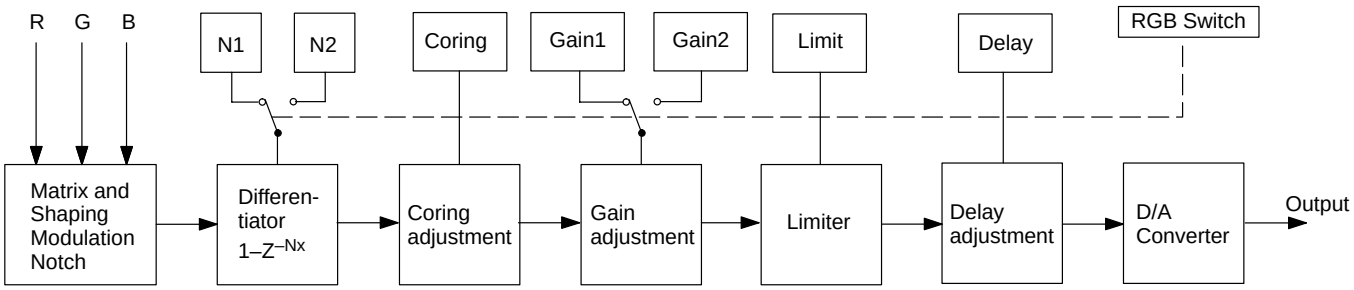


Fig. 2–8: SVM Block diagram

2.1.16. Display Phase Shifter

A phase shifter is used to partially compensate the phase differences between the video source and the flyback signal. By using the described clock system, this phase shifter works with an accuracy of approximately 1 ns. It has a range of 1 clock period which is equivalent to $\pm$ 24.7 ns at 20.25 MHz. The large amount of phase shift (full clock periods) is realized in the front-end circuit.

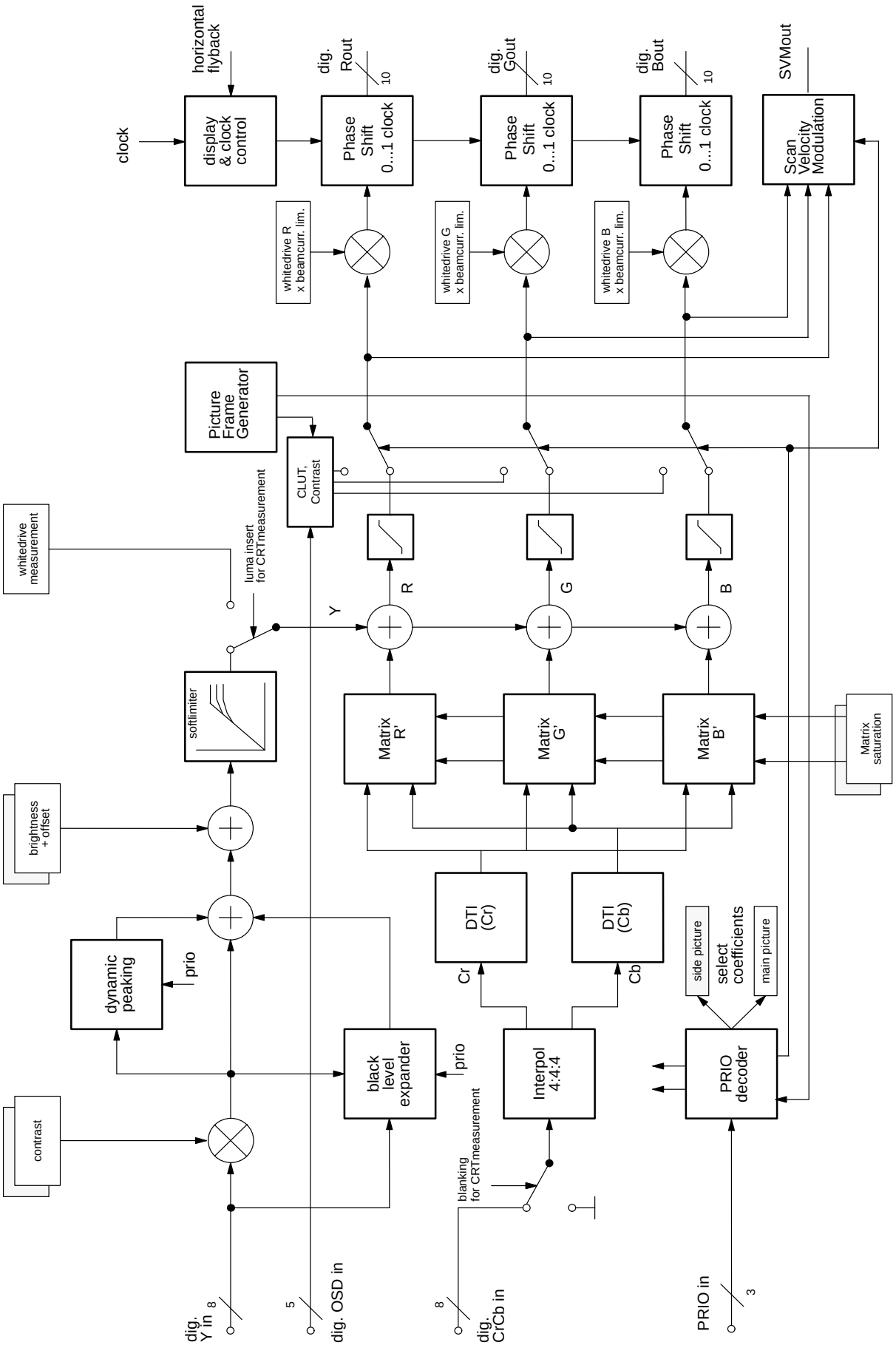


Fig. 2–9: Display part

2.2. Analog Back End

The digital RGB signals are converted to analog RGBs using three video digital to analog converters (DAC) with 10-bit resolution. An analog brightness value is provided by three additional DACs. The adjustment range is 40% of the full RGB range.

The back-end allows insertion of an external analog RGB signal. The RGB signal is key-clamped and inserted into the main RGB by the fast blank switch. The external RGB signals are virtually handled as priority bus signals. Thus, they can be overlaid or underlaid to the digital picture. The external RGB signals can be adjusted independently as regards DC-level (brightness) and magnitude (contrast).

Controlling the whitedrive/analog brightness and also the external contrast and brightness adjustments is done via the Fast Processor, located in the VPC 3200 A (ref 2.3.5.). Control of the cutoff DACs is via I^2C-bus registers.

Finally cutoff and blanking values are added to the RGB signals. Cutoff (dark current) is provided by three 9-bit DACs. The adjustment range is 60% of full scale RGB range.

The analog RGB-outputs are current outputs with current-sink characteristics. The maximum current drawn by the output stage is obtained with peak white RGB.

2.2.1. CRT Measurement and Control

The display processor is equipped with an 8-bit PDM-ADC for all measuring purposes. The ADC is connected to the sense input pin, the input range is 0 to 1.5V. The bandwidth of the PDM filter can be selected; it is 40/80 kHz for small/large bandwidth setting. The input impedance is more than 1 MΩ.

Cutoff and white drive current measurement are carried out during the vertical blanking interval. They always use the small bandwidth setting. The current range for the cutoff measurement is set by connecting a sense resistor to the MADC input. For the whitedrive measurement, the range is set by using another sense resistor and the range select switch 2 output pin (RSW2). During the active picture, the minimum and maximum beam current is measured. The measurement range can be set by using the range select switch 1 pin (RSW1) as shown in Fig. 2–10 and Fig. 2–11. The timing window of this measurement is programmable. The intention is to automatically detect letterbox transmission or to measure the actual beam current. All control loops are closed via the external control microprocessor.

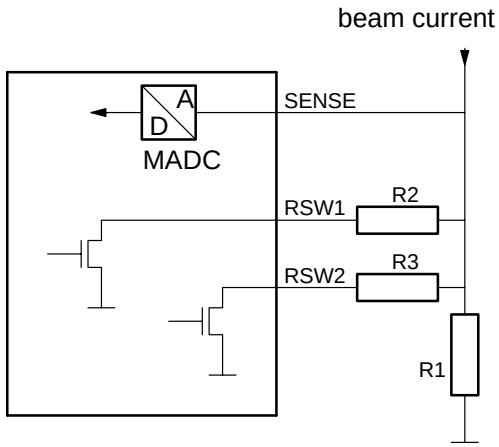


Fig. 2–10: MADC Range Switches

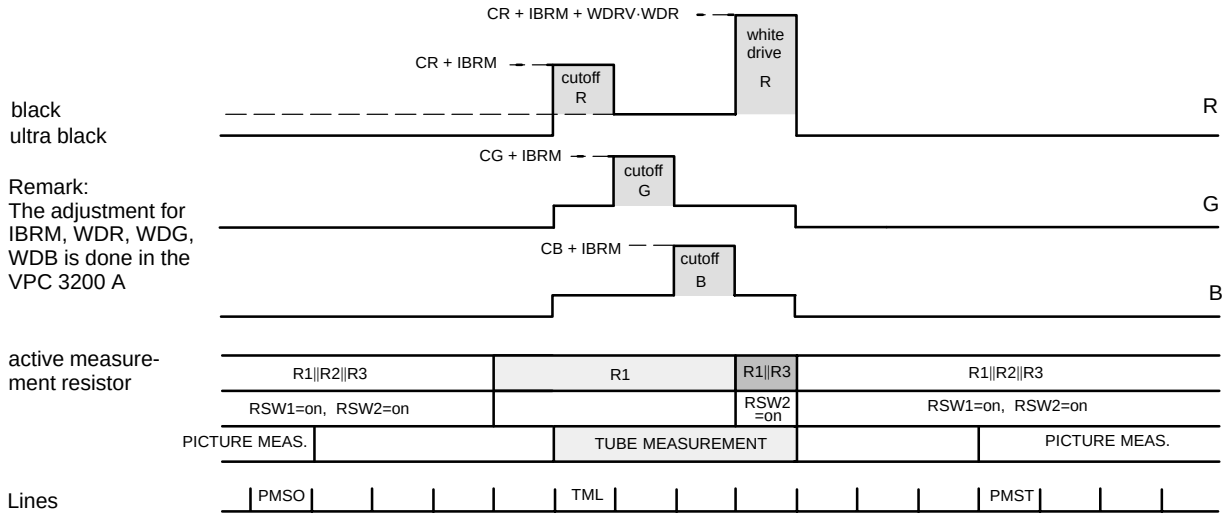


Fig. 2–11: MADC Measurement Timing

In each field two sets of measurements can be taken:

a) The picture tube measurement returns results for

– cutoff R

– cutoff G

– cutoff B

– white drive R or G or B (sequentially)

b) The picture measurement returns data on

– active picture maximum current

– active picture minimum current

The tube measurement is automatically started when the cutoff blue result register is read. Cutoff control for RGB requires one field only while a complete white-drive control requires three fields. If the measurement mode is set to 'offset check', a measurement cycle is run with the cutoff/whitedrive signals set to zero. This allows to compensate the MADC offset as well as input the leakage currents. During cutoff and whitedrive measurements, the average beam current limiter function (ref. 2.2.3.) is switched off and a programmable value is used for the brightness setting. The start line of the tube measurement can be programmed via I^2C-bus, the first line used for the measurement, i.e. measurement of cutoff red, is 2 lines after the programmed start line.

The picture measurement must be enabled by the control microprocessor after reading the min./max. result registers. If a '1' is written into bit 2 in subaddress 25, the measurement runs for one field. For the next measurement a '1' has to be written again. The measurement is always started at the beginning of active video.

The vertical timing for the picture measurement is programmable, and may even be a single line. Also the signal bandwidth is switchable for the picture measurement.

Two horizontal windows are available for the picture measurement. The large window is active for the entire active line. Tube measurement is always carried out with the small window. Measurement windows for picture and tube measurement are shown in Figure 2–12.

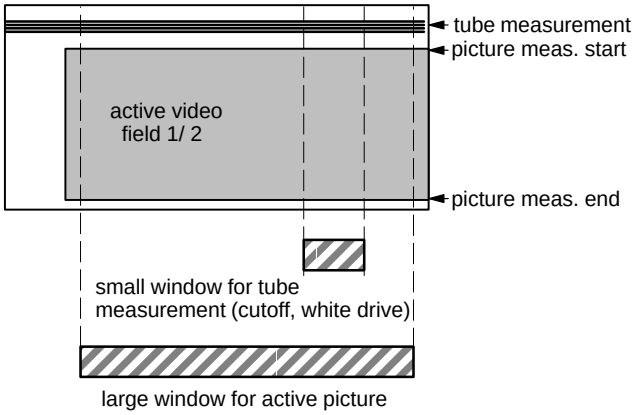


Fig. 2–12: Windows for tube and picture measurements

2.2.2. SCART Output Signal

The RGB output of the DDP 3300 A can also be used to drive a SCART output. In the case of the SCART signal, the parameter CLMPR (clamping reference) has to be set to 1. Then, during blanking, the RGB outputs are automatically set to 50% of the maximum brightness. The DC offset values can be adjusted with the cutoff parameters CR, CG, and CB. The amplitudes can be adjusted with the drive parameters WDR, WDG, and WDB (located in the VPC 3200 A).

2.2.3. Average Beam Current Limiter

The average beam current limiter (BCL) uses the sense input for the beam current measurement. The BCL uses a different filter to average the beam current during the active picture. The filter bandwidth is approx. 2 kHz. The beam current limiter has an automatic offset adjustment that is active two lines before the first cutoff measurement line.

The beam current limiter function is located in the VPC 32XX A. The data exchange between the VPC and the DDP is done via a single-wire serial interface (ref. section 2.3.5.).

The beam current limiter allows the setting of a threshold current. If the beam current is above the threshold, the excess current is low-pass filtered and used to attenuate the RGB outputs by adjusting the white-drive multipliers for the internal (digital) RGB signals, and the analog contrast multipliers for the analog RGB inputs, respectively.

The lower limit of the attenuator is programmable, thus a minimum contrast can always be set. During the tube measurement, the ABL attenuation is switched off. After the white drive measurement line it takes 3 lines to switch back to BCL limited drives and brightness.

Typical characteristics of the ABL for different loop gains are shown in Fig. 2–13; for this example the tube has been assumed to have square law characteristics.

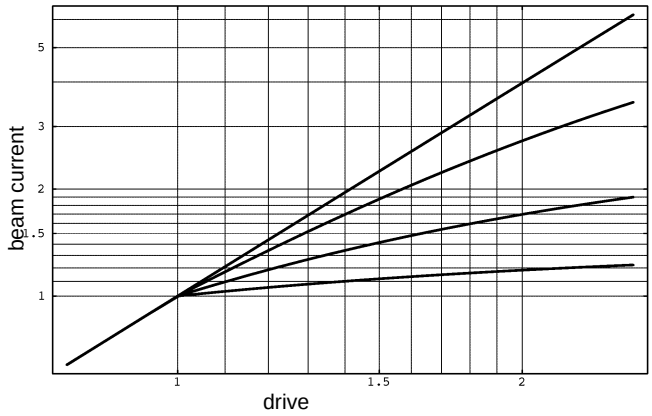


Fig. 2–13: Beam current limiter characteristics:
beam current output vs. drive
BCL threshold: 1

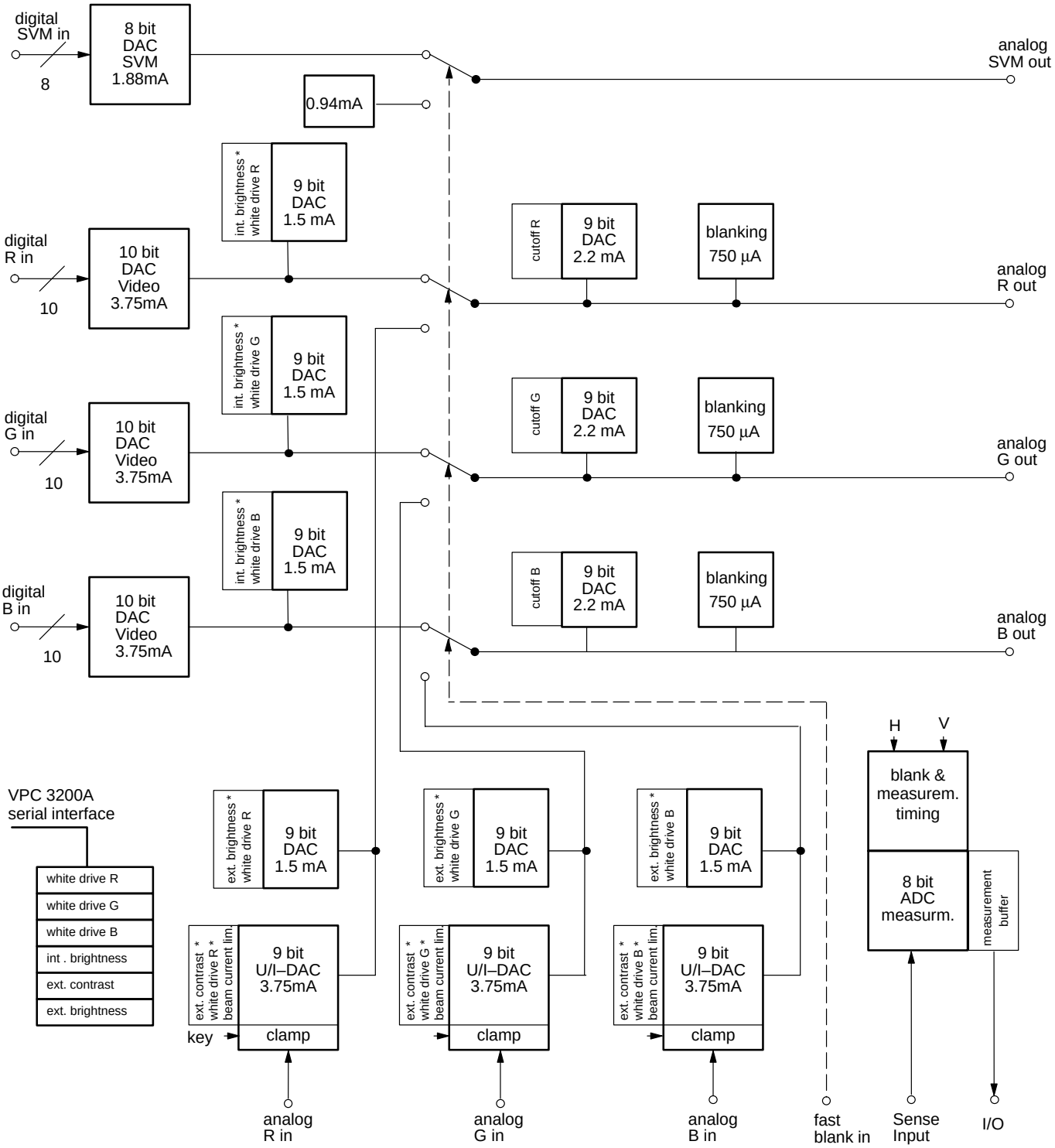


Fig. 2–14: Analog back-end

2.3. Synchronization and Deflection

The synchronization and deflection processing is distributed over front-end, e.g., the VPC 320X and the DDP 3300 A back end. The video clamping, horizontal and vertical sync separation and all video related timing information are processed in the front end. Most of the processing that runs at the horizontal frequency is programmed on the internal Fast Processor (FP). Also the values for vertical & East/West deflection are calculated by the FP software.

The information extracted by the video sync processing is multiplexed onto the hardware front sync signal (FSY) and distributed to the rest of the video processing system. The format of the front sync signal is given in Fig. 2–15.

The data for the vertical deflection, the sawtooth and the East/West correction signal is calculated in the VPC 320X. The data is transferred to the back-end by a single wire interface.

The display related synchronization, i.e. generation of horizontal and vertical drive and synchronization of horizontal and vertical drive to the video timing extracted in the front-end, are implemented in hardware in the back-end.

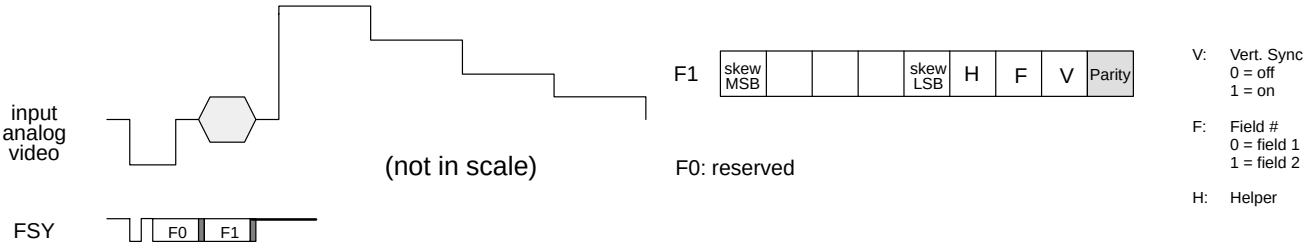


Fig. 2–15: Front sync format

2.3.1. Deflection Processing

The deflection processing generates the signals for the horizontal and vertical drive (see Fig. 2–16). This block contains two phase-locked loops:

– PLL2 generates the horizontal and vertical timing, e.g. blanking, clamping and composite sync. Phase and frequency are synchronized by the front sync signal.

– PLL3 adjusts the phase of the horizontal drive pulse and compensates for the delay of the horizontal output stage. Phase and frequency are synchronized by the oscillator signal of PLL2.

The horizontal drive circuitry uses a digital sine wave generator to produce the exact (subclock) timing for the drive pulse. The generator runs at 1 MHz; in the output stage the frequency is divided down to give drive-pulse period and width. In standby mode, the output stage is driven from an internal 1 MHz clock that is derived from the 5 MHz clock input signal and a fixed drive pulse width is used. When the circuit is switched out of standby operation the drive pulse width is programmable. The horizontal drive uses a high voltage (8V) open drain output transistor.

The Main Sync (MSY) signal that is generated from PLL3 is a multiplex of all display-related data (Fig. 2–17). This signal is intended for use by other processors, e.g. a PIP processor can use this signal to adjust to a certain display position.

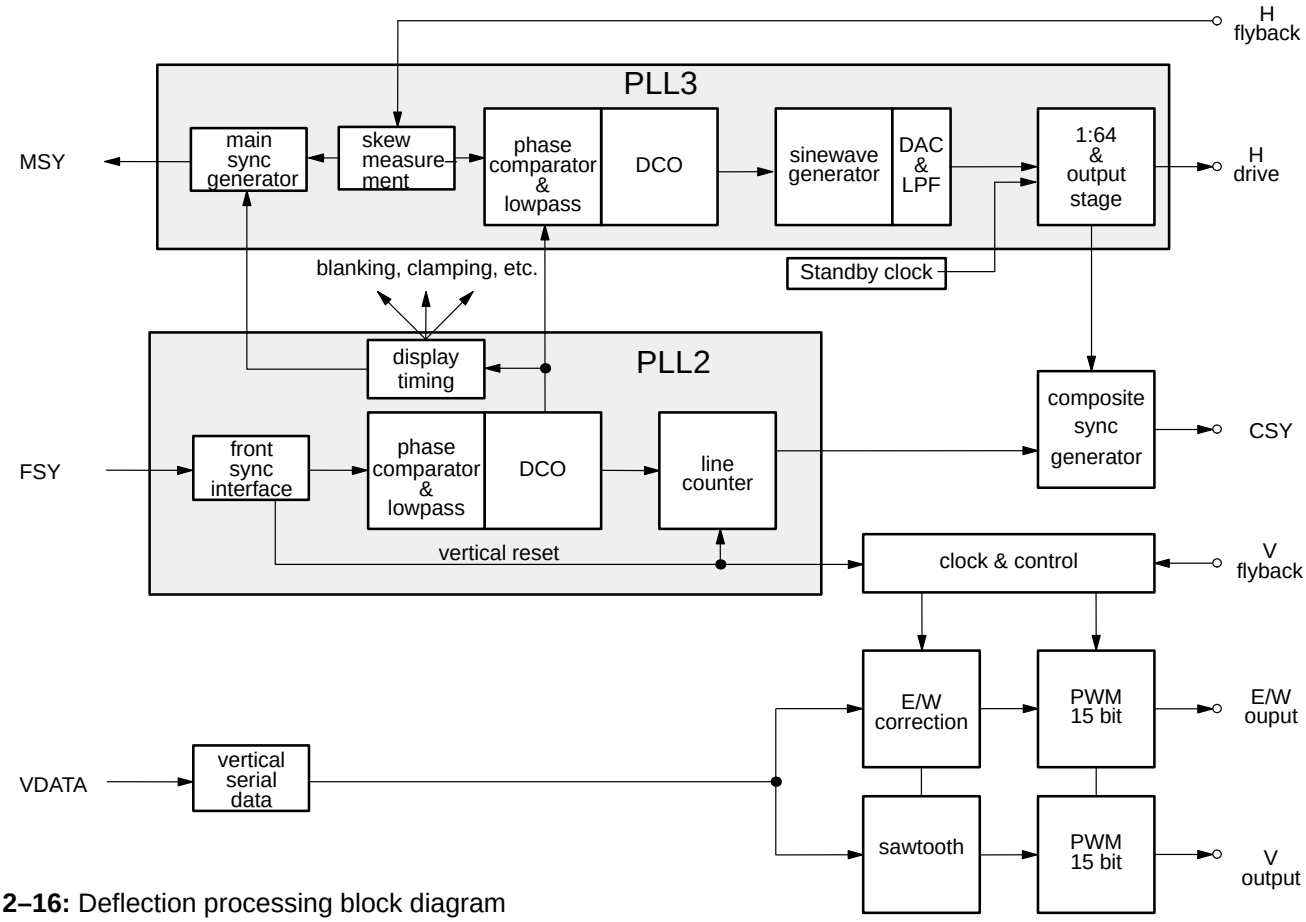


Fig. 2–16: Deflection processing block diagram

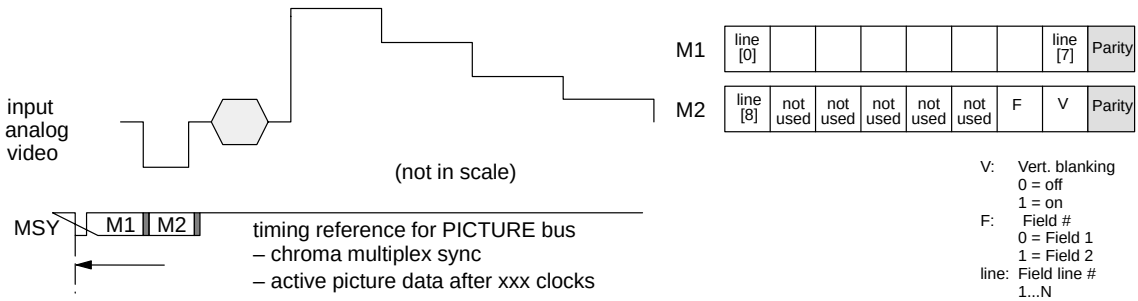


Fig. 2–17: Main sync format

2.3.2. Horizontal Phase Adjustment

This section describes a simple way to align PLL phases and the horizontal frame position.

1. The parameter NEWLIN in the VPC 320X has to be adjusted. The minimum possible value is 34 (recommended for a standard 4:3 signal).
2. With HDRV, the duration of the horizontal drive pulse has to be adjusted.
3. With POFS2, the clamping pulse for the analog RGB input has to be adjusted to the correct position, e.g. the pedestal of the generator signal.
4. With POFS3, the horizontal position of the analog RGB signal (from SCART) has to be adjusted.
5. With HPOS, the digital RGB output signal (from VPC) has to be adjusted to the correct horizontal position.
6. With HBST and HBSO, the start and stop values for the horizontal blanking have to be adjusted.

2.3.3. Vertical and East/West Deflection

The calculations of the vertical and East/West deflection waveforms are done in the video front-end, i.e., the VPC 320X. The algorithm uses a chain of accumulators to generate the required polynomial waveforms. To produce the deflection waveforms, the accumulators are initialized at the beginning of each field. The initialization values must be computed by the TV control processor and are written to the VPC 320X once. The waveforms are described as polynomials in x, where x varies from 0 to 1 for one field.

$P: a + b(x–0.5) + c(x–0.5)^2 + d(x–0.5)^3 + e(x–0.5)^4$

The initialization values for the accumulators a0..a3 for vertical deflection and a0..a4 for East/West deflection are 12-bit values.

The vertical waveform can be scaled according the average beam current. This is used to compensate the effects of electric high tension changes due to beam current variations. In order to get a faster vertical retrace timing, the output impedance of the vertical D/A-converter can be reduced by 50% during the retrace.

Fig. 2–18 shows some vertical and East/West deflection waveforms. The polynomial coefficients are also stated.

Detailed information on the programming of the vertical and East/West deflection parameters is given in the VPC 320X datasheet.

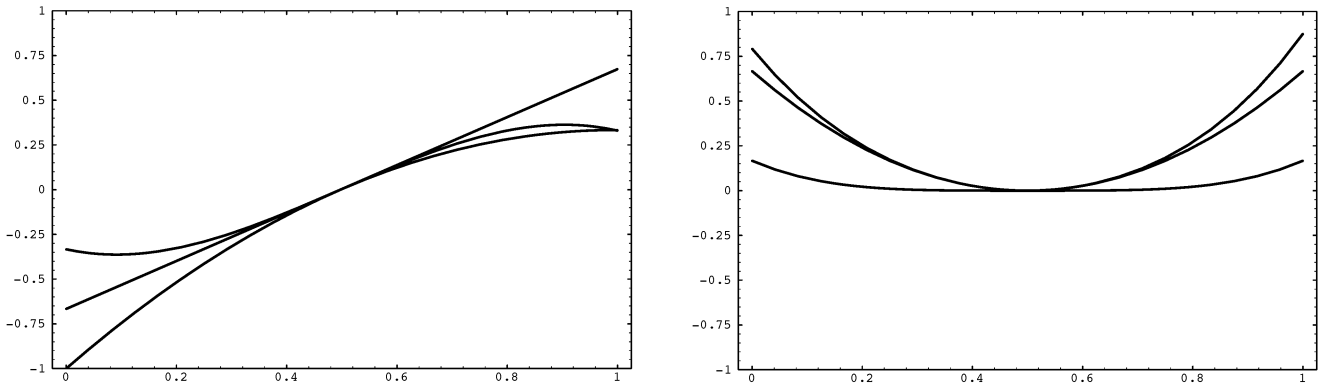


Fig. 2–18: Vertical and East/West Deflection Waveforms

Vertical: a,b,c,d 0,1,0,0
0,1,1,0
0,1,0,1

East/West: a,b,c,d,e 0,0,1,0,0
0,0,0,0,1
0,0,1,1,1

2.3.4. Protection Circuitry

– Picture tube and drive stage protection is provided through the following measures:

– Vertical flyback protection input: this pin searches for a negative edge in every field, otherwise the RGB drive signals are blanked.

– Drive shutoff during flyback: this feature can be selected by software.

– Safety input pin: this input has two thresholds. Between zero and the lower threshold, normal functioning takes place. Between the lower and the higher threshold, the RGB signals are blanked. Above the higher threshold, the RGB signals are blanked and the horizontal drive is shut off. Both thresholds have a small hysteresis.

– The main oscillator (not included in the DDP) and the horizontal drive circuitry are run from a separate (standby) power supply and are already active while the TV set is powering up.

2.3.5. Deflection Bus

The deflection bus is a serial, bidirectional interface between the DDP and the Fast Processor in the VPC chip, so the calculation of the vertical and the East/West signals is performed by the FP in the VPC. The FP in the VPC also does the beam current limitation. The following data is transferred via the deflection bus:

– vertical and East/West drive values for the VERT and EW DAC from VPC to DDP

– values for R/G/B DACs for ext. brightness, internal brightness, external contrast, white drive from VPC to DDP

– tube current measurement from DDP to VPC

– status bits from DDP to VPC

– vertical reset of deflection back-end (from VPC to DDP).

2.4. Reset and Standby Functions

Reset of most functions (exceptions see below) is performed by a reset pin. When this pin becomes active, all the internal registers and counters are set to zero. When this pin is released, the internal reset is still active for approximately 4 µs. After that time all the internal registers are loaded with the values defined in the defaults ROM. All the registers which are updated with the vertical sync get these values with the next vertical sync. During this initialization procedure (approx. 60 µs) it is not possible to access the DDP via the serial interface (I^2C). Access to other ICs via the serial bus is possible during that time. The same initialization procedure is started when the internal clock supervision detects that there is no clock (in the video processing part).

Exceptions for initialization :

– CCU clock divider (5MHz), not initialized by reset

– standby clock divider (1MHz), not initialized by reset, but clock selector switched to standby clock

During standby, only the horizontal drive pulse and the 5 MHz clock output for the control microprocessor are active. The standby circuitry is reset when the standby supply voltage is applied.

2.4.1. Standby Mode for VPC and DDP

In a system with the video processor VPC and the display processor DDP it is possible to realize a standby mode where the whole signal processing is disabled and only some basic functions are working. This is possible because different supply pins for normal operation and standby operation are available. The standby mode is realized by switching off the supplies for analog frontend (VSUPF), analog backend (VSUPO) and the normal digital supply (VSUPD). The standby supply (VSTDBY) still has its nominal voltage. In the standby mode, all registers and counter values in the VPC and DDP are lost, they have to be re-initialized after analog and digital supplies are switched on again. The VPC still generates the 5 MHz clock which is used in the DDP as timing reference during standby.

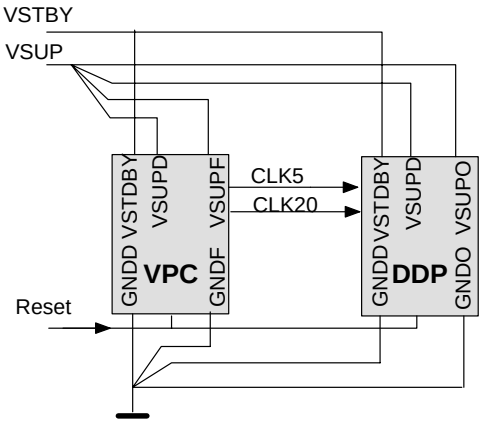


Fig. 2–19: VPC & DDP Supply and Clock

To disable all the analog and digital functions, it is necessary to bring the analog and digital supplies below 0.5 V. Only this guarantees that all the normal functions are disabled and the standby current for analog and digital supply is at its minimum.

In the standby mode the following functions are still available :

– crystal oscillator of VPC

– 5 MHz clock output of VPC, standby clock for DDP, can also be used as CCU clock

– horizontal output of DDP, duty cycle set to 50 %, the 5 MHz clock is used as timing reference in standby mode (standby clock); protection modes with safety and horizontal flyback pins (in VPC) are not available

When the main power goes down, DDP and VPC react in different ways. An internal power supervision, in both VPC and DDP, generates the required power down signals.

2.4.2. DDP Power on

The DDP has its own clock and voltage supervision circuit to generate a reset signal during power on. The initialization of registers is described in section 2.4.3. ‘DDP Standby On/Off’. The HOUT signal is disabled until a proper CLK5 signal (5 MHz clock) has been detected. Therefore at least one positive and negative edge with the correct distance (two 20 MHz clocks) has to be received. After this Clock Release signal, the HOUT generator runs with the standby clock, which is derived from the 5 MHz clock (divide by 5). Switching to the line

locked clock from the horizontal PLL is performed by the CCU.

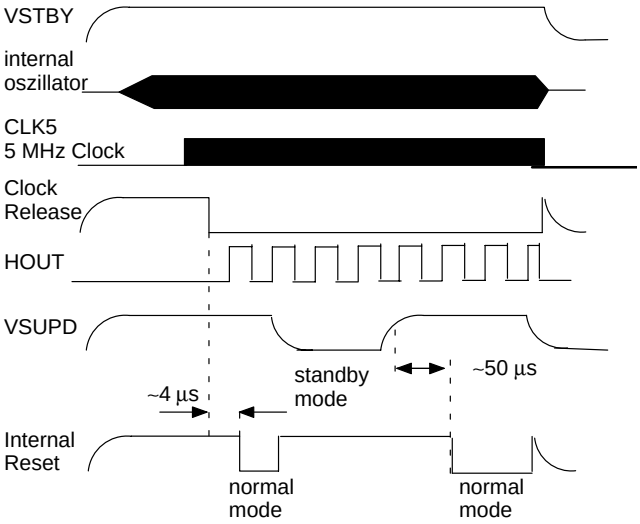


Fig. 2–20: DDP power on, standby on/off

2.4.3. DDP Standby On/Off

Switching the DDP to Standby Mode is more critical because of the HOUT output signal. Before the standby mode is entered, the clock source for the horizontal output generator has to be switched to the standby clock.

Switching to Standby Mode can be done by the CCU as a reaction to a remote control command (see register 53, EHPLL = disable) or by the internal voltage supervision of the DDP. This voltage supervision activates the Power Down signal when the supply for the digital circuits (VSUPD) goes below $V_{SUPD–pd}$ (~4.5 V). The Power Down signal switches the clock source for the HOUT generation to the standby clock and sets the duty factor to 50%. This is exactly what the EHPLL bit does.

Because the clocks from the DDP–pll and the standby clock are not in phase, the actual phase (High/Low) of the HOUT signal may be up to one pll or standby clock (~1 µs) longer than a regular one when the clock source is changed.

The voltage supervising reacts if VSUPD goes below $V_{SUPD–pd}$ for more than 50 ns. This Power Down signal is extended by 50 µs after VSUPD is back again.

When switched off, the negative slope of the supply voltage VSUPD should not be larger than approximately 0.2 V/µs (see Recommended Operating Conditions).

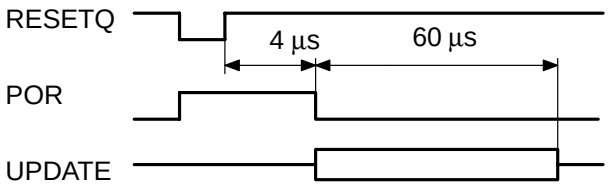


Fig. 2–21: External RESET

2.4.4. Reset DDP

Reset of most functions (exception see below) is performed by different sources:

– power on circuit (VSTBY, VSUPD)

– reset pin (DDP)

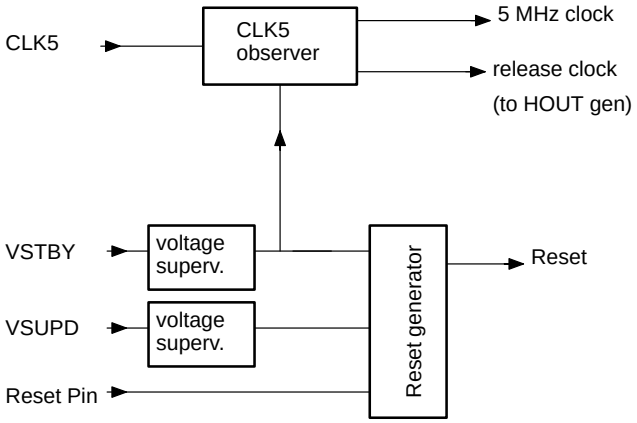


Fig. 2–22: DDP reset generation

If one of these sources creates a reset, all the internal registers and counters are set to zero. When this reset source becomes inactive, the internal reset is still active for 4 µs. After that time all the internal registers are loaded with the values defined in the defaults ROM. All the registers which are updated with the vertical sync (chain registers) get these values with the next vertical sync. During this initialization procedure (approx. 60 µs) it is not possible to access the DDP via the I^2C-bus.

3. Serial Interface

3.1. I²C-bus Interface

Communication between the DDP 3300 A and the external controller is done via I²C-bus. The DDP 3300 A has an I²C-bus slave interface and uses I²C clock synchronization to slow down the interface if required. The I²C-bus interface uses one level of subaddress: one I²C-bus address is used to address the IC and a subaddress selects one of the internal registers. The I²C-bus chip address is given below:
Note: The I²C address is subject to change!

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	0	1	0/1

The registers of the DDP 3300 A have 8 or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data words.

Functions implemented by firmware in the on-chip control microprocessor (FP) located in the VPC are explained in the VPC datasheet.

Figure 3–1 shows I²C-bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with read command set.

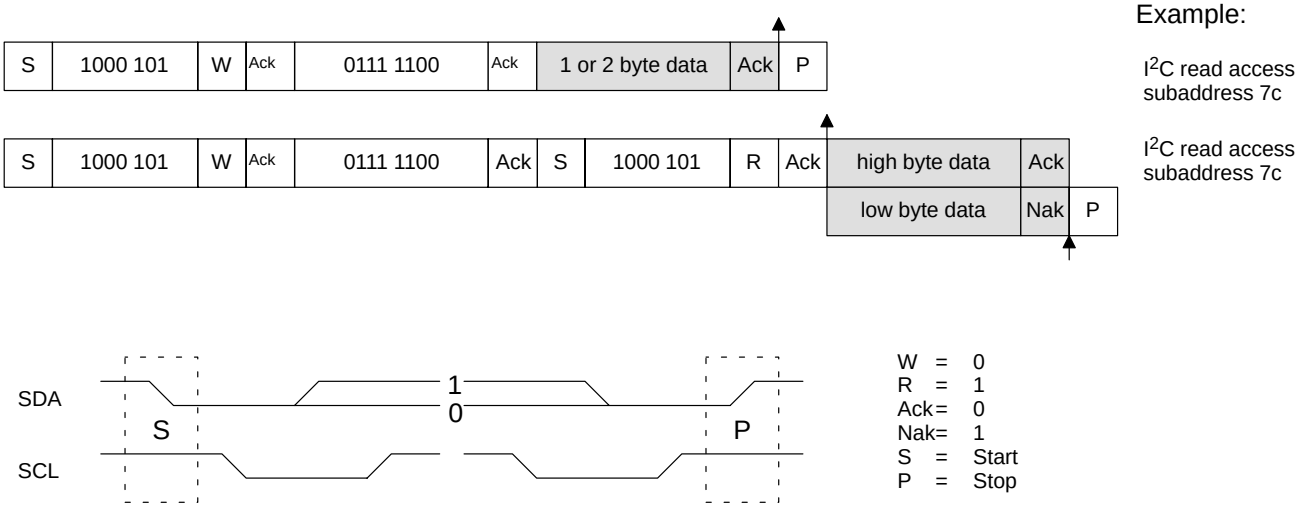


Fig. 3–1: I²C-bus protocols

3.2. Control and Status Registers

Table 3–1 gives definitions of the DDP 3300 A control and status registers. The number of bits indicated for each register in the table is the number of bits implemented in hardware, i.e., a 9-bit register must always be accessed using two data bytes, but the 7 MSB will be don't care on write operations and 0 on read operations. Write registers that can be read back are indicated in the following table.

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in Table 3–1.

The register modes given in Table 3–1 are:

w	write only register
w/r	write/read data register
r	read data from DDP 3300 A
h	register is latched with horizontal pulse
v	register is latched with vertical pulse

The mnemonics used in the INTERMETALL DDP 3300 A demo software are given in the last column.

Table 3–1: Control and status registers

I²C sub address	Number of bits	Mode	Function	Default	Name
	PRIORITY BUS				
			priority mask register, if bit[x] is set to 1 then the function is active for the respective signal priority		
75	9	w v	bit [7:0] bit[x] 0/1: select contrast,brightness,matrix for main / side picture	0	PBCT
71	9	w v	bit [7:0] bit[x] 0/1: select main(video)/external (via CLUT) RGB	0	PBERGB
7d	9	w v	bit [7:0] bit[x] 0/1: disable/enable black level expander	0	PBBLE
79	9	w v	bit [7:0] bit[x] 0/1: disable/enable peaking transient suppression when signal is switched	0	PBPK
4b	9	w v	bit [7:0] bit[x] 0/1: disable/enable analog fast blank input	0	PBFB
47	9	w v	bit [2:0] picture frame generator priority id bit [8] enable prio id for picture frame generator	0	PFGID PFGEN
	LUMA CHANNEL				
61	9	w v	bit [5:0] 0..63/32 main picture contrast	32	CTM
65	9	w v	bit [5:0] 0..63/32 side picture contrast	32	CTS
51	9	w v	bit [8:0] –256..255 main picture brightness	0	BRM
55	9	w v	bit [8:0] –256..255 side picture brightness	0	BRS
59	9	w v	black level expander: bit [3:0] 0..15 tilt coefficient bit [8:4] 0...31 amount	 8 12	 BTLT BAM
5d	9	w v	black level expander: bit [8:0] 0..511 disable expansion, threshold value	 200	 BTHR
69	9	w v	luma peaking filter, the gain at high frequencies and small signal amplitudes is: 1 + (k1+k2)/8 bit [3:0] 0..15 k1: peaking level undershoot bit [7:4] 0..15 k2: peaking level overshoot bit [8] 0/1 peaking value normal/inverted (peaking/softening)	 4 4 0	 PKUN PKOV PKINV
6d	9	w v	luma peaking filter, coring bit [4:0] 0..31 coring level bit [7:5] reserved bit [8] 0/1 peaking filter center frequency high/low	 3 0	 COR PFS
41	9	w v	luma soft limiter, slope A and B bit [3:0] slope segment A bit [7:4] slope segment B	 0 0	 LSLSA LSLSB
45	9	w v	bit [7:0] luma soft limiter absolute limit (unsigned) bit [8] 0/1 modulation off/on	255 1	LSLAL LSLM
49	9	w v	bit [8:0] luma soft limiter segment B tilt point (unsigned)	300	LSLTB
4d	9	w v	bit [8:0] luma soft limiter segment A tilt point (unsigned)	250	LSLTA

I²C sub address	Number of bits	Mode	Function	Default	Name
	CHROMA CHANNEL				
14	8	w/r	luma/chroma matching delay bit [2:0] –3...3 variable chroma delay bit [3] 0/1 chroma polarity signed / offset binary bit [4] 0/1 C_B (U) sample first / C_R (V) sample first bit [5] test bit, set to 0	 0 1 0 0	 LDB COB ENVU
66	9	w v	digital transient improvement bit [3:0] 0..15 coring value bit [7:4] 0..15 DTI gain bit [8] 0/1 narrow/wide bandwidth mode	 1 5 1	 DTICO DTIGA DTIMO
	INVERSE MATRIX				
7c 74	9 9	w v w v	main picture matrix coefficient R–Y = MR1M*C_B + MR2M*C_R bit [9:0] –256/128 ... 255/128 bit [9:0] –256/128 ... 255/128	0 86	MR1M, MR2M
6c 64	9 9	w v w v	main picture matrix coefficient G–Y = MG1M*C_B + MG2M*C_R bit [9:0] –256/128 ... 255/128 bit [9:0] –256/128 ... 255/128	–22 –44	MG1M, MG2M
5c 54	9 9	w v w v	main picture matrix coefficient B–Y = MB1M*C_B + MB2M*C_R bit [9:0] –256/128 ... 255/128 bit [9:0] –256/128 ... 255/128	113 0	MB1M, MB2M
78 70	9 9	w v w v	side picture matrix coefficient R–Y = MR1S*C_B + MR2S*C_R bit [9:0] –256/128 ... 255/128 bit [9:0] –256/128 ... 255/128	0 73	MR1S, MR2S
68 60	9 9	w v w v	side picture matrix coefficient G–Y = MG1S*C_B + MG2S*C_R bit [9:0] –256/128 ... 255/128 bit [9:0] –256/128 ... 255/128	–19 –37	MG1S, MG2S
58 50	9 9	w v w v	side picture matrix coefficient B–Y = MB1S*C_B + MB2S*C_R bit [9:0] –256/128 ... 255/128 bit [9:0] –256/128 ... 255/128	97 0	MB1S, MB2S
	COLOR LOOK-UP TABLE				
00–0f	16	w h	color look-up table : 16 entries, 12 bit wide, The CLUT registers are initialized at power-up bit [3:0] 0..15 blue amplitude bit [7:4] 0..15 green amplitude bit [11:8] 0..15 red amplitude	000H F00H 0F0H FF0H 00FH F0FH 0FFH FFFH 7FFH 700H 070H 770H 007H 707H 077H 777H	CLUT0 CLUT15
11	16	w h	picture frame color 12 bit wide, bit [3:0] 0..15 blue amplitude bit [7:4] 0..15 green amplitude bit [11:8] 0..15 red amplitude	 0 0 0	 PFCB PFCG PFCR

I²C sub address	Number of bits	Mode	Function	Default	Name
4c	9	w v	digital OSD insertion contrast for R (amplitude range: 0 to 255) bit [3:0] 0..13 R amplitude = CLUTn · (DRCT + 4) 14,15 invalid picture frame insertion contrast for R (ampl. range: 0 to 255) bit [7:4] 0..13 R amplitude = PFCR · (PFRCT + 4) 14,15 invalid	8 8	DRCT PFRCT
48	9	w v	digital OSD insertion contrast for G (amplitude range: 0 to 255) bit [3:0] 0..13 G amplitude = CLUTn · (DGCT + 4) 14,15 invalid picture frame insertion contrast for G (ampl. range: 0 to 255) bit [7:4] 0..13 G amplitude = PFCG · (PFGCT + 4) 14,15 invalid	8 8	DGCT PFGCT
44	9	w v	digital OSD insertion contrast for B (amplitude range: 0 to 255) bit [3:0] 0..13 B amplitude = CLUTn · (DBCT + 4) 14,15 invalid picture frame insertion contrast for B (ampl. range: 0 to 255) bit [7:4] 0..13 B amplitude = PFCB · (PFBCT + 4) 14,15 invalid	8 8	DBCT PFBCT
	PICTURE FRAME GENERATOR				
4F	9	w v	bit [8:0] horizontal picture frame begin code 0 = picture frame generator horizontally disabled code 1FF = full frame	0	PFGHB
53	9	w v	bit [8:0] horizontal picture frame end	0	PFGHE
63	9	w v	bit [8:0] vertical picture frame begin code 0 = picture frame generator vertically disabled	270	PFGVB
6f	9	w v	bit [8:0] vertical picture frame end	56	PFGVE
			enable and priority – see under ‘PRIORITY BUS’ picture frame color – see under ‘COLOR LOOK-UP TABLE’		
	SCAN VELOCITY MODULATION				
62	9	w v	video mode coefficients bit [5:0] gain1 bit [8:6] differentiator delay 1 (0= filter off, 1...6= delay)	 60 4	 SVG1 SVD1
5e	9	w v	text mode coefficients bit [5:0] gain 2 bit [8:6] differentiator delay 2 (0= filter off, 1...6= delay)	 60 4	 SVG2 SVD2
5a	9	w v	limiter bit [6:0] limit value bit [8:5] not used, set to ”0”	 100 0	 SVLIM
56	9	w v	delay and coring bit [3:0] adjustable delay, in 1/2 display clock steps, (value 5 : delay of SVMOUT is the same as for RGBOUT bit [7:4] coring value bit [8] not used, set to ”0”	 7 0	 SVDEL SVCOR

I²C sub address	Number of bits	Mode	Function	Default	Name
	DISPLAY CONTROLS				
52 4e 4a	9 9 9	w v w v w v	cutoff Red cutoff Green cutoff Blue	0 0 0	CR CG CB
	TUBE AND PICTURE MEASUREMENT				
7b	9	w v	picture measurement start line bit [8:0] (TML+9)..511 first line of picture measurement	23	PMST
6b	9	w v	picture measurement stop line bit [8:0] (PMST+1)..511 last line of picture measurement	308	PMSO
7f	9	w v	tube measurement line bit [8:0] 0..511 start line for tube measurement	15	TML
25	8	w/r	tube and picture measurement control bit [0] 0/1 disable/enable tube measurement bit [1] 0/1 80/40 kHz bandwidth for picture measurement bit [2] 0/1 disable/enable picture measurement (writing a '1' starts one measurement cycle) bit [3] 0/1 large/small picture measurement window, will be disabled from bit[3] in address 32 bit [4] 0/1 measure / offset check for adc bit [7:5] reserved	0	PMC TMEN PMBW PMEN PMWIN OFSEN
13	16	w/r	white drive measurement control bit [9:0] 0..1023 RGB values for white drive beam current measurement bit [10] reserved bit [11] 0/1 RGB values for white drive beam current measurement disabled/enabled	512 0	WDRV EWDM
18–1d 18 19 1a 1d 1c 1b	8	r	measurement result registers minimum in active picture maximum in active picture white drive cutoff/leakage red cutoff/leakage green cutoff/leakage blue, read pulse starts tube measurement	– 	 MRMIN MRMAX MRWDR MRCR MRCG MRCB
1e	8	r	measurement adc status and fast blank input status measurement status register bit [0] 0/1 tube measurement active / complete bit [2:1] white drive measurement cycle 00 red 01 green 10 blue 11 reserved bit [3] 0/1 picture measurement active / complete bit [4] 0/1 fast blank input low / high (static) bit [5] 1 fast blank input negative transition since last read (bit reset at read) bit [7:6] reserved	–	PMS

I^2C sub address	Number of bits	Mode	Function	Default	Name
	TIMING				
67	9	w v	vertical blanking start bit [8:0] 0..511 first line of vertical blanking	305	VBST
77	9	w v	vertical blanking stop bit [8:0] 0..511 last line of vertical blanking	25	VBSO
73	9	w v	start of Black Level Expander measurement bit [8:0] 0..511 first line of measurement, stop with first line of vertical blanking	30	AVST
5f	9	w v	bit [8:0] free running field period = (value + 4) lines	0	STIMP
	HORIZONTAL DEFLECTION				
7a	9	w v	adjustable delay of PLL2, clamping, and blanking (relative to front sync) adjust clamping pulse for analog RGB input bit [8:0] –256..+255 ± 8 µs	–141	POFS2
76	9	w v	adjustable delay of flyback, main sync, csync and analog RGB (relative to PLL2) adjust horizontal drive or csync bit [8:0] –256..+255 ±8 µs	0	POFS3
7e	9	w v	adjustable delay of main sync (relative to flyback) adjust horizontal position for digital picture bit [8:0] 20 steps = 1 µs	120	HPOS
5b	9	w/r	start of horizontal blanking bit [8:0] 0..511	1	HBST
57	9	w/r	end of horizontal blanking bit [8:0] 0..511	48	HBSO
			PLL2/3 filter coefficients, 1 of 5 bit code (n = bit number set to 1)		
6a	9	w v	bit [5:0] proportional coefficient PLL3, 2^{-n-1}	2	PKP3
6e	9	w v	bit [5:0] proportional coefficient PLL2, 2^{-n-1}	1	PKP2
72	9	w v	bit [5:0] integral coefficient PLL2, 2^{-n-5}	2	PKI2
15	16	w/r	horizontal drive and vertical signal control register bit [5:0] 0..63 horizontal drive pulse duration in µs (internally limited to 4..61) bit [6] 0/1 disable/enable horizontal PLL2 and PLL3 bit [7] 0/1 1: disable horizontal drive pulse during flyback bit [8] 0/1 reserved, set to '0' bit [9] 0/1 enable/disable ultra black blanking bit [10] 0/1 0: all outputs blanked 1: normal mode bit [11] 0/1 enable/disable clamping for analog RGB input bit [12] 0/1 disable/enable vertical free running mode (FIELD is set to field2, no interlace) bit [13] 0/1 enable/disable vertical protection bit [14] 0/1 internal/external (under VPC control) start of vertical and E/W signal bit [15] 0/1 disable/enable phase shift of display clock	32 0 0 0 0 1 0 0 0 1	HDRV EHPLL EFLB INTRL DUBL EBL DCRGB SELFT DVPR XDEFL DISKA

I²C sub address	Number of bits	Mode	Function	Default	Name
	OUTPUT PINS				
10	8	w/r	output pin configuration bit [2:0] pin driver strength, MSY and CSY 7 = minimum strength 0 = maximum strength bit [[4:3] pin driver strength, FPDAT 3 = minimum strength 0 = maximum strength bit [5] 0/1 disable/enable internal resistor for vertical and East/West drive output bit [7:6]] function of CSY pin : 00 composite sync signal output 01 25 Hz output (field1/field2 signal) 10 no interlace (field 2), output = 0 11 1 MHz horizontal drive clock	0	PSTSY PSTPRI VEWXR CSYM
	MISCELLANEOUS				
32	8	w/r	fast blank interface mode bit [0] 0 fast blank from FBLIN pin 1 force internal fast blank signal to high bit [1] 0/1 fast blank active high/low at FBLIN pin bit [2] 0/1 disable/enable clamping reference for RGB outputs bit [3] 1 full line MADC measurement window, disables bit [3] in address 25 bit [4] 0/1 horizontal flyback pulse input active high/low bit [6:5] 0 testbits, set to ‘0’ bit [7] reserved, set to ‘0’	0	FNFOH FBPOL CLMPR FLMW FLPOL SKMOD

4. Specifications

4.1. Outline Dimensions

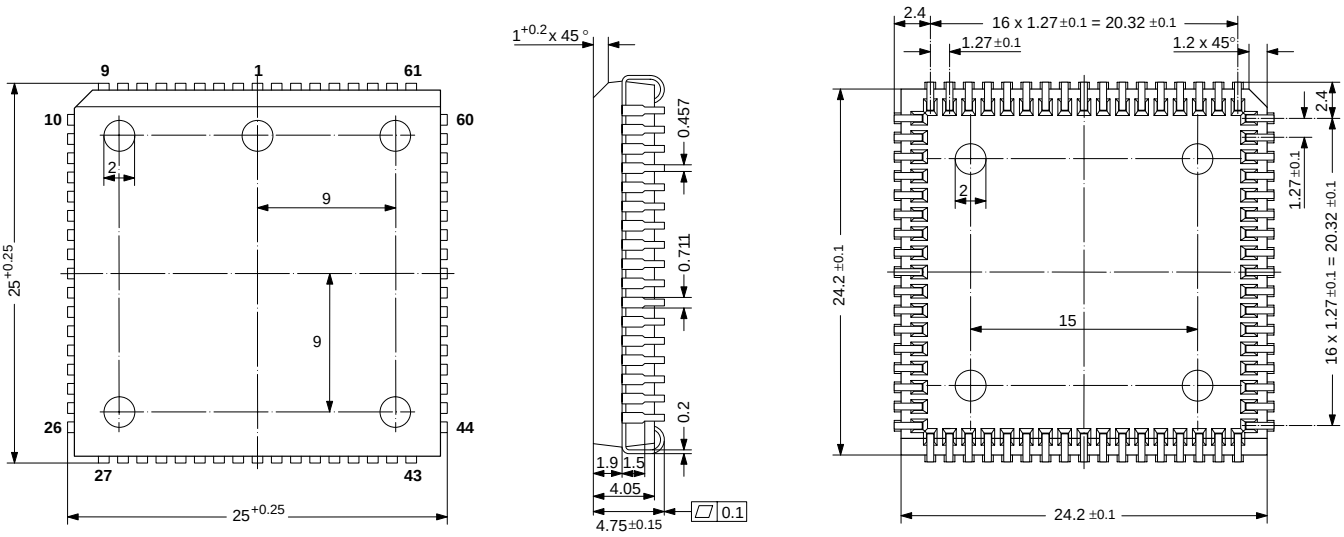


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Fig. 4–1:
68-pin Plastic Leaded Chip Carrier Package
(PLCC68)
Weight approx. 4.8 g
Dimensions in mm

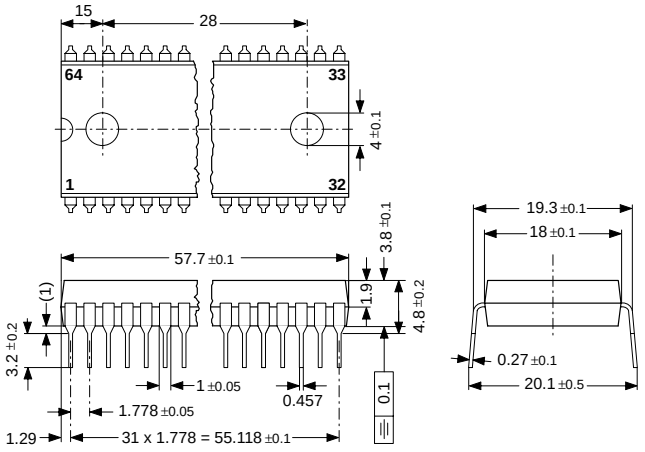

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Fig. 4–2:
64-Pin Plastic Shrink Dual-Inline-Package
(PSDIP64)
Weight approx. 9.0 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

IN = Input
OUT = Output

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Connection (if not used)	Pin Name	Type	Short Description
1	32	LV	MSY	OUT	Main Sync
2	–	GNDD	NC		Not connected
3	31	X	FSY	IN	Front Sync
4	30	X	CLK5	IN	5 MHz Clock
5	29	X	HOUT	OUT	Horizontal Drive Output
6	28	X	VSTBY		Stand-By Supply Voltage
7	27	H_{OUT}	HFLB	IN	Horizontal Flyback Input
8	26	GNDO	VPROT	IN	Vertical Protection Input
9	25	GNDO	SAFETY	IN	Safety Input
10	24	X	SCL	IN	I^2C-bus Clock
11	23	X	SDA	IN/OUT	I^2C-bus Data
12	22	GNDD	TEST	IN	Test Pin
13	21	X	$\overline{RES}$	IN	Reset Input
14	20	GNDO	RSW2	IN	Range Switch2, Measurement ADC
15	19	GNDO	RSW1	IN	Range Switch1, Measurement ADC
16	18	GNDO	SENSE	IN	Sense ADC Input
17	17	X	GNDM		Ground, MADC Input
18	16	LV	VERT	OUT	Vertical Sawtooth Output
19	15	LV	EW	OUT	Vertical Parabola Output
20	14	GNDD	NC		Not connected
21	13	X	XREF	IN	Reference Input for RGB DACs
22	–	GNDD	NC		Not connected
23	12	X	SVMOUT	OUT	Scan Velocity Modulation
24	11	VSUPO	ROUT	OUT	Analog Output Red
25	10	VSUPO	GOUT	OUT	Analog Output Green
26	9	VSUPO	BOUT	OUT	Analog Output Blue
27	8	X	GND_O		Ground, Analog Backend
28	7	X	VSUPO		Supply Voltage, Analog Backend

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Connection (if not used)	Pin Name	Type	Short Description
29	6	X	VRD/BCS	IN	DAC Reference, Beam Current Safety
30	5	GNDO	RIN	IN	Analog Red Input
31	4	GNDO	GIN	IN	Analog Green Input
32	3	GNDO	BIN	IN	Analog Blue Input
33	2	GNDO	FBLIN	IN	Fast Blank Input
34	–	GNDO	NC		Not connected
35	1	GNDD	OSD0	IN	Picture Bus OSD (LSB)
36	64	GNDD	OSD1	IN	Picture Bus OSD
37	63	GNDD	OSD2	IN	Picture Bus OSD
38	62	GNDD	OSD3	IN	Picture Bus OSD
39	61	GNDD	OSD4	IN	Picture Bus OSD (MSB)
40	60	X	FPDAT	IN/OUT	Deflection Data Interface to VPC
41	59	GNDD	PR2	IN	Picture Bus Priority (MSB)
42	58	GNDD	PR1	IN	Picture Bus Priority
43	57	GNDD	PR0	IN	Picture Bus Priority (LSB)
44	56	GNDD	C0	IN	Picture Bus Chroma (LSB)
45	55	GNDD	C1	IN	Picture Bus Chroma
46	54	GNDD	C2	IN	Picture Bus Chroma
47	53	GNDD	C3	IN	Picture Bus Chroma
48	52	GNDD	C4	IN	Picture Bus Chroma
49	51	GNDD	C5	IN	Picture Bus Chroma
50	50	GNDD	C6	IN	Picture Bus Chroma
51	49	GNDD	C7	IN	Picture Bus Chroma (MSB)
52	48	X	VSUPD		Supply Voltage, Digital Circuitry
53	47	X	GNDD		Ground, Digital Circuitry
54	46	X	CLK20	IN	20 MHz System Clock Input
55	45	GNDD	Y0	IN	Picture Bus Luma (LSB)
56	44	GNDD	Y1	IN	Picture Bus Luma
57	43	GNDD	Y2	IN	Picture Bus Luma
58	42	GNDD	Y3	IN	Picture Bus Luma
59	41	GNDD	Y4	IN	Picture Bus Luma

Pin No. PLCC 68-pin	Pin No. PSDIP 64-pin	Connection (if not used)	Pin Name	Type	Short Description
60	40	GNDD	Y5	IN	Picture Bus Luma
61	39	GNDD	NC		Not connected
62	38	GNDD	Y6	IN	Picture Bus Luma
63	37	GNDD	Y7	IN	Picture Bus Luma (LSB)
64	36	GNDD	NC		Not connected
65	–	X	GNDD		Ground, Digital Circuitry
66	35	GNDD	NC		Not connected
67	34	X	VSUPP		Supply Voltage, Output Pin Driver
68	33	LV	CSY	OUT	Composite Sync Output

4.3. Pin Descriptions (Pin Numbers for PLCC68)

NC = not connected

Pin 1 – Main Sync Signal Output **MSY** (Fig. 4–5)
This pin supplies the front end ICs with the main horizontal sync information, locked to the horizontal flyback. Also line number, field even/odd and vertical blanking information is included.

Pin 3 – Front Sync Signal Input **FSY** (Fig. 4–11)
This pin gets the front horizontal sync information from the video decoder VPC 32XX. Also skew, vertical sync, field even/odd and PAL-plus helper line indication is included.

Pin 4 – 5 MHz Clock Input **CLK5** (Fig. 4–7)
5 MHz clock required for HOUT and CSY generation during standby mode.

Pin 5 – Horizontal Drive **HOUT** (Fig. 4–13)
This open drain output supplies the drive pulse for the horizontal output stage. The gating with the flyback pulse is selectable by software.

Pin 6 – Standby Supply Voltage **VSTDBY**
In standby mode this pin supplies the horizontal drive circuitry.

Pin 7 – Horizontal Flyback Input **HFLB** (Fig. 4–9)
Via this pin the horizontal flyback pulse is supplied to the DDP.

Pin 8 – Vertical Protection Input **VPROT** (Fig. 4–9)
The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. During vertical blanking, a signal level of 2.5V is sensed. If a negative edge cannot be detected, the RGB output signals are blanked.

Pin 9 – Safety Input, **SAFETY** (Fig. 4–9)
This is a three-level input. Low level means normal function. At the medium level RGB signals are blanked and at high level RGB signals are blanked and horizontal drive is shut off.

Pin 10 – I^2C Clock Input **SCL** (Fig. 4–10)
Via this pin the clock signal for the I^2C-bus is supplied.

Pin 11 – I^2C Data Input/Output **SDA** (Fig. 4–10)
Via this pin the I^2C-bus data are written to or read from the DDP.

Pin 12 – Test Input **TEST** (Fig. 4–7)
This pin enables factory test modes. For normal operation it must be connected to ground.

Pin 13 – Reset Input **$\overline{\text{RES}}$** (Fig. 4–7)
A low level on this pin resets the DDP.

Pin 14,15 – Range Switch for Meas. ADC **RSW1 RSW2** (Fig. 4–14)
These pins are open drain pulldown outputs. During cut-off measurement both switches are off. During white drive measurement RSW1 is switched off and RSW2 is switched on. During the rest of time both switches are on.

Pin 16 – Measurement ADC Input **SENSE** (Fig. 4–9)
This is the input of the analog to digital converter for the picture and tube measurement. Three ranges of measurement are selectable with RSW1 and RSW2.

Pin 17 – Measurement ADC Reference Input **MGND**
This is the ground reference for the measurement A/D converter.

Pin 18 – Vertical Sawtooth Output **VERT** (Fig. 4–15)
This pin supplies the drive signal for the vertical output stage. The drive signal is generated with 15-bit precision by the Fast Processor in the VPC. The analog voltage is generated by a 4 bit current-DAC with external resistor and uses digital noise shaping.

Pin 19 – East-West Parabola Output **EW** (Fig. 4–15)
This pin supplies the parabola signal for the East-West correction. The drive signal is generated with 15 bit precision by the Fast Processor in the VPC. The analog voltage is generated by a 4 bit current-DAC with external resistor and uses digital noise shaping.

Pin 20 – NC

Pin 21 – DAC Current Reference **XREF** (Fig. 4–16)
External reference resistor for DAC output currents, typical 10 kΩ to adjust the output current of the D/A converters. (see recommended operating conditions). This resistor has to be connected to analog ground as closely as possible to the pin.

Pin 23 – Scan Velocity Modulation Output **SVMOUT** (Fig. 4–12)
This output delivers the analog SVM signal. The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50% of the maximum output current.

Pin 26,25,24 – Analog RGB Output **ROUT**,**GOUT**,**BOUT** (Fig. 4–12)
This are the analog Red/Green/Blue outputs of the backend. The outputs are current sinks with a maximum current of 8 mA.

Pin 27 – Ground, Analog Backend **GNDO**

Pin 28 – Supply Voltage, Analog Backend **VSUPO**

Pin 29 – DAC Reference Decoupling/Beam Current Safety **VRD/BCS** (Fig. 4–16)
Via this pin the DAC reference voltage is decoupled by an external capacitor. The DAC output currents depend on this voltage, therefore a pulldown transistor can be used to shut off all beam currents. A decoupling capacitor of 3.3 µF||100 nF is required.

Pin 32,31,30 – Analog RGB Input **RIN**,**GIN**,**BIN** (Fig. 4–9)
These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can by switched to the analog RGB outputs with the fast blank signal. The analog backend provides separate brightness and contrast settings for the external analog RGB signals.

Pin 33 – Fast Blank Input **FBLIN** (Fig. 4–9)
This pin is used to switch the RGB outputs to the external analog RGB inputs.

Pin 34 – NC

Pin 35...39 – Picture Bus OSD **OSD0...OSD4** (Fig. 4–11)
The Picture Bus OSD lines carry the digital OSD color data. They are used as address for the color lookup table.

Pin 40 – Deflection Data Interface **FPDAT** (Fig.4–6)
This is the bidirectional interface to the fast processor in the VPC for deflection data calculation.

Pin 41,42,43 – Picture Bus Priority **PR2–PR0** (Fig. 4–6)
The Picture Bus Priority lines carry the digital priority selection signals. The priority interface allows digital switching of up to 8 sources to the backend processor. Switching for different sources is prioritized and can be done from pixel to pixel.

Pin 44...51 Picture Bus Chroma **C0...C7** (Fig. 4–11)
The Picture Bus Chroma lines carry the digital chrominance data. The data are sampled at 20.25 MHz and multiplexed C_B C_R.

Pin 52 – Supply Voltage, Digital Circuitry **VSUPD**

Pin 53 – Ground, Digital Circuitry **GNDD**

Pin 54 – Main Clock Input **CLK20** (Fig. 4–8)
This is the 20.25 MHz main system clock that is used by all circuits in a high-end VPC system.

Pin 55...60, 62, 63 – Picture Bus Luma **L0...L7** (Fig. 4–11)
The Picture Bus Luma lines carry the digital luminance data. The data are sampled at 20.25 MHz.

Pin 61 – NC

Pin 64 – NC

Pin 65 – Ground, Digital Circuitry Input Reference **GNDD**

Pin 66 – NC

Pin 67 – Supply Voltage, Output Pin Driver **VSUPP**
This pin is used as supply for the following digital output pins : CSY, MSY.

Pin 68 – Composite Sync Output **CSY** (Fig. 4–5)
This output supplies a standard composite sync signal that is compatible to the analog RGB output signals.

4.4. Pin Configuration

The pin drawings show all signals for the 68-pin PLCC package (Fig. 4–3) and for the 64-pin Shrink DIP package (Fig. 4–4)

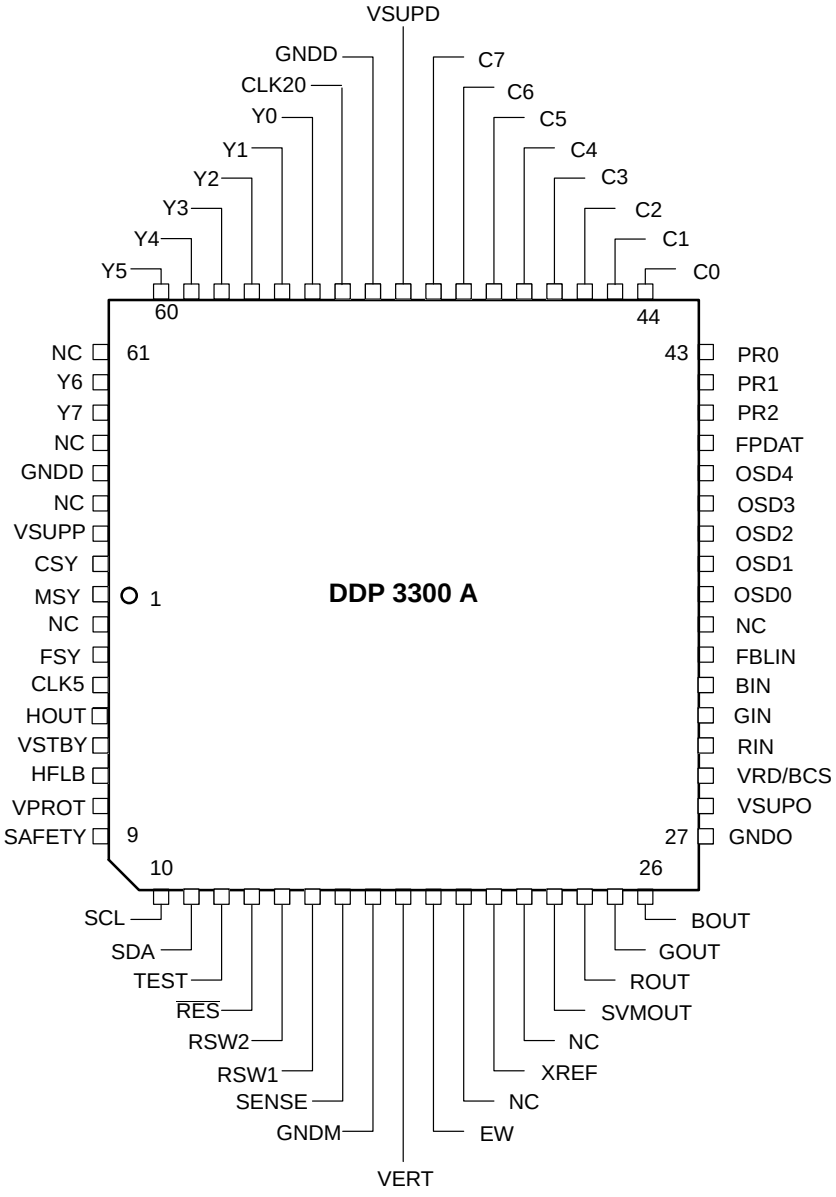

Fig. 4–3: Pinning of the DDP 3300 A in PLCC68 Package

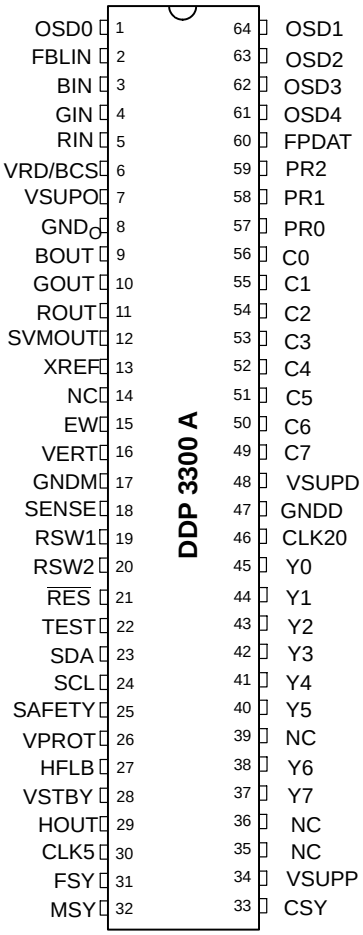

Fig. 4–4: Pinning of the DDP 3300 A in PSDIP64 Package

4.5. Pin Circuits

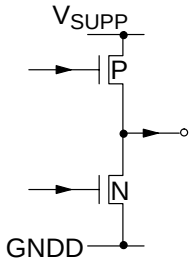

Fig. 4–5: Output pins MSY, CSY

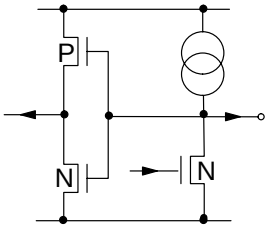

Fig. 4–6: I/O pins PR0, PR1, PR2, FPDAT

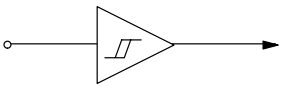

Fig. 4–7: Input pins TEST, $\overline{RES}$, CLK5

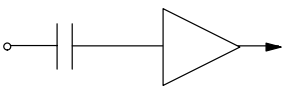

Fig. 4–8: Input pins CLK20

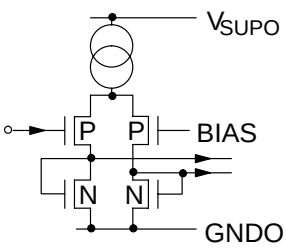

Fig. 4–9: Input pins SAFETY, VPROT, HFLB, FBLIN, RIN, BIN, GIN, SENSE

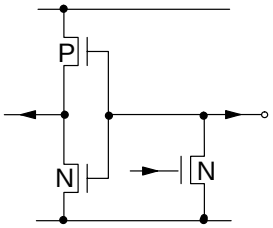

Fig. 4–10: I/O pins SCL, SDA

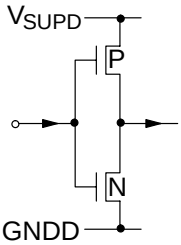

Fig. 4–11: Input pins C[7:0], L[7:0], OSD[4:0], FSY

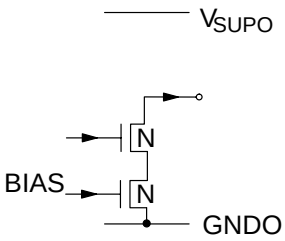

Fig. 4–12: Analog output pins ROUT, GOUT, BOUT, SVMOUT

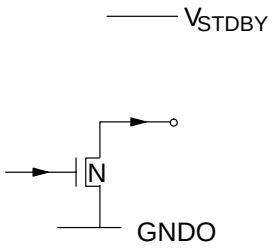

Fig. 4–13: Output pin HOUT

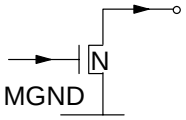

Fig. 4–14: Output pins RSW1, RSW2

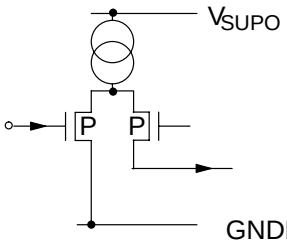

Fig. 4–15: Output pins for Vert and E/W

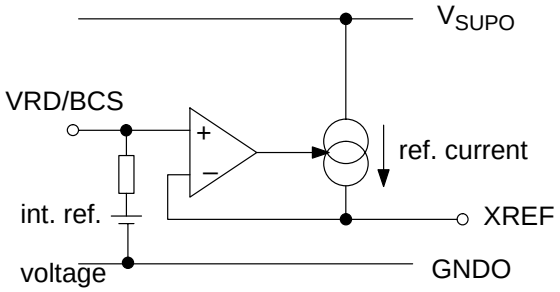

Fig. 4–16: Input pins XREF and VRD/BCS

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	−40	125	°C
V_{SUP}	Supply Voltage, all Supply Inputs		−0.3	6	V
V_I	Input Voltage, all Inputs		−0.3	$V_{SUP}+0.3$	V
V_O	Output Voltage, all Outputs		−0.3	$V_{SUP}+0.3$	V

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltages, all Supply Pins (but output pin driver supply)		4.75	5.0	5.25	V
V_{SUPP}	Output Pin Driver Supply Voltage	VSUPP	3.0	5.0	5.25	V
f_{sys}	Clock Frequency	CLK20		20.25		MHz
R_{xref}	RGB – DAC Current defining Resistor	XREF	9.5	10	10.5	kΩ
NS_{VDD}	Negative Slope of VDD (power down)	VSUPD			0.2	V/µs

4.6.3. Characteristics

Min./Max. values at: $T_A = 0$ to 65 °C, $V_{SUP} = 4.75$ to 5.25 V, $R_{xref} = 10$ kΩ, $f = 20.25$ MHz
Typical values at: $T_C = 60$ °C, $V_{SUP} = 5$ V, $R_{xref} = 10$ kΩ, $f = 20.25$ MHz

4.6.4. General Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
I_{VSUPO}	Current Consumption Analog Backend	VSUPO	58	70	85	mA
I_{VSUPD}	Current Consumption Digital Processing	VSUPD		70		mA
I_{VSUPP}	Current Consumption Output Pin Driver	VSUPP		TBD		mA
I_{VSTDBY}	Current Consumption Standby Circuit	VSTDBY		3		mA
P_{TOT}	Total Power Dissipation			0.74		W
I_L	Input and Output Leakage Current (if not otherwise specified)		–	–	1.0	µA

4.6.5. Bus Inputs: Luma, Chroma, OSD, Front Sync (see Fig. 4–17)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	Y[0..7] C[0..7] OSD[0:4] FSY	–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		7	–	–	ns	
t_{IH}	Input Hold Time		–	–	6	ns	

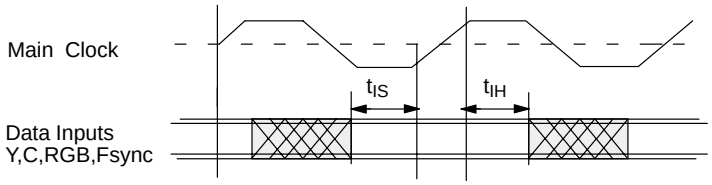

Fig. 4–17: Picture bus input timing

4.6.6. 20.25 MHz Main Clock Input, internally AC coupled (see Fig. 4–18)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IT}	Input Trigger Level	CLK20	2.1	2.5	2.9	V	
f_{Φ}	Φ Main Clock Frequency		10	20.25	24	MHz	
$V_{\Phi MIDC}$	Φ Main Clock Input DC Voltage		1.0	–	3.5	V	
$V_{\Phi MIAC}$	Φ M Clock Input AC Voltage (p–p)		0.8	–	2.5	V	
$\frac{t_{\Phi MIH}}{t_{\Phi MIL}}$	Φ M Clock Input High/Low Ratio		0.9	1.0	1.1		
$t_{\Phi MIHL}$	Φ M Clock Input High to Low Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$		
$t_{\Phi MILH}$	Φ M Clock Input Low to High Transition Time		–	–	$\frac{0.15}{f_{\Phi M}}$		

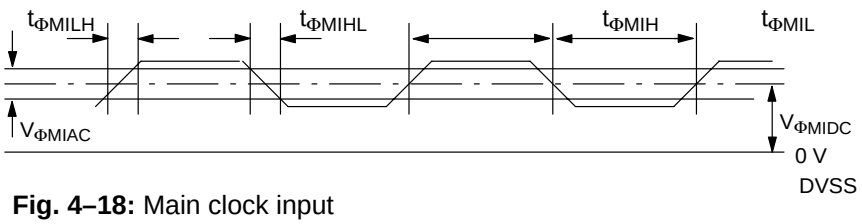

Fig. 4–18: Main clock input

4.6.7. 5 MHz Clock Input (see Fig. 4–19)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	CLK5	–	–	2.0	V	
V_{IH}	Input High Voltage		3.1	–	–	V	
t_F	Signal Fall Time		–	–	60	ns	
t_R	Signal Rise Time		–	–	60	ns	
f_{CK5}	Clock Frequency		4	–	6	MHz	

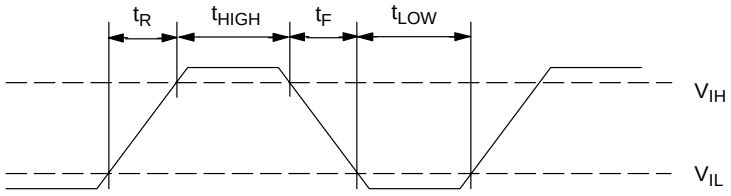

Fig. 4–19: 5 MHz clock input

4.6.8. I²C-Bus Interface

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	SDA SCL	–	–	1.5	V	
V_{IH}	Input High Voltage		3.0	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4 0.6	V V	I_I = 3mA I_I = 6mA
I_{OL}	Output Low Current		–	–	10	mA	
V_{IH}	Input Capacitance		–	–	TBD	pF	
t_F	Signal Fall Time		–	–	300	ns	C_L = 400 pF
t_R	Signal Rise Time		–	–	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	SCL	0	–	400	kHz	
t_{LOW}	Low Period of SCL		1.3	–	–	µs	
t_{HIGH}	High Period of SCL		0.6	–	–	µs	
$t_{SU\ Data}$	Data Set Up Time to SCL high	SDA	100	–	–	ns	
$t_{HD\ Data}$	DATA Hold Time to SCL low		0	–	0.9	µs	

4.6.9. Reset Input, Test Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	$\overline{RES}$ TEST	–	–	2.0	V	
V_{IH}	Input High Voltage		3.1	–	–	V	

4.6.10. Serial Deflection Interface

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	FPDAT	–	–	0.5	V	I_{OL} = 8 mA, strength 3 I_{OL} = 6 mA, strength 2 I_{OL} = 4 mA, strength 1 I_{OL} = 2 mA, strength 0
V_{OH}	Output High Voltage		1.8	2.0	2.5	V	$-I_{OL} < 10\ \mu A$ C_{LOAD} = 71pF
t_{OH}	Output Hold Time		6	–	TBD	ns	C_{LOAD} = 71pF I_{PL} = 8.4 mA
t_{ODL}	Output Delay Time		–	–	35	ns	C_{LOAD} = 71pF I_{PL} = 8.4 mA
I_{PL}	Output Pull-up Current		1.2	1.5	1.8	mA	V_{OL} = 0V
V_{IL}	Input Low Voltage		–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		7	–	–	ns	
t_{IH}	Input Hold Time		5	–	–	ns	

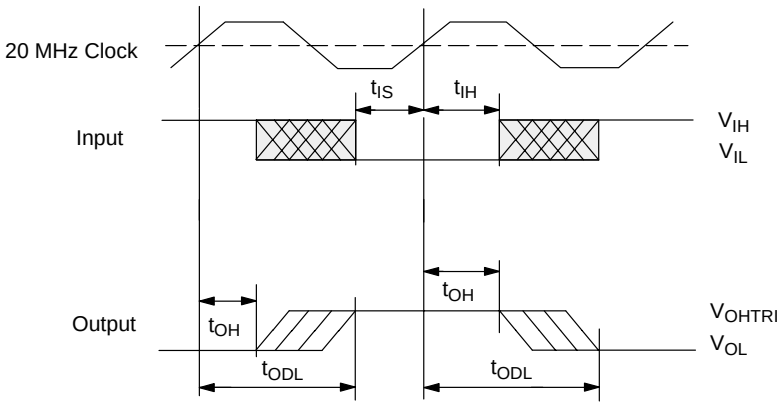

Fig. 4–20: Serial deflection interface

4.6.11. Priority Bus Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	PR[2:0]	–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		7	–	–	ns	
t_{IH}	Input Hold Time		5	–	–	ns	

4.6.12. Horizontal Flyback Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	HFLB	–	–	1.8	V	
V_{IH}	Input High Voltage		2.6	–	–	V	
V_{IHST}	Input Hysteresis		0.1	–	–	V	
$PSRR_{HF}$	Power Supply Rejection Ratio of Trigger Level		0			dB	f = 20 MHz
$PSRR_{MF}$	Power Supply Rejection Ratio of Trigger Level		–20			dB	f < 15 kHz
$PSRR_{LF}$	Power Supply Rejection Ratio of Trigger Level		–40			dB	f < 100 Hz
t_{PID}	Internal Delay				12	ns	slew rate 500 mV/ns swing 1 V_{PP}

4.6.13. Main Sync Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	MSY	–	0.2	0.4	V	I_{OL} = 1.6 mA, strength 7
V_{OH}	Output High Voltage		V_{SUPP} – 0.4	–	V_{SUPP}	V	$-I_{OL}$ = 1.6mA, strength 7
t_{OH}	Output Hold Time		6	14	TBD	ns	C_{LOAD} = 70pF
t_{OD}	Output Delay Time		–	–	35	ns	C_{LOAD} = 70pF
I_{OL}	Output Current		–10	–	10	mA	driver imp. = 0

4.6.14. Combined Sync Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	CSY	–	–	0.4	V	I_{OL} = 1.6 mA strength 7
V_{OH}	Output High Voltage		V_{SUPP} – 0.4	–	V_{SUPP}	V	$-I_{OL}$ = 1.6 mA strength 7
t_{OT}	Output Transition Time		–	10	20	ns	C_{LOAD} = 30 pF
I_{OL}	Output Current		–10	–	10	mA	driver imp . = 0

4.6.15. Horizontal Drive Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	HOUT	–	–	0.4	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (Open Drain Stage)		–	–	8	V	external pull-up resistor
t_{OF}	Output Fall Time		–	8	20	ns	C_{LOAD} = 30pF
I_{OL}	Output Low Current		–	–	10	mA	

4.6.16. Vertical Protection Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	VPROT	–	–	1.8	V	
V_{IH}	Input High Voltage		2.6	–	–	V	
V_{IHST}	Input Hysteresis		0.1	–	–	V	

4.6.17. Vertical Safety Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{ILA}	Input Low Voltage A	SAFETY	–	–	1.8	V	
V_{IHA}	Input High Voltage A		2.6	–	–	V	
V_{ILB}	Input Low Voltage B		–	–	3.1	V	
V_{IHB}	Input High Voltage B		3.9	–	–	V	
V_{IHST}	Input Hysteresis A and B		0.1	–	–	V	
t_{PID}	Internal Delay				100	ns	

4.6.18. Vertical and East/West Drive Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Voltage LOW	EW VERT		0		V	R_{load} = 6800 R_{xref} = 10 kΩ
V_{OH}	Output Voltage HIGH		2.82	3	3.2	V	R_{load} = 6800 R_{xref} = 10 kΩ
I_{dacn}	Full scale DAC Output Current		415	440	465	µA	Vo = 0V R_{xref} = 10 kΩ
PSRR	Power Supply Rejection Ratio		20	–	–	dB	

4.6.19. Sense A/D Converter Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_I	Input Voltage Range	SENSE	0	–	V_{sup}	V	
V_{I255}	Input Voltage for code 255		1.4	1.54	1.7	V	Read cutoff blue register
C_0	Digital Output for zero Input				16	LSB	Offset check, read cutoff blue register
R_I	Input Impedance		1	–	–	MΩ	
Range Switch Outputs							
R_{ON}	Output On Resistance	RSW1 RSW2	–	–	50	Ω	I_{OL} = 10 mA
I_{Max}	Maximum Current		–	–	15	mA	
I_{LEAK}	Leakage Current		–	–	600	nA	RSW High Impedance
C_{IN}	Input Capacitance		–	–	TBD	pF	

4.6.20. Analog RGB and FB Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{RGBIN}	External RGB Inputs Voltage Range	RIN GIN BIN	–0.3	–	1.1	V	
V_{RGBIN}	nominal RGB Input Voltage peak-to-peak		0.5	0.7	1.0	V_{PP}	SCART Spec: 0.7 V ±3 dB
V_{RGBIN}	RGB Inputs Voltage for Maximum Output Current			0.44			Contrast setting: 511
	RGB Inputs Voltage for Maximum Output Current			0.7			Contrast setting: 323
	RGB Inputs Voltage for Maximum Output Current			1.1			Contrast setting: 204
C_{RGBIN}	External RGB Input Coupling Capacitor			15		nF	
	Clamp Pulse Width		3.1			µs	
C_{IN}	Input Capacitance		–	–	13	pF	
I_{IL}	Input Leakage Current		–0.5	–	0.5	µA	Clamping OFF, V_{IN} –0.3..3 V
V_{CLIP}	RGB Input Voltage for Clipping Current			2		V	
V_{CLAMP}	Clamp Level at Input		40	60	80	mV	Clamping ON
V_{INOFF}	Offset Level at Input		–10		10	mV	Extrapolated from V_{IN} = 100 mV and 200 mV
V_{INOFF}	Offset Level Match at Input		–10		10	mV	Extrapolated from V_{IN} = 100 mV and 200 mV
R_{CLAMP}	Clamping-ON-Resistance			140	–	Ω	
V_{FBLOFF}	FBLIN Low Level	FBLIN	–	–	0.5	V	
V_{FBLON}	FBLIN High Level		0.9	–	–	V	
$V_{FBLTRIG}$	Fast Blanking Trigger Level typical			0.7			
t_{PID}	Delay Fast Blanking to RGB_{OUT} from midst of FBLIN–transition to 90% of RGB_{OUT}– transition			8	15	ns	Internal RGB = 3.75 mA Full Scale Int. Brightness = 0 External Brightness = 1.5 mA (Full Scale) RGBin = 0 V_{FBLOFF} = 0.4 V V_{FBLON} = 1.0 V Rise and fall time = 2 ns
	Difference of Internal Delay to External RGBin Delay		–5		+5	ns	
	Switch-Over-Glitch			0.5		pAs	Switch from 3.75 mA (int) to 1.5 mA (ext)

4.6.21. Analog RGB Outputs, D/A Converters

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Internal RGB Signal D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	10	–	bit	
I_{OUT}	Full Scale Output Current		3.6	3.75	3.9	mA	R_{ref} = 10 kΩ
I_{OUT}	Differential Nonlinearity				0.5	LSB	
I_{OUT}	Integral Nonlinearity				1	LSB	
I_{OUT}	Glitch Pulse Charge			0.5		pAs	Ramp signal, 25 Ω output termination
I_{OUT}	Rise and Fall Time			3		ns	10% to 90%, 90% to 10%
I_{OUT}	Intermodulation				–50	dB	2/2.5MHz full scale
I_{OUT}	Signal to Noise		+50			dB	Signal: 1MHz full scale Bandwidth: 10MHz
I_{OUT}	Matching R–G, R–B, G–B		–2		2	%	
	R/B/G Crosstalk one channel talks two channels talk				–46	dB	Passive channel: I_{OUT} =1.88 mA Crosstalk–Signal: 1.25 MHz, 3.75 mA_{PP}
	RGB Input Crosstalk from external RGB one channel talks two channels talk three channels talk				 –50 –50 –50	 dB dB dB	
Internal RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT		9		bits	
I_{BR}	Full Scale Output Current relative		39.2	40	40.8	%	Ref to max. digital RGB
I_{BR}	Full Scale Output Current absolute			1.5		mA	
I_{BR}	differential nonlinearity				0.5	LSB	
I_{BR}	integral nonlinearity				1	LSB	
I_{BR}	Match R–G, R–B, G–B		–2		2	%	
I_{BR}	Match to digital RGB R–R, G–G, B–B		–2		2	%	
External RGB Voltage/Current Converter Characteristics							
	Resolution	ROUT GOUT BOUT		9		bits	
I_{EXOUT}	Full Scale Output Current relative		96	100	104	%	Ref. to max. Digital RGB V_{IN} = 0.7 V_{PP}, contrast = 323
	Full Scale Output Current absolute			3.75		mA	Same as Digital RGB
CR	Contrast Adjust Range			16:511			

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
	Gain Match R–G, R–B, G–B	ROUT GOUT BOUT	–2		2	%	Measured at RGB Outputs V_{IN} = 0.7 V, contrast = 323
	Gain Match to RGB–DACs R–R, G–G, B–B		–3		3	%	Measured at RGB Outputs V_{IN} = 0.7 V, contrast = 323
	R/B/G Input Crosstalk one channel talks two channels talk				–46	dB	Passive channel: V_{IN} = 0.7V, contrast = 323
	RGB Input Crosstalk from Internal RGB one channel talks two channels talk tree channels talk				–50	dB	Crosstalk signal: 1.25 MHz, 3.75 mA_{PP}
	RGB Input Noise and Distortion				–50	dB	V_{IN}=0.7 V_{PP} at 1 MHz contrast = 323 Bandwidth: 10 MHz
	RGB Input Bandwidth –3dB		10	15	–	MHz	V_{IN} = 0.7 V_{PP}, contrast =323
	RGB Input THD		–50 –40			dB dB	Input signal 1 MHz Input signal 6 MHz V_{IN} = 0.7 V_{PP} contrast =323
	Differential Nonlinearity of Contrast Adjust				1.0	LSB	V_{IN} = 0.44V
	integral nonlinearity of Contrast Adjust				7	LSB	
V_{RGBO}	R,G,B Output Voltage		–1.0		0.3	V	Referred to V_{SUPO}
	R,G,B Output Load Resistance				100	Ω	Ref. to V_{SUPO}
V_{OUTC}	RGB Output Compliance		–1.5	–1.3	–1.2	V	Ref. to V_{SUPO} Sum of max. Current of RGB–DACs and max. Current of Int. Brightness DACs is 2% degraded
External RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT		9		bits	
I_{EXBR}	Full Scale Output Current relative		39.2	40	40.8	%	Ref to max. digital RGB
	Full Scale Output Current absolute			1.5		mA	
	Differential Nonlinearity				0.5	LSB	
	Integral Nonlinearity				1	LSB	
	Matching R–G, R–B, G–B		–2		2	%	
	Matching to digital RGB R–R, G–G, B–B		–2		2	%	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
RGB Output Cutoff D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT		9		bits	
I_{CUT}	Full Scale Output Current relative		58.8	60	61.2	%	Ref to max. digital RGB
I_{CUT}	Full Scale Output Current absolute			2.25		mA	
I_{CUT}	Differential nonlinearity				0.5	LSB	
I_{CUT}	Integral nonlinearity				1	LSB	
I_{CUT}	Match to digital RGB R–R, G–G, B–B		–2		2	%	
RGB Output Ultrablack D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT		1		bits	
I_{UB}	Full Scale Output Current relative		19.6	20	20.4	%	Ref to max. digital RGB
	Full Scale Output Current absolute			0.75		mA	
	Match to digital RGB R–R, G–G, B–B		– 2		2	%	

4.6.22. DAC Reference, Beam Current Safety

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{DACREF}	DAC–Ref. Voltage	VRD/BCS	2.38	2.50	2.67	V	
	DAC–Ref. Output resistance	VRD/BCS	18	25	32	kΩ	
V_{XREF}	DAC–Ref. Voltage Bias Current Generation	XREF	2.25	2.34	2.43	V	

4.6.23. Scan Velocity Modulation Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
SVM D/A Converter Characteristics							
	Resolution	SVMOUT		8		bit	
I_{OUT}	Full Scale Output Current		1.55	1.875	2.25	mA	
I_{OUT}	Differential Nonlinearity				0.5	LSB	
I_{OUT}	Integral Nonlinearity				1	LSB	
I_{OUT}	Glitch Pulse Charge			0.5		pAs	Ramp, output line is terminated on both ends with 50 Ohms
I_{OUT}	Rise and Fall Time			3		nsec	10% to 90%, 90% to 10%

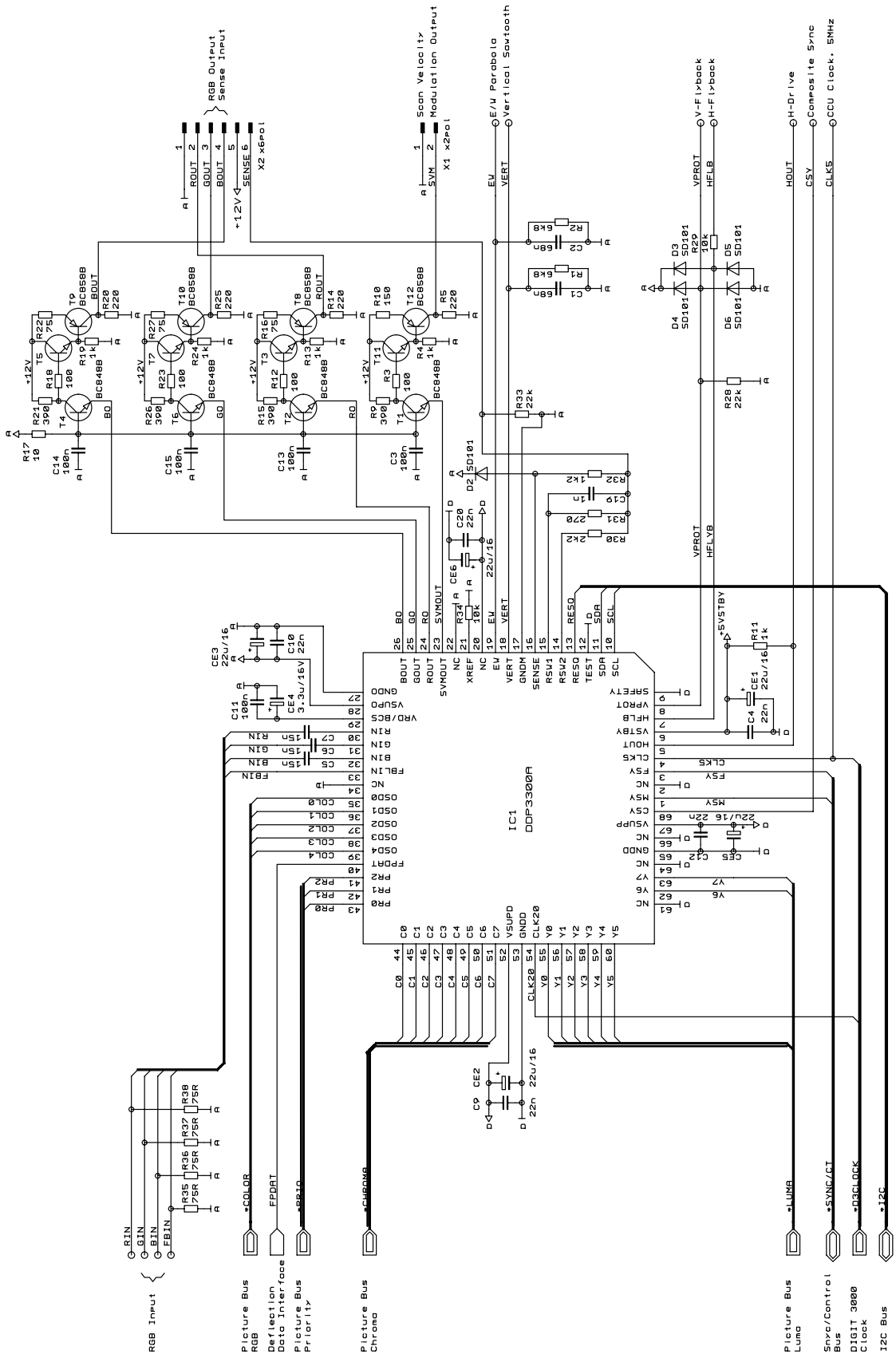

Fig. 5–1: Application diagram

5. Data Sheet History

1. Advance information: “DDP 3300 A”, Feb. 9, 1996, 6251-421-1AI. First release of the advance information.

2. Preliminary data sheet: “DDP 3300 A”, June 19, 1996, 6251-421-1PD. First release of the preliminary data sheet.

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Printed in Germany
Order No. 6251-421-1PD

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