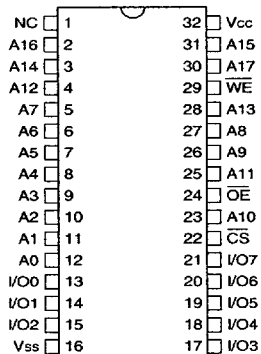




256Kx8 SRAM MODULE

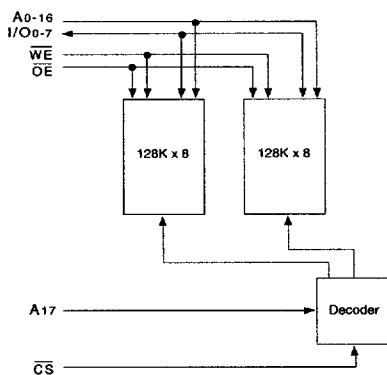
FIG. 1

PIN CONFIGURATION
TOP VIEW

PIN DESCRIPTION

A0-17	Address Inputs
I/O0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

BLOCK DIAGRAM



FEATURES

- Access Times 55, 70, 85, 100, 120ns
- Standard Microcircuit Drawing, 5962-93157
- MIL-STD-883 Compliant Devices Available
- JEDEC Standard 32 pin, Hermetic Ceramic DIP (Package 300)
- Commercial, Industrial and Military Temperature Ranges
- Organized as 256K x 8
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Battery Back-Up Operation

SRAM MODULES



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _g	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	40	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	40	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

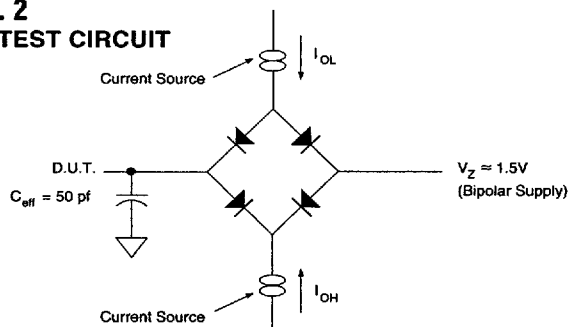
Parameter	Sym	Conditions	-55		-70		-85		-100		-120		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10		10		10		10		10	μA
Output Leakage Current	I _{LO}	$\overline{\text{CS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10		10		10		10		10	μA
Operating Supply Current	I _{CC}	$\overline{\text{CS}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz, V _{CC} = 5.5		130		90		80		70		70	mA
Standby Current	I _{SB}	$\overline{\text{CS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz		50		30		2.5		1.5		1.5	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5		0.4		0.4		0.4		0.4		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4		2.4		2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	-55			-70			-85			-100			-120			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	$\overline{\text{CS}} \geq \text{V}_{\text{CC}} - 0.2\text{V}$	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention	I _{CCDR1}	V _{CC} = 3V		30	6400		30	2000		10	1000		10	1000		10	1000	μA

FIG. 2
AC TEST CIRCUIT

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.

**AC CHARACTERISTICS**(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-55		-70		-85		-100		-120		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle												
Read Cycle Time	t _{RC}	55		70		85		100		120		ns
Address Access Time	t _{AA}		55		70		85		100		120	ns
Output Hold from Address Change	t _{OH}	3		5		15		15		15		ns
Chip Select Access Time	t _{ACS}		55		70		85		100		120	ns
Output Enable to Output Valid	t _{OE}		40		50		55		60		60	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	5		5		10		10		10		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	0		5		5		5		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		35		40		45		50		50	ns
Output Disable to Output in High Z	t _{OHZ} ¹		30		40		45		50		50	ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-55		-70		-85		-100		-120		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle												
Write Cycle Time	t _{WC}	55		70		85		100		120		ns
Chip Select to End of Write	t _{CW}	45		65		80		90		110		ns
Address Valid to End of Write	t _{AW}	50		50		75		75		85		ns
Data Valid to End of Write	t _{DW}	30		40		45		50		50		ns
Write Pulse Width	t _{WP}	40		40		65		70		80		ns
Address Setup Time	t _{AS}	2		2		2		2		2		ns
Address Hold Time	t _{AH}	2		2		2		2		2		ns
Output Active from End of Write	t _{OW} ¹	5		10		10		10		10		ns
Write Enable to Output in High Z	t _{WHZ} ¹	0	30	0	40	0	45	0	50	0	50	ns
Data Hold Time	t _{DH}	1		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.



FIG. 3
TIMING WAVEFORM - READ CYCLE

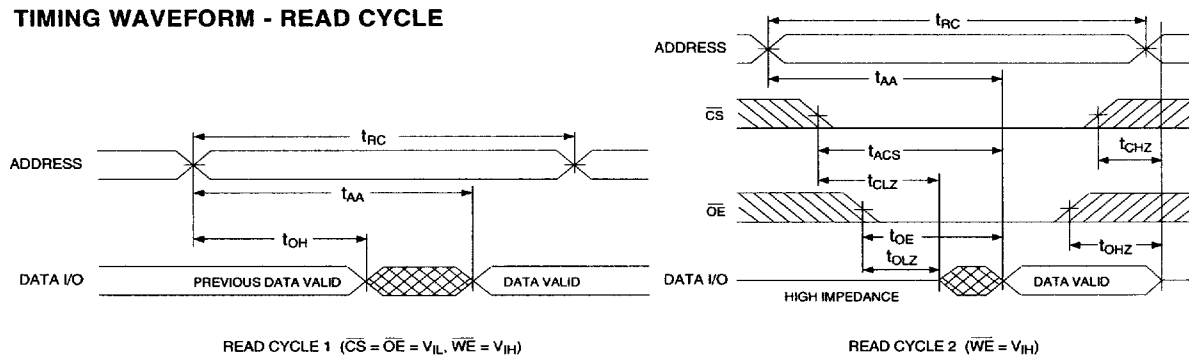


FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED

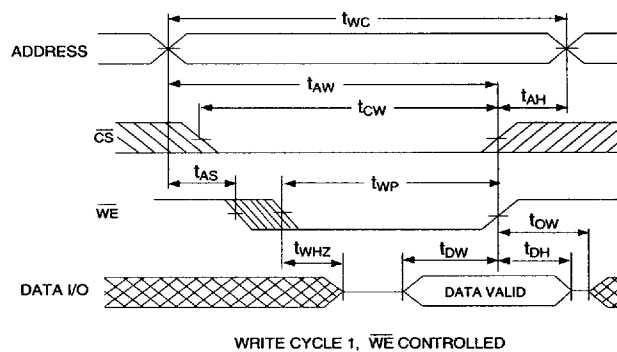
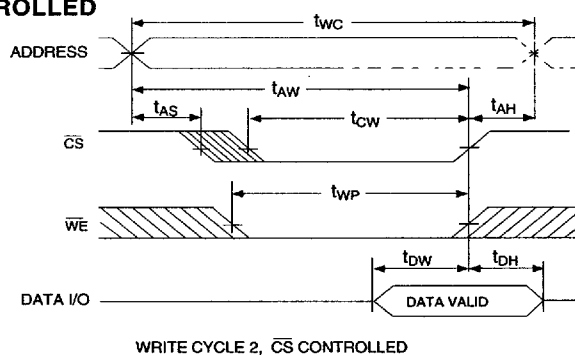
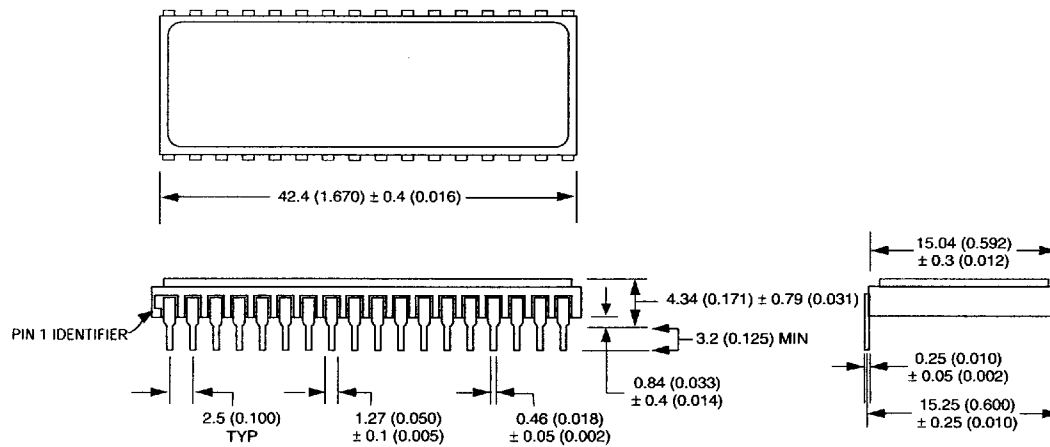


FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED





PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

SRAM MODULES



ORDERING INFORMATION

W S 256K 8 - XXX C X

DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE:

C = Ceramic 0.600" DIP (Package 300)

ACCESS TIME in ns

ORGANIZATION, 256K x 8

SRAM

WHITE MICROELECTRONICS

SRAM MODULES

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
256K x 8 SRAM	120ns	32 pin DIP	5962-93157 01HXX
256K x 8 SRAM	100ns	32 pin DIP	5962-93157 02HXX
256K x 8 SRAM	85ns	32 pin DIP	5962-93157 03HXX
256K x 8 SRAM	70ns	32 pin DIP	5962-93157 04HXX
256K x 8 SRAM	55ns	32 pin DIP	5962-93157 05HXX