Data Sheet | March 15, 2005 | FN8150.0

Hot Swap Controller with Advanced Fault Protection and Voltage Regulator Output

FEATURES

- **Hot swap controller**
  - Overvoltage and undervoltage protection
  - Undervoltage lockout for battery/redundant supplies
  - Electronic circuit breaker
  - Slew Rate for External FET Gate Control
  - Overcurrent Detection and Gate Shut-off
  - 3X overcurrent limit on insertion
  - 5µs overcurrent filter
  - Hardshort Retry and Indicator
  - Typically operates from -30V to -80V. Tolerates transients to -200V (limited by external components)
  - Positive Voltages (low side switching) from 12V to 60V
  - Soft Re-insertion
  - Soft extraction
- **Battery backup mode**
- **Hardshort retry**
- **Overcurrent Filter**
- **Insertion Limits.**
- **Selectable Gate Current**
- **Voltage Regulator Output for Supervisory Functions**
- **Debounced manual reset input**
- **Available packages**
  - 20-lead Quad No-Lead Frame (QFN)

APPLICATIONS

- **-48V Hot Swap Power Backplane/Distribution Central Office, Ethernet for VOIP**
- **Positive Voltage Hotswap 12V to 60V Applications (low side switching)**
- **Card Insertion Detection**
- **IP Phone Applications**
- **Databus Power Interfacing**
- **Custom Industrial Power Backplanes**
- **Distributed Power Systems**

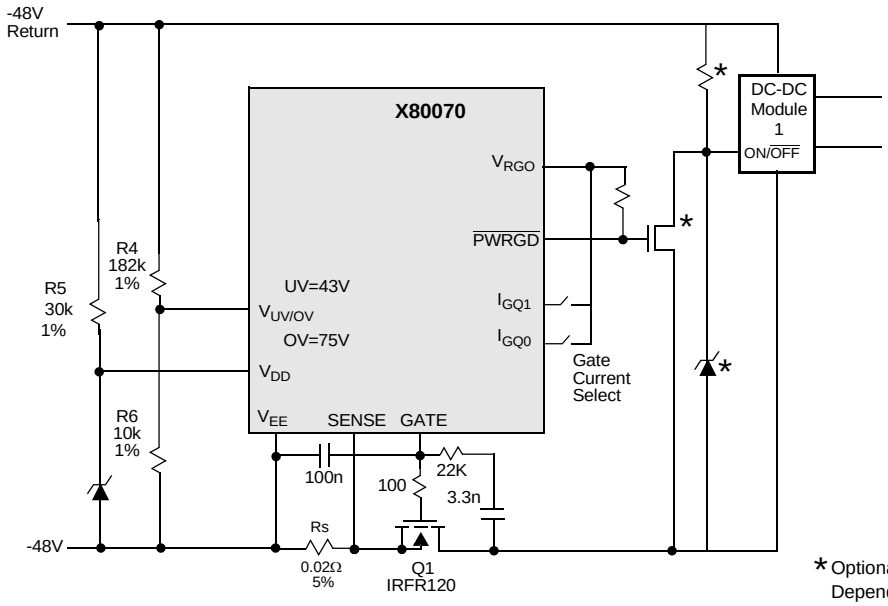
DESCRIPTION

The X80070 is a hot swap controller that allows a board to be safely inserted and removed from a live backplane without turning off the main power supply.

During insertion, the gate of an external power MOSFET is clamped low to suppress contact bounce. The undervoltage/overvoltage circuits and the power-on reset circuitry suppress the gate turn on until the mechanical bounce has ended. The X80070 turns on the gate with a slew rate to limit the inrush current and incorporates an electronic circuit breaker set by a sense resistor. After the load is successfully charged, the $\overline{\text{PWRGD}}$ signal is asserted; indicating that the device is ready to power sequence the DC-DC power bricks.

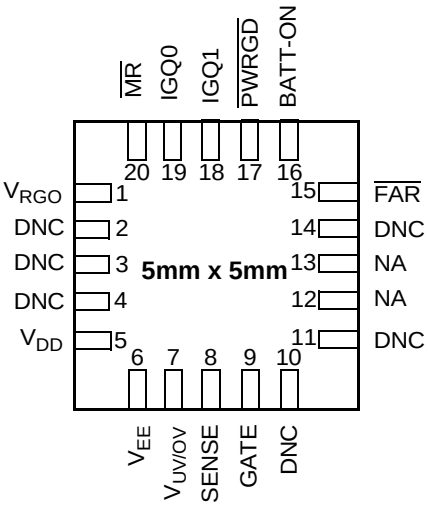
At all times, the X80070 monitors for undervoltage, overvoltage, and overcurrent conditions. If any fault occurs, the gate will be immediately shut off and the $\overline{\text{PWRGD}}$ will be returned to the inactive state. The X80070 contains overvoltage, undervoltage and overcurrent detection, hardshort retry, gate control slew rate and power good control.

TYPICAL APPLICATION



ORDERING INFORMATION

QFN package
(Top view)



ORDER NUMBER	OV (V)	UV1 (V)	UV2 (V)	t_{NF} (us)	V_{OC} (mV)	V_{OCI} (mV)	Over-current Retry	Retry Delay (ms)	I_{GATE} (uA)	T_{DELAY} (ms)	t_{POR} (ms)	Temp	PART MARK
X80070Q20I	74.9	42.4	33.2	5	50	150	Always	100	50	100	100	-40°C to 85°C	80070I
X80071Q20I	68.0	42.4	33.2	5	50	150	Always	100	50	100	100	-40°C to 85°C	80071I
X80072Q20I	74.9	42.4	33.2	5	50	150	5 retries	100	50	100	100	-40°C to 85°C	80072I
X80073Q20I	68.0	42.4	33.2	5	50	150	5 retries	100	50	100	100	-40°C to 85°C	80073I

ABSOLUTE MAXIMUM RATINGS

Temperature under bias .....-65°C to +135°C
Storage temperature .....-65°C to +150°C
Voltage on given pin (Hot Side Functions):
$V_{ov\ /\ uv\ pin}$ ..... 5.5V + V_{EE}
SENSE pin ..... 400mV + V_{EE}
V_{EE} pin ..... -80V
$\overline{PWRGD}$ pin ..... 7 V + V_{EE}
GATE pin ..... V_{DD} + V_{EE}
$\overline{FAR}$ pin ..... 7V + V_{EE}
$\overline{MR}$ pin ..... 5.5V + V_{EE}
BATT-ON pin ..... 5.5V + V_{EE}

Voltage on given pin (Cold Side Functions):
IGQ1 and IGQ0 pins ..... 5.5V + V_{EE}
V_{DD} pin ..... 14V + V_{EE}
D.C. output current 5mA
Lead temperature (soldering, 10 seconds) .....300°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Industrial	-40°C	+85°C

Supply Voltage
V_{DD} = 12V

ELECTRICAL CHARACTERISTICS (Standard Settings)

(Over the recommended operating conditions unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
DC Characteristics						
V_{DD}	Supply Operating Range	10	12	14	V	
I_{DD}	Supply Current		2.5	5	mA	
V_{RGO}	Regulated 5V output	4.5		5.5		I_{RGO} = 10uA
I_{RGO}	V_{RGO} current output			50	µA	
I_{GATE}	Gate Pin Current	46.2	52.5	58.8	µA	Gate Drive On, $V_{GATE} = V_{EE}$, $V_{SENSE} = V_{EE}$ (sourcing)
			9		mA	$V_{GATE} - V_{EE}$ = 3V $V_{SENSE}-V_{EE}$ = 0.1V (sinking)
V_{GATE}	External Gate Drive (Slew Rate Control)	V_{DD}-1		V_{DD}	V	I_{GATE} = 50uA
V_{PGA}	Power Good Threshold ($\overline{PWRGD}$ High to Low)	0.9	1	1.1	V	Referenced to V_{EE} $V_{UV1} < V_{UV/OV} < V_{OV}$
V_{IHB}	Voltage Input High (BATT-ON)	V_{EE} + 4		V_{EE} + 5	V	
V_{ILB}	Voltage Input Low (BATT-ON)			V_{EE} + 2	V	
I_{LI}	Input Leakage Current ($\overline{MR}$, IGQ0, IGQ1)			10	µA	V_{IL} = GND to V_{CC}
I_{LO}	Output Leakage Current ($\overline{PWRGD}$)			10	µA	Gate is Off
V_{IL}	Input LOW Voltage ($\overline{MR}$, IGQ0, IGQ1)	-0.5 + V_{EE}		(V_{EE} + 5) x 0.3	V	
V_{IH}	Input HIGH Voltage ($\overline{MR}$, IGQ0, IGQ1)	(V_{EE} + 5) x 0.7		(V_{EE} + 5) + 0.5	V	
V_{OL}	Output LOW Voltage ($\overline{FAR}$, $\overline{PWRGD}$)			V_{EE} + 0.4	V	I_{OL} = 4.0 mA (V_{EE} + 2.7 to V_{EE} + 5.5V) I_{OL} = 2.0 mA (V_{EE} + 2.7 to V_{EE} + 3.6V)
C_{OUT}(1)	Output Capacitance ($\overline{FAR}$)			8	pF	V_{OUT} = 0V
C_{IN}(1)	Input Capacitance ($\overline{MR}$)			6	pF	V_{IN} = 0V
V_{OC}	Overcurrent threshold	45	50	55	mV	$V_{OC} = V_{SENSE} - V_{EE}$
V_{OCI}	Overcurrent threshold (Insertion)	135	150	165	mV	$V_{OC} = V_{SENSE} - V_{EE}$ $\overline{PWRGD}$ = HIGH Initial Power-up condition
V_{OVR}	Overvoltage threshold (rising) X80070, X80072 X80071, X80073	3.85 3.49	3.90 3.54	3.95 3.59	V	Referenced to V_{EE}
V_{OVF}	Overvoltage threshold (falling) X80070, X80072 X80071, X80073	3.82 3.46	3.87 3.51	3.92 3.56	V	Referenced to V_{EE}
V_{UV1R}	Undervoltage 1 threshold (rising)	2.19	2.24	2.29	V	Referenced to V_{EE} BATT-ON = V_{EE}
V_{UV1F}	Undervoltage 1 threshold (falling)	2.16	2.21	2.26	V	
V_{UV2R}	Undervoltage 2 threshold (rising)	1.71	1.76	1.81	V	Referenced to V_{EE} BATT-ON = V_{RGO}
V_{UV2F}	Undervoltage 2 threshold (falling)	1.68	1.73	1.78	V	
AC Characteristics						
t_{FOC}	Sense High to Gate Low	1.5	2.5	3.5	µs	

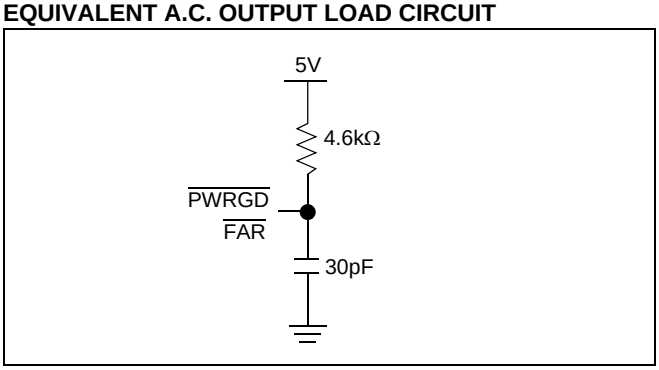
ELECTRICAL CHARACTERISTICS (Standard Settings) **(Continued)**

(Over the recommended operating conditions unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{FUV}	Undervoltage conditions to Gate Low	0.5	1.0	1.5	µs	
t_{FOV}	Overvoltage Conditions to Gate Low	1.0	1.5	2	µs	
t_{VFR}	Overvoltage/undervoltage failure recovery time to Gate =1V.	1.2	1.6	2	µs	V_{DD} does not drop below 3V, No other failure conditions.
$t_{BATT-ON}$	Delay BATT-ON Valid		100		ns	
t_{MR}	Minimum time high for reset valid on the $\overline{MR}$ pin	5			µs	
t_{MRE}	Delay from $\overline{MR}$ enable to Gate Pin LOW	1.0	1.6	2.4	µs	I_{GATE} = 60µA, No Load
t_{MRD}	Delay from $\overline{MR}$ disable to GATE reaching 1V	1.8		2.6	µs	I_{GATE} = 60µA, No Load
t_{QC}	Delay from IGQ1 and IGQ0 to valid Gate pin current			1	µs	
t_{SC_RETRY}	Delay between Retries	90	100	110	ms	
t_{NF}	Noise Filter for Overcurrent	4.5	5	5.5	µs	
t_{DPOR}	Device Delay before Gate assertion	45	50	55	ms	

Notes: (1) This parameter is based on characterization data.

EQUIVALENT A.C. OUTPUT LOAD CIRCUIT



A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing levels	V_{CC} x 0.5
Output load	Standard output load

Figure 1. Overvoltage/Undervoltage GATE Timing

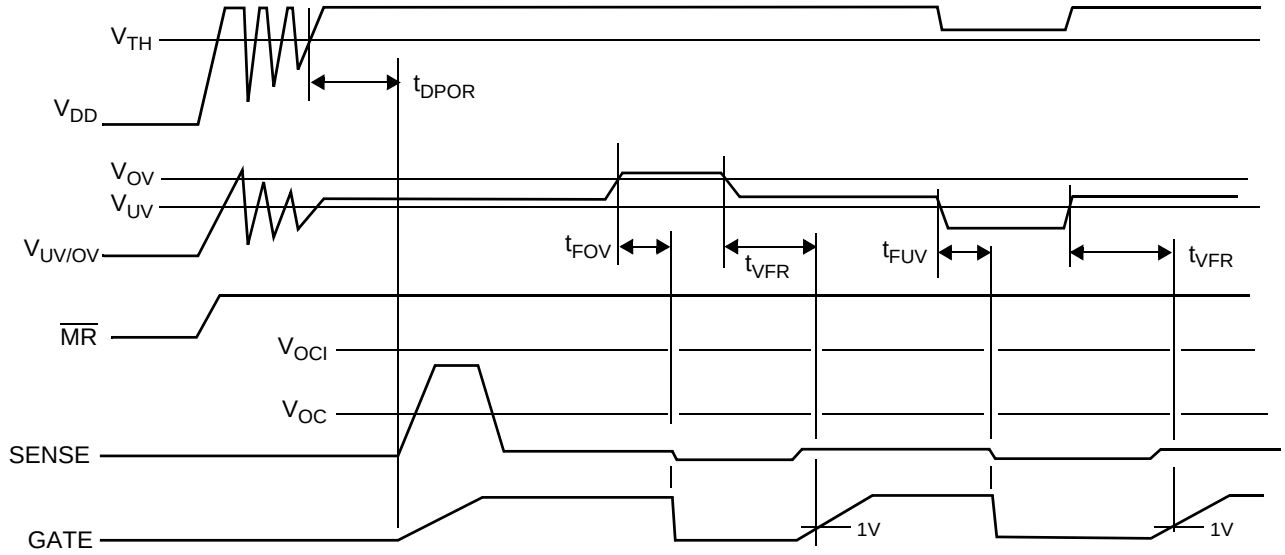


Figure 2. Overcurrent GATE Timing

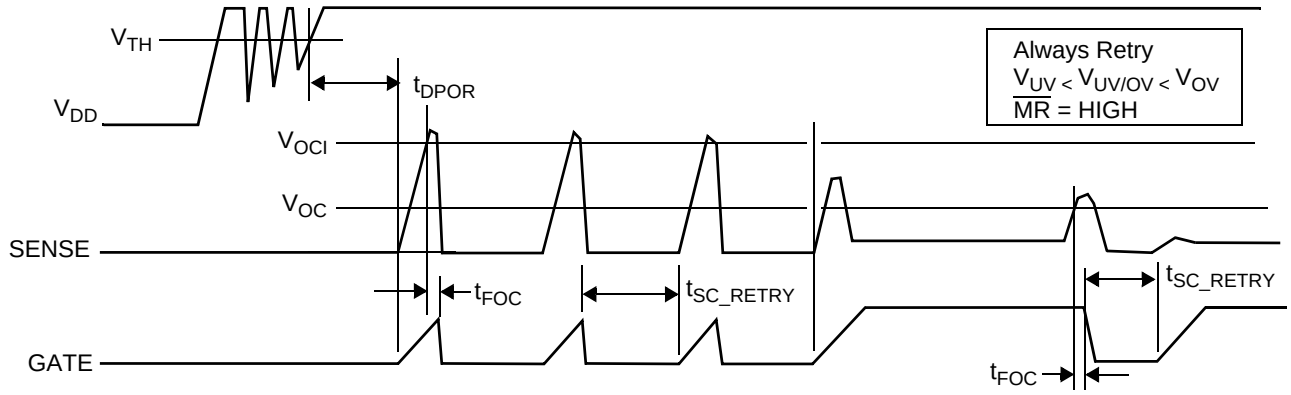
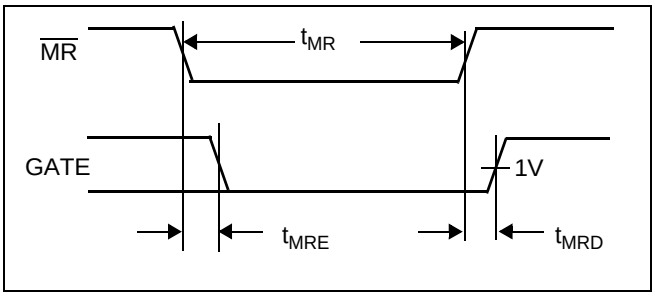
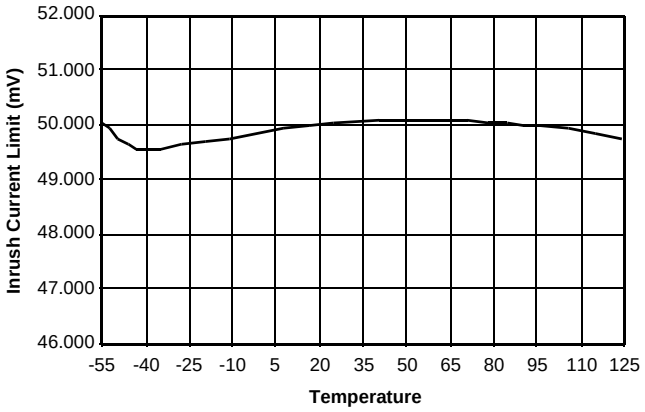


Figure 3. Manual Reset

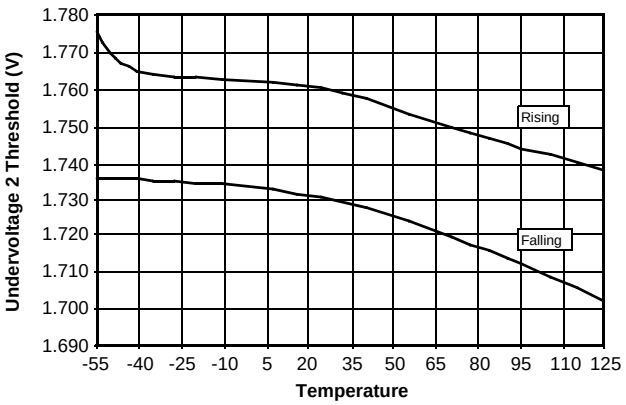


TYPICAL PERFORMANCE CHARACTERISTICS

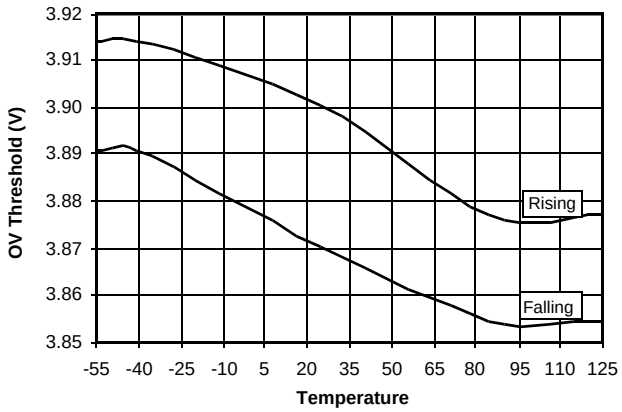
Overcurrent Threshold vs. Temperature



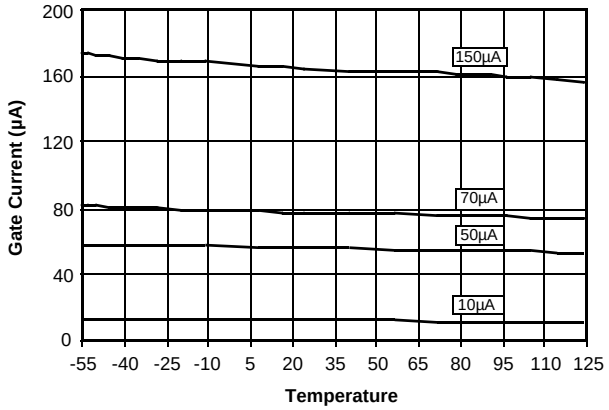
Undervoltage 2 Threshold vs. Temperature



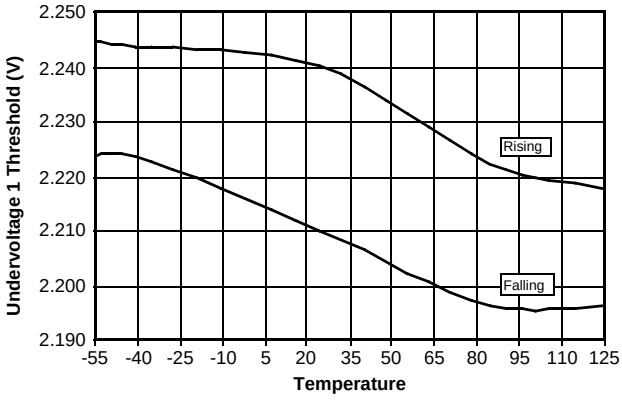
Overvoltage Threshold vs. Temperature



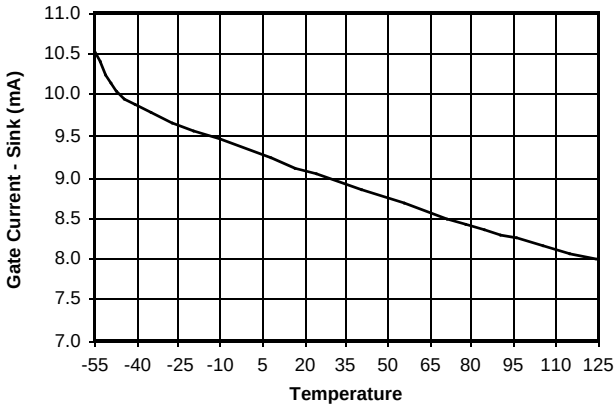
I_{GATE} (source) vs. Temperature



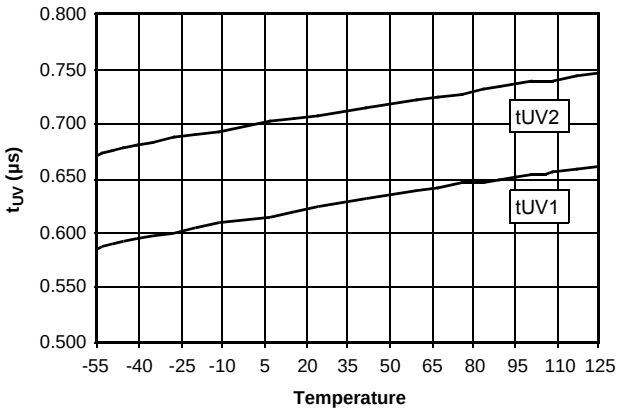
Undervoltage 1 Threshold vs. Temperature



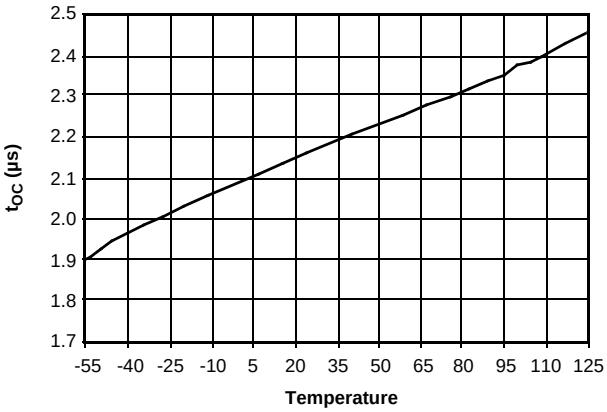
I_{GATE} (sink) vs. Temperature



t_{FUV} vs. Temperature



t_{FOC} vs. Temperature



t_{FOV} vs. Temperature

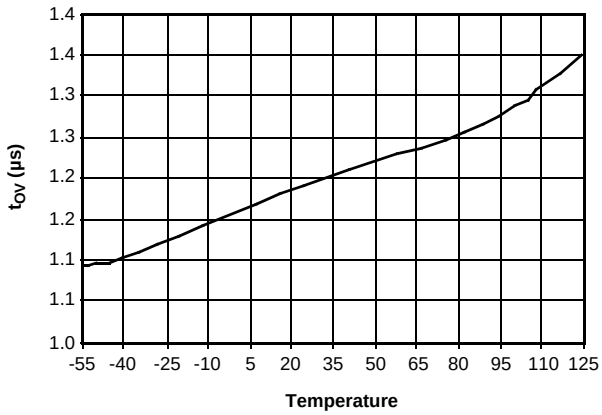
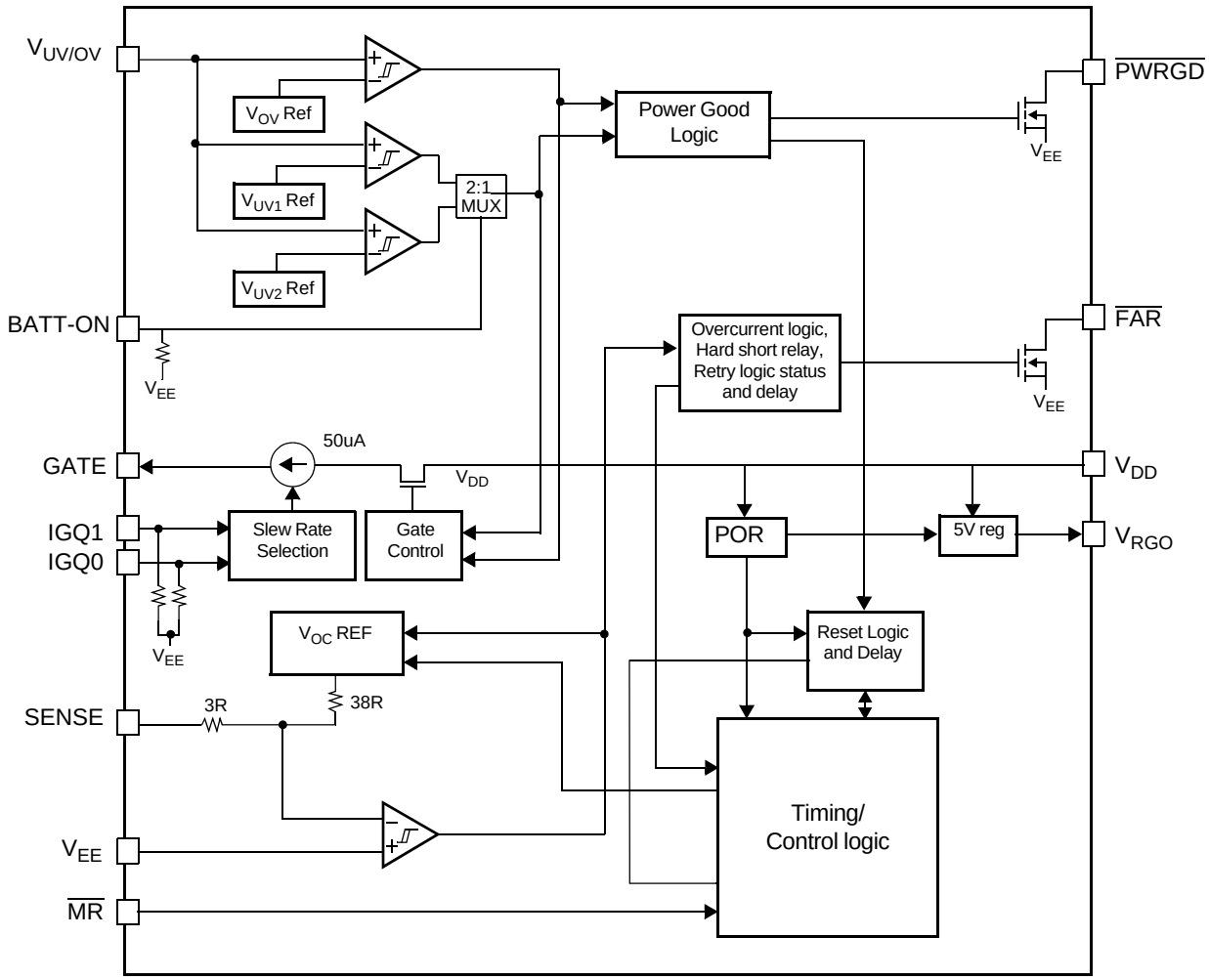
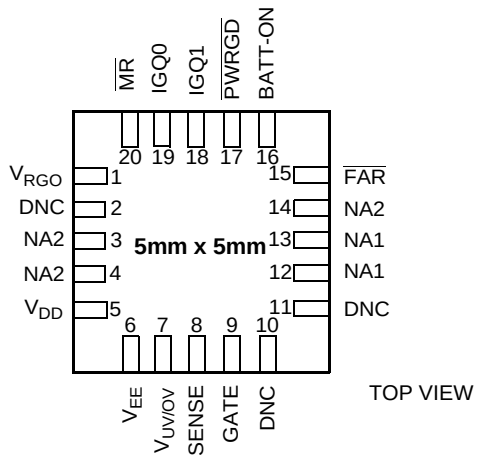


Figure 4. Block Diagram



PIN CONFIGURATION



NA1 pins connect to V_{RGO}
NA2 pins connect to V_{EE}

PIN DESCRIPTIONS

Pin	Name	Description
1	V_{RGO}	**Regulated 5V output.** Used to pull-up user programmable inputs IGQ0, IGQ1, BATT-ON and MRH (if needed).
2	DNC	**Pin not used.** Do not connect to this pin.
3	NA2	**Not Available.** Connect to V_{EE}.
4	NA2	**Not Available.** Connect to V_{EE}.
5	V_{DD}	**Positive Supply Voltage Input.**
6	V_{EE}	**Negative Supply Voltage Input.**
7	$V_{UV/OV}$	**Analog Undervoltage and Overvoltage Input.** Turns off the external N-channel MOSFET when there is an undervoltage or overvoltage condition.
8	SENSE	**Circuit Breaker Sense Input**. This input pin detects the overcurrent condition.
9	GATE	**FET Gate Drive.** This pin supplies the current to turn on the FET.
10	DNC	**Pin not used.** Do not connect to this pin.
11	DNC	**Pin not used.** Do not connect to this pin.
12	NA1	**Not Available.** Connect to V_{RGO}.
13	NA1	**Not Available.** Connect to V_{RGO}.
14	NA2	**Not Available.** Connect to V_{EE}.
15	$\overline{FAR}$	**Failure After Re-try ($\overline{FAR}$)** output signal.
16	BATT-ON	**Battery On Input**. This input signals that the battery backup (or secondary supply) is supplying power to the backplane. It has an internal pulldown resistor. (>10MΩ typical)
17	$\overline{PWRGD}$	**Power Good Output.** This output pin enables a power module.

PIN DESCRIPTIONS (Continued)

Pin	Name	Description
18	IGQ1	**Gate Current Quick Select Bit 1 Input.** This pin is used to change the gate current drive and is intended to allow for current ramp rate control of the gate pin of an external FET. It has an internal pulldown resistor. (>10MΩ typical)
19	IGQ0	**Gate Current Quick Select Bit 0 Input.** This pin is used to change the gate current drive and is intended to allow for current ramp rate control of the gate pin of an external FET. It has an internal pulldown resistor. (>10MΩ typical)
20	$\overline{MR}$	**Manual Reset.** Pulling the $\overline{MR}$ pin LOW initiates a GATE pin reset (GATE pin pulled LOW). The $\overline{MR}$ signal must be held LOW for 5µsecs (minimum).

FUNCTIONAL DESCRIPTION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or DC/DC converter can draw huge transient currents as they charge up. This transient current can cause permanent damage to the board's components and cause transients on the system power supply.

The X80070 is designed to turn on a board's supply voltage in a controlled manner (see Figure 5), allowing the board to be safely inserted or removed from a live backplane. The device also provides undervoltage, overvoltage and overcurrent protection while keeping the power module (dc-dc converter) off until the backplane input voltage is stable and within tolerance.

Figure 5. Typical Inrush with Gate Slew Rate Control

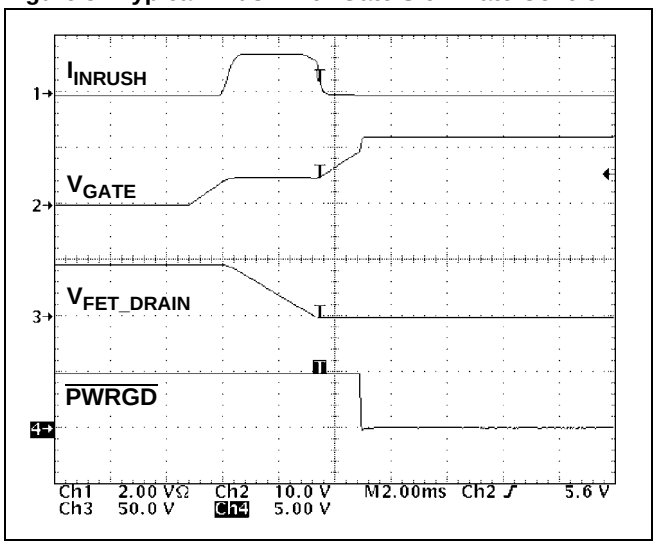
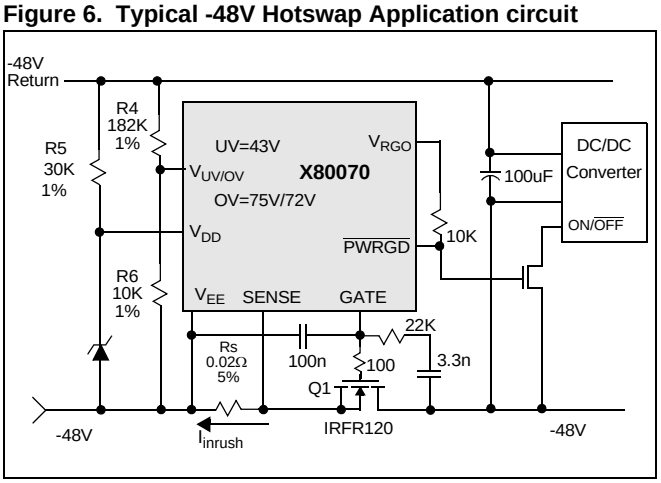


Figure 6. Typical -48V Hotswap Application circuit



Overvoltage and Undervoltage Shutdown

The X80070 provides overvoltage and undervoltage protection circuits.

When an overvoltage (V_{OV}) or undervoltage (V_{UV1} and V_{UV2}) condition is detected, the GATE pin immediately pulls low turning off the supply to the system. The undervoltage threshold V_{UV1} applies to the normal operation with a main supply. The undervoltage threshold V_{UV2} assumes the system is powered by a battery. When using a battery backup, the BATT-ON pin is pulled to V_{RGO}. The default thresholds have been set so the external resistance values in Figure 6 provide an overvoltage threshold of 74.9V (X80070 and X80072) or 68V (X80071 and X80073), a main undervoltage threshold of 43V and a battery undervoltage threshold of 33.8V.

As shown in Figure 9, this circuit block contains comparators and voltage references to monitor for a single overvoltage and dual undervoltage trip points. The overvoltage and undervoltage trip points as shown in Table 1 below.

Table 1. Overvoltage/Undervoltage default thresholds

Symbol	Description	Threshold falling	Threshold rising	Max/Min Voltage [1]	Lockout Voltage [2]
V_{OV}	Overvoltage (X80070/72)	3.87V	3.9V	74.3	74.9
V_{OV}	Overvoltage (X80071/73)	3.51V	3.54V	67.4	68
V_{UV1}	Undervoltage 1	2.21V	2.24V	43.0	42.4
V_{UV2}	Undervoltage 2	1.73V	1.76V	33.8	33.2

Notes: 1: Max/Min Voltage is the maximum and mimimum operating voltage assuming the recommended $V_{UV/OV}$ resistor divider.

2: Lockout voltage is the voltage where the X8007x turns off the FET.

A resistor divider connected between the plus and minus input voltages and the $V_{UV/OV}$ pin (see Figure 7) determines the overvoltage and undervoltage shutdown voltages and the operating voltage range. Using the thresholds in Table 1 and the equations of Figure 7 the desired operating voltage can be determined. Figure 8 shows the resistance values for various operating voltages (X80070 and X80072).

Figure 7. Overvoltage Undervoltage Divider

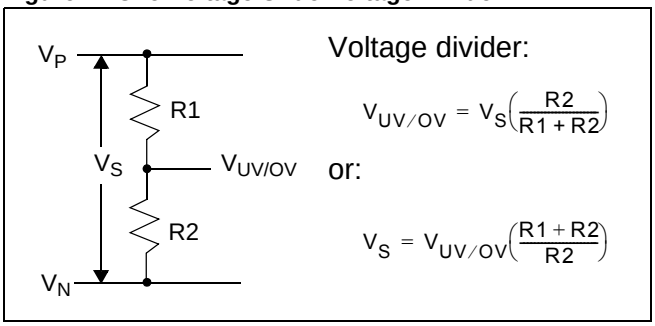
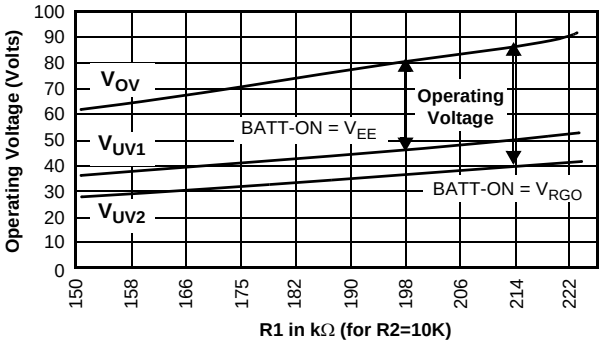


Figure 8. Operating voltage vs. resistor ratio



Battery back up operations

An external signal, BATT-ON is provided to switch the undervoltage trip point. The BATT-ON signal is a LOGIC HIGH if $V_{IHB} > V_{EE} + 4V$ and is a LOGIC LOW if $V_{ILB} < V_{EE} + 2V$. The time from a BATT-ON input change to a valid new undervoltage threshold is 100ns. See Electrical Specifications for more details.

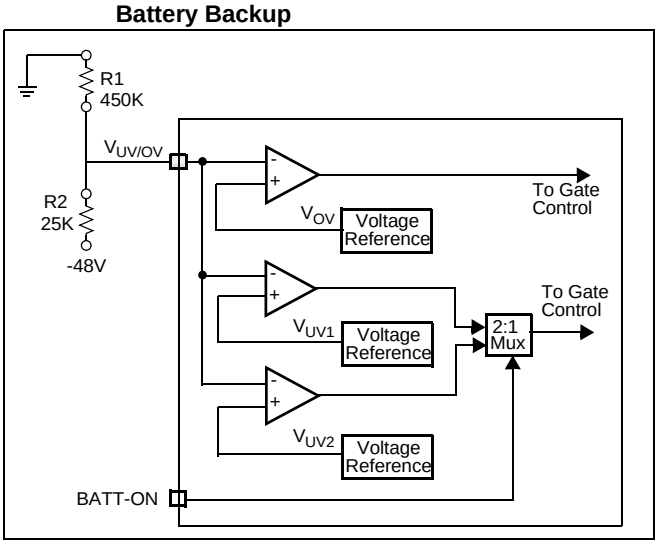
Note: The $V_{UV/OV}$ pin must be limited to less than $V_{EE} + 5.5V$. in worst case conditions. Values for R1 and R2 must be chosen such that this condition is met. Intersil recommends R1 = 182kΩ and R2 = 10kΩ to conform to factory settings. These should be 1% resistors.

Table 2. Selecting between Undervoltage Trip Points

Pin	Description	Trip Point Selection
BATT-ON	Undervoltage Trip Point Selection Pin	If BATT-ON = 0, V_{UV1} trip point is selected; If BATT-ON = 1, V_{UV2} trip point is selected.

V_{UV1} and V_{UV2} are undervoltage thresholds.

Figure 9. Overvoltage/Undervoltage for Primary and Battery Backup



Overcurrent Protection (Circuit Breaker Function)

The X80070 overcurrent circuit provides the following functions:

– Overcurrent shut-down of the power FET and external power good indicators.
– Noise filtering of the current monitor input.
– Relaxed overcurrent limits for initial board insertion.
– Overcurrent recovery retry operation.

Overcurrent shut-down

A sense resistor, placed in the supply path between V_{EE} and SENSE (see Figure 6) generates a voltage internal to the X80070. When this voltage exceeds 50mV, an overcurrent condition exists and an internal “circuit breaker” trips, turning off the gate drive to the external FET. The actual overcurrent level is dependent on the value of the current sense resistor. For example a 20mΩ sense resistor sets the overcurrent level to 2.5A.

As shown in Figure 10, this overcurrent circuit block contains a resistor ladder, a comparator, a noise filter and a voltage reference to monitor for overcurrent conditions.

The overcurrent voltage threshold (V_{OC}) is 50mV. This can be factory set, by special order, to any setting between 30mV and 100mV.

If an overcurrent condition is detected, the GATE output is shut down and the power good indicator goes inactive.

Overcurrent during insertion

Insertion is defined as the first plug-in of the board to the backplane. In this case, the X80070 is initially fully powered off prior to the hot plug connection to the main supply. This condition is different from a situation where the main supply has temporarily failed resulting in a partial recycle of the power. This second condition will be referred to as a power cycle.

During insertion, the board can experience high levels of current for short periods of time as power supply capacitors charge up on the power bus. To prevent the overcurrent sensor from turning off the FET inadvertently, the X80070 has the ability to allow more current to flow through the power FET and the sense resistor for a short period of time until the FET turns on and the $\overline{PWRGD}$ signal goes active.

In the X80070, 150mV is allowed across sense resistor during insertion (7.5A assuming a 20mW resistor). This provides a mechanism to reduce insertion issues associated with huge current surges. Insertion currents of 1X, 2X, or 4X are also available. Please contact Intersil for these factory options.

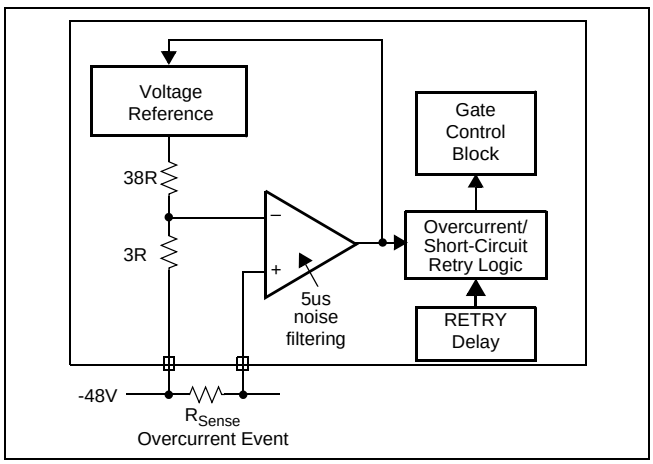
After the $\overline{PWRGD}$ signal is asserted, the X80070 switches back to the normal overcurrent setting.

Hardshort Protection - (Retry)

In the event on an overcurrent or hard short condition, the X80070 includes a retry circuit. This circuit waits for 100ms, then attempts to again turn on the FET. If the fault condition still exists, the FET turns off and the sequence repeats. For versions X80070 and X80072, this process continues indefinely until the overcurrent condition does not exist. For the X80071 and X80073, this process repeats five times only, then will keep the FET off and set the $\overline{FAR}$ pin active. After $\overline{FAR}$ is asserted, it can be cleared using the master reset pin, $\overline{MR}$, or cycling the power-on V_{DD}. When using the $\overline{MR}$ pin, the $\overline{FAR}$ output is cleared upon $\overline{MR}$ assertion.

If an overcurrent condition does not occur on any retry, the gate pin will proceed to open at the user defined slew rate.

Figure 10. Overcurrent Detection/Short Circuit Protection.



Overcurrent noise filter

The X80070 has a noise (low pass) filter built into the overcurrent comparator. The comparator will thus require the current spikes to exceed the overcurrent limit for more than 5µs.

Gate Drive Output Slew Rate (Inrush Current) Control

The gate output drives an external N-Channel FET. The GATE pin goes high when no overcurrent, undervoltage or overvoltage conditions exist.

The X80070 provides an I_{GATE} current of 50uA to provide on-chip slew rate control to minimize inrush current and provide the best turn on time for a given load, while avoiding overcurrent conditions.

Slew Rate (Gate) Control

As shown in Figure 11, this circuit block contains a current source (I_{GATE}) that drives the 50uA current into the GATE pin. This current provides a controlled slew rate for the FET.

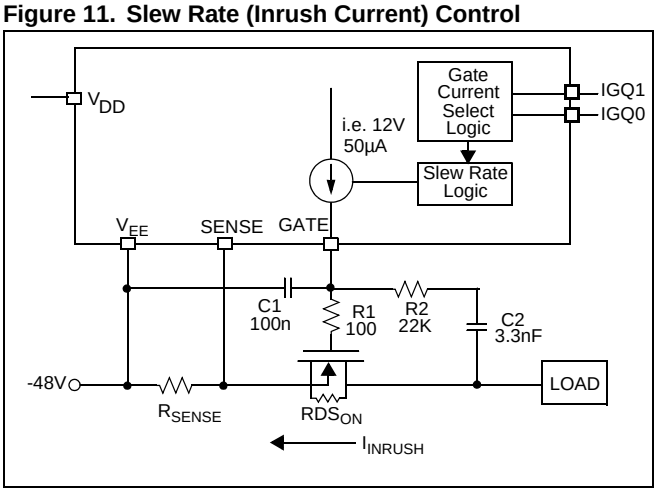
To give the designer flexibility in the design of the hot swap circuit, the X80070 provides two external pins, IGQ1 and IGQ0. These pins allow the user to switch to different GATE currents on-the-fly by selecting one of four pre-selected I_{GATE} currents. When IGQ0 and IGQ1 are left unconnected, the gate current is 50uA. The other three settings are 10uA, 70uA and 150uA, as shown in Table 3.

Table 3. IGQ Gate Current Selection

IGQ1 pin	IGQ0 pin	Operation
0	0	Defaults to gate current 50μA
0	1	Gate Current is 10μA
1	0	Gate Current is 70μA
1	1	Gate Current is 150μA

Typically, the delay from IGQ1 and IGQ0 selection to a change in the GATE pin current is less than 1 μsecond.

Figure 11. Slew Rate (Inrush Current) Control



Gate Capacitor, Filtering and Feedback

The FET control circuit includes an FET feedback capacitor C_2, which provides compensation for the FET during turn on. The capacitor value depends on the load, the choice of FET (because of the FET internal capacitances) and the FET gate current.

The value of C2 can be selected with the following formula.

$$C2 = \frac{I_{GATE} \times C_{LOAD}}{I_{INRUSH}}$$

Where:

I_{GATE} = FET Gate current

I_{INRUSH} = Maximum desired inrush current

C_{LOAD} = DC/DC bulk capacitance

With the X80070, there is some control of the gate current with the IGQ pins, so one selection of C2 can cover a wide range of possible loading conditions. Typical values for C2 range from 2.2 to 4.7nF.

When power is applied to the system, the FET tries to turn on due to its internal gate to drain capacitance (Cgd) and the feedback capacitor C2 (see Figure 11.) The X80070 device, when powered, pulls the gate output low to prevent the gate voltage from rising and keep the FET from turning on. However, unless V_{DD} powers up very quickly, there will be a brief period of time during initial application of power when the X80070 circuits cannot hold the gate low. The use of an external capacitor (C1) prevents this. Capacitors C1 and C2 form a voltage divider to prevent the gate voltage from rising above the FET turn on threshold before the X80070 can hold the gate low. Use the following formula for choosing C1.

$$C1 = \frac{V1 - V2}{V2} C2$$

Where:

V1 = Maximum input voltage,

V2 = FET threshold Voltage,

C1 = Gate capacitor,

C2 = Feedback capacitor.

In a system where V_{DD} rises very fast, a smaller value of C1 may suffice as the X80070 will control voltage at the gate before the voltage can rise to the FET turn on threshold. The circuit of Figure 11 assumes that the input voltage can rise to 80V before the X80070 sees operational voltage on V_{DD}. If C1 is used then the series resistor R1 will be required to revent high frequency oscillations.

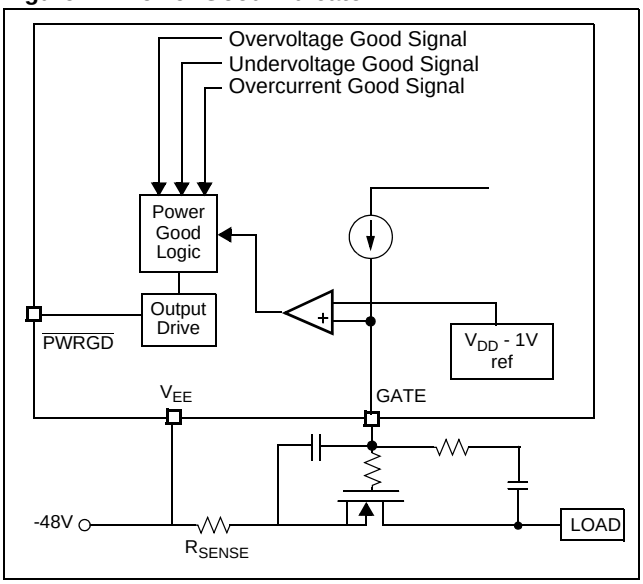
Power Good Indication

The $\overline{PWRGD}$ signal asserts (Logic LOW) only when all of the below conditions are true:

– there is no overvoltage or no undervoltage condition, (i.e. undervoltage < V_{EE} < overvoltage.)
– There is no overcurrent condition (i.e. V_{EE} - V_{SENSE} < V_{OC}.)
– The FET is turned on (i.e. V_{GATE} > V_{DD} - 1V)

As shown in Figure 12, this circuit block contains a comparator, and an internal voltage reference. These provide a circuit to determine the whether the gate drive to the FET has fully turned on as requested. If so, the power good indicator ($\overline{PWRGD}$) goes active.

Figure 12. Power Good Indicator



Manual Reset

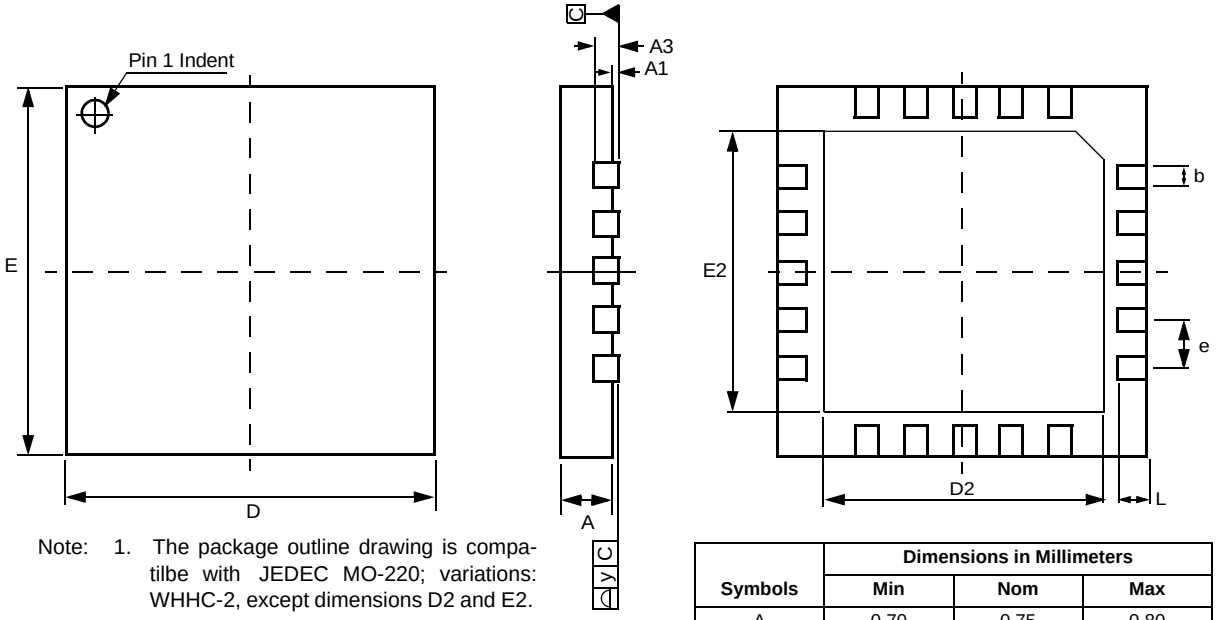
The X80070 has a manual reset pin. $\overline{MR}$ (manual reset). The $\overline{MR}$ signal is used as a manual reset for the GATE pin. This pin is used to initiate Soft Reinsert. When $\overline{MR}$ is pulled LOW the GATE pin will be pulled LOW. It also clears the $\overline{FAR}$ signal. When the $\overline{MR}$ pin goes HIGH, it removes the override signal and the gate will turn on based on the selected gate control mechanism. (See Figure 3.)

Table 4. Manual Reset (Gate Signal)

$\overline{MR}$	Gate Pin	Requirements
1	Operational	When $\overline{MR}$ is HIGH the reset function is disabled
0	OFF	$\overline{MR}$ must be held LOW minimum of 5μsecs

PACKAGING INFORMATION

20-Lead Quad Flat No Lead Package (Package Code: Q20)
5mm x 5mm Body with 0.65mm Lead Pitch



Note: 1. The package outline drawing is compatilbe with JEDEC MO-220; variations: WHHC-2, except dimensions D2 and E2.

2. The terminal #1 identifier is a laser marked feature

Symbols	Dimensions in Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
A3	0.19	0.20	0.25
D	4.90	5.00	5.10
D2	3.70	3.80	3.90
E	4.90	5.00	5.10
E2	3.70	3.80	3.90
e	—	0.65	—
L	0.35	0.40	0.45
y		—	0.08