élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2120C
100 MHz Current Feedback Amplifier

Features

- Excellent differential gain and phase on ±5V to ±15V supplies
- 100 MHz −3 dB bandwidth from gains of ±1 to ±10
- 700 V/µs slew rate
- 0.1 dB flatness to 20 MHz
- Output disable in 50 ns - remains high impedance even when driven with large slew rates
- Single +5V supply operation
- AC characteristics are lot and temperature stable
- Available in small SO-8 package

Applications

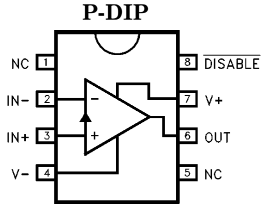
- Video gain block
- Residue amplifier
- Multiplexer
- Current to voltage converter
- Coax cable driver with gain of 2
- ADC driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2120CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2120CS	0°C to +75°C	8-Lead SO	MDP0027

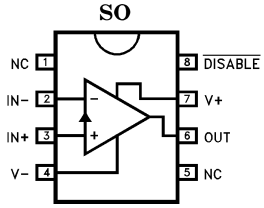
Connection Diagrams

P-DIP



2120–1

SO



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Top View

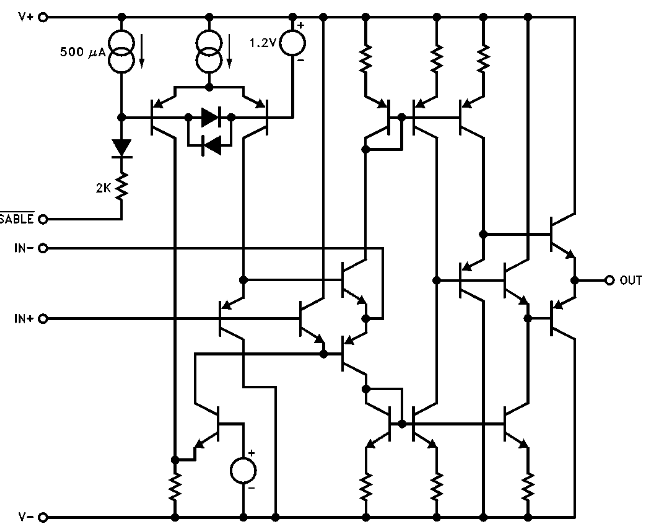
General Description

The EL2120C is a wideband current feedback amplifier optimized for video performance. Its 0.01% differential gain and 0.03 degree differential phase performance when at ±5V supplies exceeds the performance of other amplifiers running on ±15V supplies. Operating on ±8 to ±15V supplies reduces distortions to 0.01% and 0.01 degrees and below. The EL2120C can operate with supplies as low as ±2.5V or a single +5V supply.

Being a current feedback design, bandwidth is a relatively constant 100 MHz over the ±1 to ±10 gain range. The EL2120C has been optimized for flat gain over frequency and all characteristics are maintained at positive unity gain. Because the input slew rate is similar to the 700 V/µs output slew rate the part makes an excellent high-speed buffer.

The EL2120C has a superior output disable function. Time to enable or disable is 50 ns and does not change markedly with temperature. Furthermore, in disable mode the output does not draw excessive currents when driven with 1000 V/µs slew rates. The output appears as a 3 pF load when disabled.

Simplified Schematic



2120–21

January 1996 Rev E

Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation.

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Absolute Maximum Ratings ($T_A = 25°C$)

Voltage between V+ and V−	33V
Voltage at +IN, −IN, V_{OUT}	(V−) − 0.5V to (V+) + 0.5V
Voltage between +IN and − IN	±5V
Voltage at /Disable	(V+) − 10V to (V+) + 0.5V
Current into +IN, −IN, and /Disable	±5 mA
Output Current	±50 mA
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	0° to 75°C
Operating Junction Temperature P-DIP or SO	150°C
Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open Loop DC Electrical Characteristics

$V_S = \pm 5V$; $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage $V_S = \pm 15V$	Full Full		4 2	20 25	II II	mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Drift	Full		20		V	μV/°C
I_{B+}	$+V_{IN}$ Input Bias Current	Full		5	15	II	μA
I_{B-}	$-V_{IN}$ Input Bias Current	Full		10	50	II	μA
CMRR	Common-Mode Rejection (Note 1)	Full	50	55		II	dB
−ICMR	−Input Current Common-Mode Rejection (Note 1)	Full		8	20	II	μA/V
PSRR	Power Supply Rejection (Note 2)	Full	65	80		II	dB
+IPSR	+Input Current Power Supply Rejection (Note 2)	25°C		0.03		V	μA/V
−IPSR	−Input Current Power Supply Rejection (Note 2)	Full		0.6	5	II	μA/V
R_{OL}	Transimpedance	Full	70	140		II	kΩ
A_{VOL}	Voltage Gain	Full	58	66		II	dB
$+R_{IN}$	$+V_{IN}$ Input Impedance	25°C		2		V	MΩ

TD is 3.2in

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 5V$; $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{IN}	$+V_{IN}$ Range	Full	±3.0	±3.5		II	V
V_O	Output Voltage Swing	Full	±3.0	±3.5		II	V
I_{SC}	Output Short-Circuit Current	25°C		100		II	mA
$I_{O,DIS}$	Output Current, Disabled	Full		5	50	II	μA
$V_{DIS,ON}$	Disable Pin Voltage for Output Enabled	Full	(V+) − 1			II	V
$V_{DIS,OFF}$	Disable Pin Voltage for Output Disabled	Full			(V+) − 4	II	V
$I_{DIS,ON}$	Disable Pin Current for Output Enabled	Full			5	II	μA
$I_{DIS,OFF}$	Disable Pin Current for Output Disabled	Full	1.0			II	mA
I_S	Supply Current ($V_S = \pm 15V$)	Full		17	20	II	mA

Note 1: The input is moved from −3V to +3V.
Note 2: The supplies are moved from ±5V to ±15V.

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$; $A_V = +2$ ($R_F = R_G = 270\Omega$); $R_L = 150\Omega$; $C_L = 7$ pF; $C_{IN-} = 2$ pF; $T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
SR	Slew Rate; V_{OUT} from −3V to +3V Measured at −2V and +2V $V_S = \pm 15V$ $V_S = \pm 5V$		 750 550		 V V	 V/μs V/μs
t_S	Settling Time to 0.25% of a 0 to +10V Swing; $A_V = +1$ with $R_F = 270\Omega$, $R_G = \infty$, and $R_L = 400\Omega$		50		V	ns
BW	Bandwidth −3 dB ±1 dB ±0.1 dB		95 50 16		V V V	MHz MHz MHz
BW@2.5V	Bandwidth at $V_S = \pm 2.5V$ −3 dB ±1 dB ±0.1 dB		75 35 11		V V V	MHz MHz MHz
Peaking			0.5		V	dB

TD is 2.7in

TD is 2.4in

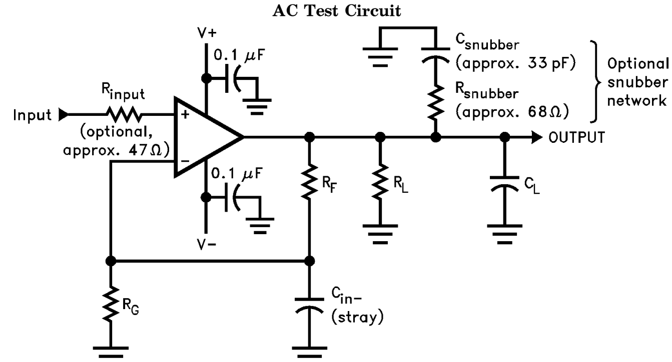
Closed Loop AC Electrical Characteristics — Contd.

$V_S = \pm 15V$; $A_V = +2$ ($R_F = R_G = 270\Omega$); $R_L = 150\Omega$; $C_L = 7$ pF; $C_{IN-} = 2$ pF; $T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
dG	Differential Gain; DC Offset from −0.7V through +0.7V, AC Amplitude 286 mVp−p					
	$V_S = \pm 15V$, f = 3.58 MHz		<0.01		V	%
	$V_S = \pm 15V$, f = 30 MHz		0.1		V	%
	$V_S = \pm 5V$, f = 3.58 MHz		0.01		V	%
dθ	Differential Phase; DC Offset from −0.7V through +0.7V, AC Amplitude 286 mVp−p					
	$V_S = \pm 15V$, f = 3.58 MHz		0.01		V	°
	$V_S = \pm 15V$, f = 30 MHz		0.1		V	°
	$V_S = \pm 5V$, f = 3.58 MHz		0.06		V	°

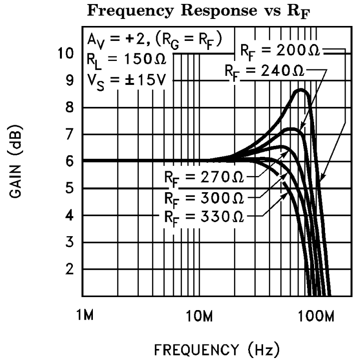
Typical Performance Curves

AC Test Circuit



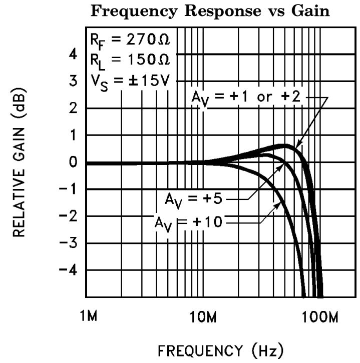
2120-3

Frequency Response vs R_F



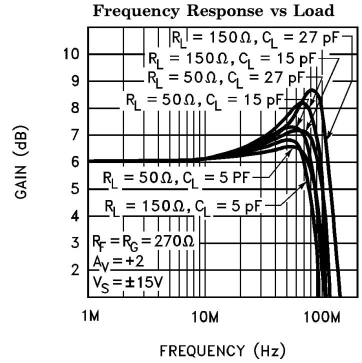
2120-4

Frequency Response vs Gain



2120-5

Frequency Response vs Load

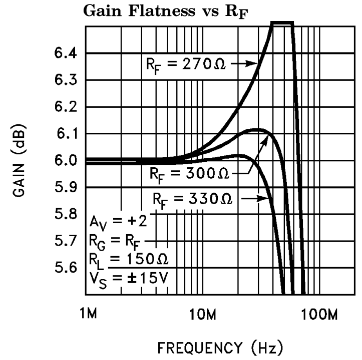


2120-6

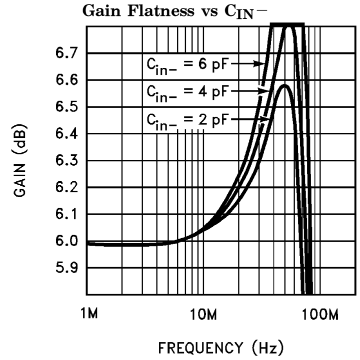
TD is 2.0in

Typical Performance Curves — Contd.

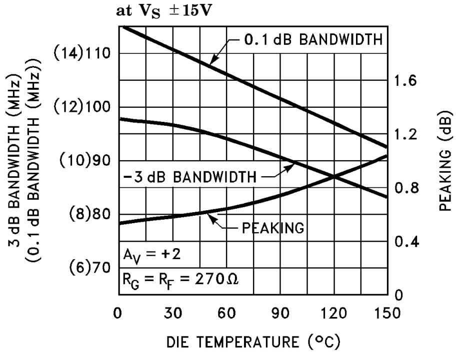
Gain Flatness vs R_F



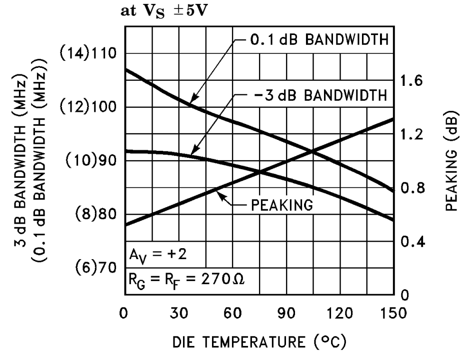
Gain Flatness vs $C_{IN}-$



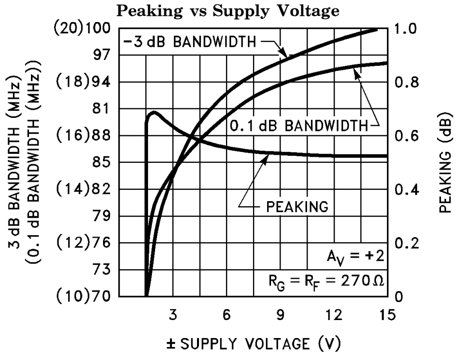
−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at V_S ±15V



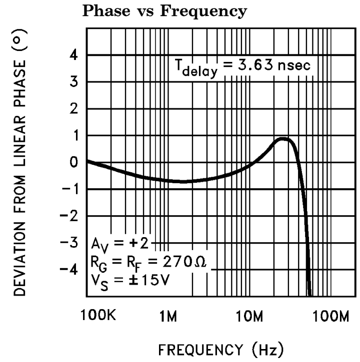
−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at V_S ±5V



−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Supply Voltage



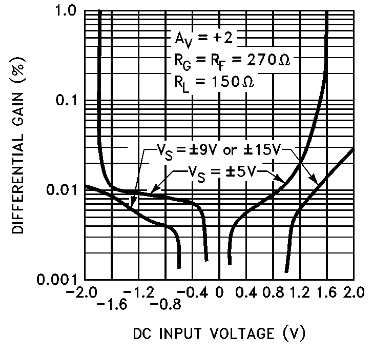
Deviation From Linear Phase vs Frequency



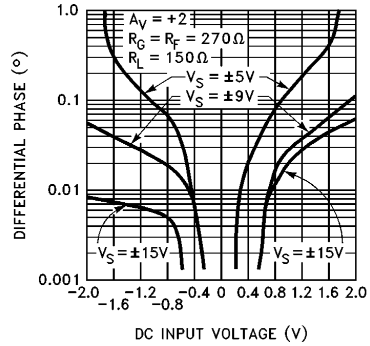
2120–7

Typical Performance Curves — Contd.

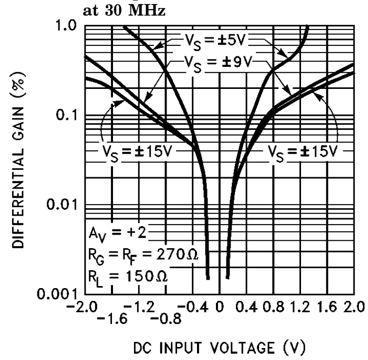
Differential Gain vs DC Input Offset at 3.58 MHz



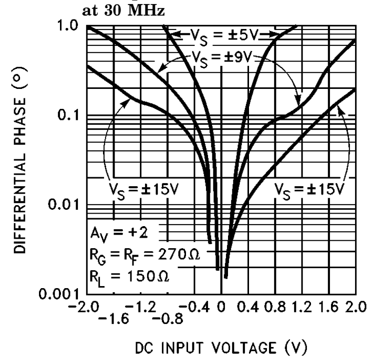
Differential Phase vs DC Input Offset at 3.58 MHz



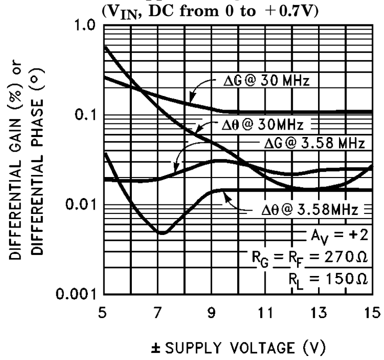
Differential Gain vs DC Input Offset at 30 MHz



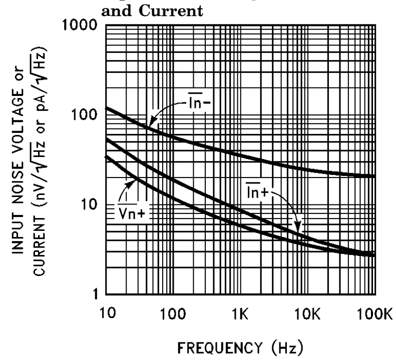
Differential Phase vs DC Input Offset at 30 MHz



Differential Gain and Phase vs Supply Voltage (V_{IN}, DC from 0 to +0.7V)



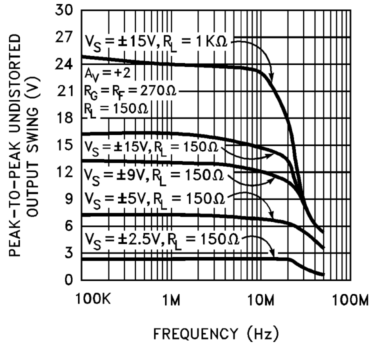
Input Noise Voltage and Current



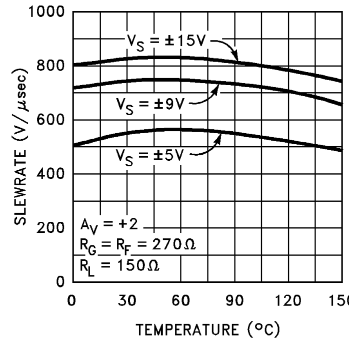
2120–8

Typical Performance Curves — Contd.

Undistorted Output Swing vs Frequency

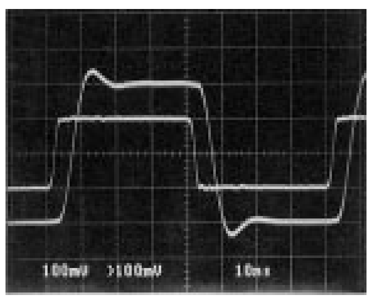


Slew Rate vs Temperature



2120-9

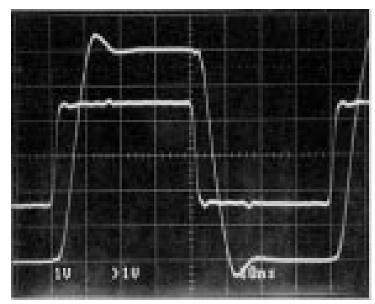
Small-Signal Transient Response



A_V = +2, R_F = R_G = 270Ω,
R_L = 150Ω

2120-10

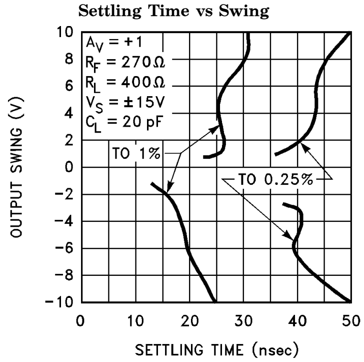
Large-Signal Transient Response



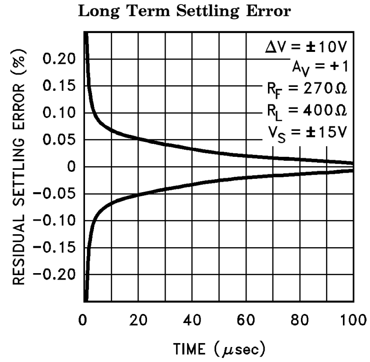
A_V = +2, R_F = R_G = 270Ω,
R_L = 150Ω, V_S = ±15V

2120-11

Settling Time vs Swing



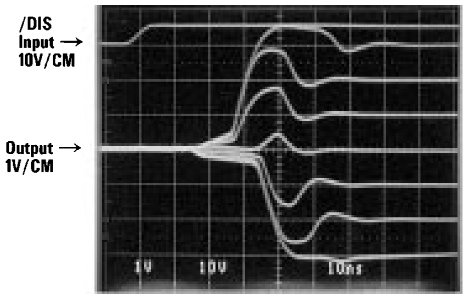
Long Term Settling Error



2120-12

Typical Performance Curves — Contd.

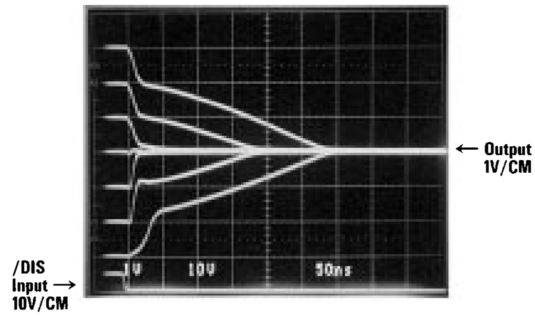
Enable Response for a Family of Inputs



$A_V = +2$, $R_L = 150\Omega$,
$V_S = \pm 5V$

2120–13

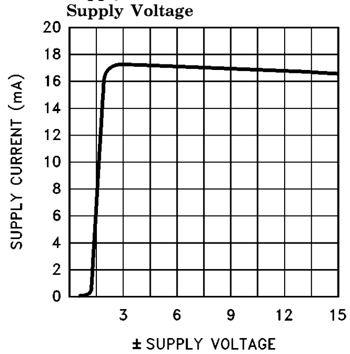
Disable Response for a Family of Inputs



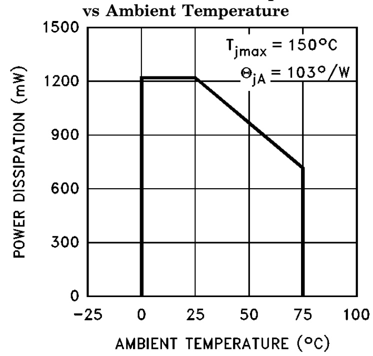
$A_V = +2$, $R_L = 150\Omega$,
$V_S = \pm 5V$

2120–14

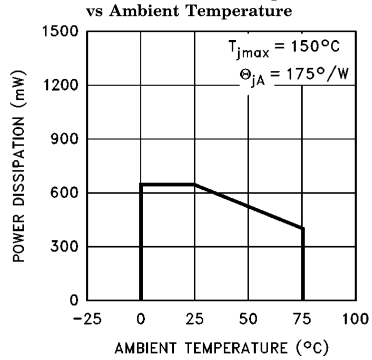
Supply Current vs Supply Voltage



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2120–15

Applications Information

The EL2120C represents the third generation of current-feedback amplifier design. It is designed to provide good high-frequency performance over wide supply voltage, load impedance, gain, temperature, and manufacturing lot variations. It is a well-behaved amplifier in spite of its 100 MHz bandwidth, but a few precautions should be taken to obtain maximum performance.

The power supply pins must be well bypassed. 0.01 μF ceramic capacitors are adequate, but lead length should be kept below ¼″ and a ground plane is recommended. Bypassing with 4.7 μF tantalum capacitors can improve settling characteristics, and smaller capacitors in parallel will not be needed. The lead length of sockets generally deteriorates the amplifier's frequency response by exaggerating peaking and increasing ringing in response to transients. Short sockets cause little degradation.

Load capacitance also increases ringing and peaking. Capacitance greater than 35 pF should be isolated with a series resistor. Capacitance at the V_{IN-} terminal has a similar effect, and should be kept below 5 pF. Often, the inductance of the leads of a load capacitance will be self-resonant at frequencies from 40 MHz to 200 MHz and can cause oscillations. A resonant load can be de-Q'ed with a small series or parallel resistor. A "snubber" can sometimes be used to reduce resonances. This is a resistor and capacitor in series connected from output to ground. Values of 68Ω and 33 pF are typical. Increasing the feedback resistor can also improve frequency flatness.

The V_{IN+} pin can oscillate in the 200 MHz to 500 MHz realm if presented with a resonant or inductive source impedance. A series 27Ω to 68Ω resistor right on the V_{IN+} pin will suppress such oscillations without affecting frequency response.

−3 dB bandwidth is inversely proportional to the value of feedback resistor R_F. The EL2120C will tolerate values as low as 180Ω for a maximum bandwidth of about 140 MHz, but peaking will increase and tolerance to stray capacitance will reduce. At gains greater than 5, −3 dB bandwidth begins to reduce, and a smaller R_F can be used to maximize frequency response.

The greatest frequency response flatness (to 0.1 dB, for instance) occurs with R_F = 300Ω to 330Ω. Even the moderate peaking caused by lower values of R_F will cause the gain to peak out of the 0.1 dB window, and higher values of R_F will cause an overcompensated response where the gain falls below the 0.1 dB level. Parasitic capacitances will generally degrade the frequency flatness.

The EL2120C should not output a continuous current above 50 mA, as stated in the ABSOLUTE MAXIMUM RATINGS table. The output current limit is set to 120 mA at a die temperature of 25°C and reduces to 85 mA at a die temperature of 150°C. This large current is needed to slew load capacitance and drive low impedance loads with low distortion but cannot be supported continuously. Furthermore, package dissipation capabilities cannot be met under short-circuit conditions. Current limit should not occur longer than a few seconds.

The output disable function of the EL2120C is optimized for video performance. While in disable mode, the feedthrough of the circuit can be modeled as a 0.2 pF capacitor from V_{IN+} to the output. No more than ±5V can be placed between V_{IN+} and V_{IN-} in disable mode, but this is compatible with common video signal levels. In disabled state the output can withstand about 1000 V/μs slew rate signals impressed on it without the output transistors turning on.

The /Disable pin logic level is referred to V+. With ±5V supplies, a CMOS or TTL driver with pull-up resistor will suffice. ±15V supplies require a +14/+11V drive span, or +15/+10V nominally. Open-collector TTL with a tapped pull-up resistor can provide these spans. The impedance of the divider should be 1k or less for optimum enable/disable speed.

The EL2120C enables in 50 ns or less. When V_{IN} = 0, only a small switching glitch occurs at the output. When V_{IN} is some other value, the output overshoots by about 0.7V when settling toward its new enabled value.

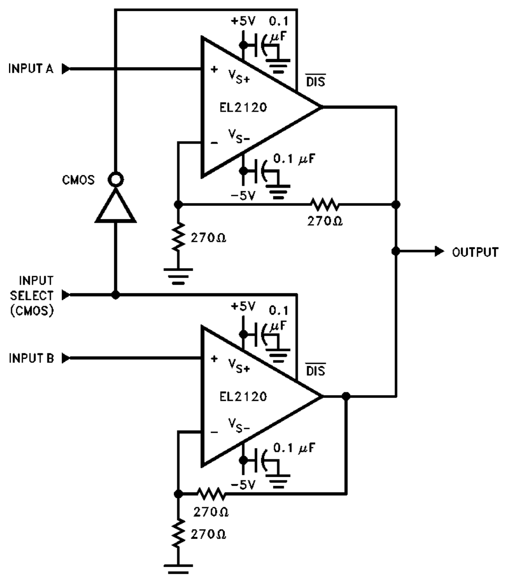
Applications Information — Contd.

When the EL2120C disables, it turns off very rapidly for inputs of ±1V or less, and the output sags more slowly for inputs larger than this. For inputs as large as ±2.5V the output current can be absorbed by another EL2120C simultaneously enabled. Under these conditions, switching will be properly completed in 50 ns or less.

The greater thermal resistance of the SO-8 package requires that the EL2120C be operated from ±10V supplies or less to maintain the 150°C maximum die temperature over the commercial temperature range. The P-DIP package allows the full ±16.5V supply operation.

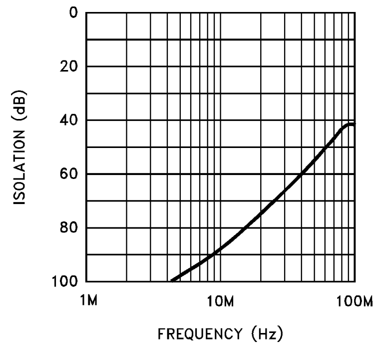
Typical Applications Circuit—A High Quality Two-Input Multiplexer

Dual EL2120C Multiplexer



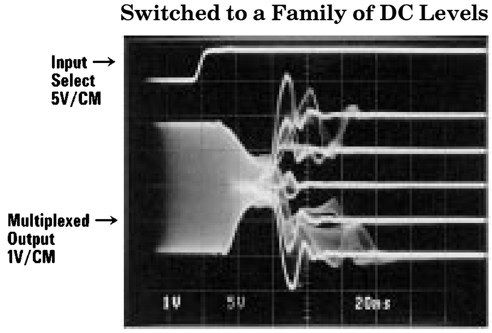
2120-16

Channel-to-Channel Isolation of Dual EL2120C Multiplexer



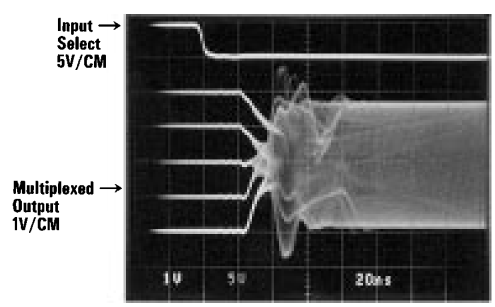
2120-17

Dual EL2120C Multiplexer Switching Channels: Uncorrelated Sinewave Switched to a Family of DC Levels



2120-18

Dual EL2120C Multiplexer Switching Channels: a Family of DC Levels Switched to an Uncorrelated Sinewave



2120-19

The EL2120C Macromodel

This macromodel has been developed to assist the user in simulating the EL2120C with surrounding circuitry. It was developed for the PSPICE simulator (copywritten by the Microsim corporation), and may need to be rearranged for other simulators, particularly the H operator. It approximates frequency response and small-signal transients as well, although the effects of load capacitance does not show. This model is slightly more complicated than the models used for low-frequency op-amps, but is much more accurate for AC.

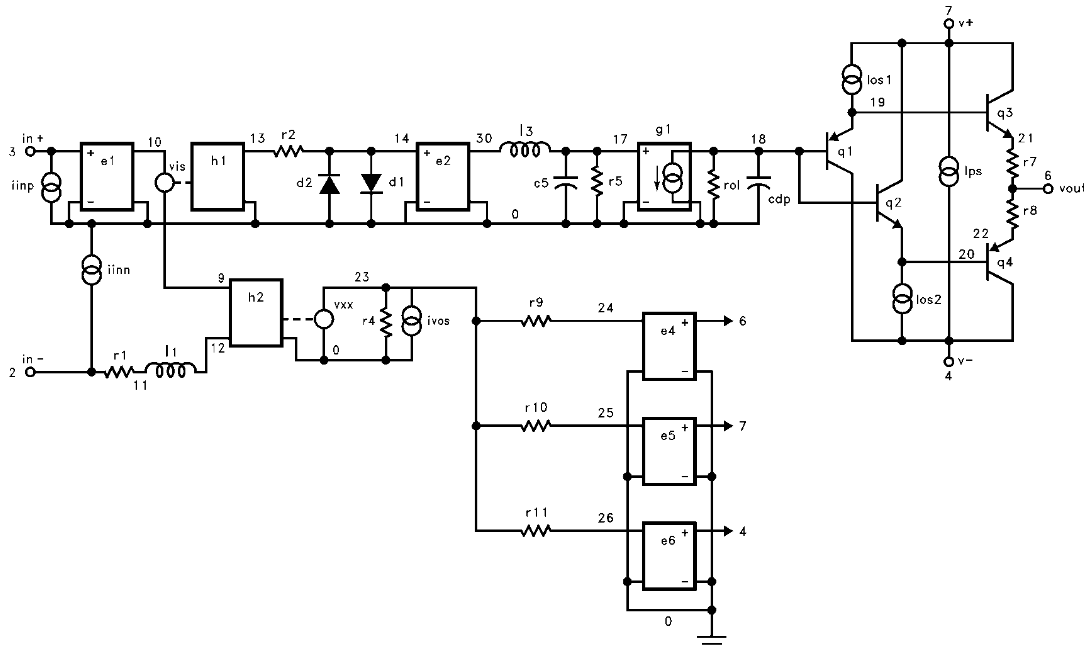
The model does not simulate these characteristics accurately:

noise	non-linearities
slew rate limitations	temperature effects
settling time	manufacturing variations
input or output resonances	CMRR and PSRR

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:     +input
*                  |      -input
*                  |      |      +Vsupply
*                  |      |      |      -Vsupply
*                  |      |      |      |      output
*                  |      |      |      |      |
.subckt M2120      3      2      7      4      6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 25
l1 11 12 20nH
iinp 3 0 10µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
s2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
15 30 17 1µH
c5 17 0 0.5pF
r5 17 0 600
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 140K
cdp 18 0 7.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply
*
ips 7 4 10mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 10K
r11 26 23 10K
*
* Models
*
.model qn npn (is=5e-15 bf=500 tf=0.1nS)
.model qp pnp (is=5e-15 bf=500 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.02 bv=4 n =4)
.ends
```


T
TAB WIDE
TD is 3.8in

The EL2120C Macromodel — Contd.



2120-20

EL2120 Macromodel

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