HOLT INTEGRATED CIRCUITS INC.

April 2007

HI-8570, HI-8571

ARINC 429
+/- 5V Supply Line Driver

DESCRIPTION

The HI-8570 and HI-8571 are CMOS integrated circuits designed to directly drive the ARINC 429 bus in an 8-pin package. Two logic inputs control a differential voltage between the output pins producing a +10 volt One, a -10 volt Zero, and a 0 volt Null.

A logic input is provided to control the slope of the differential output signal. Timing is set by an on-chip resistor and capacitor and tested to be within ARINC requirements.

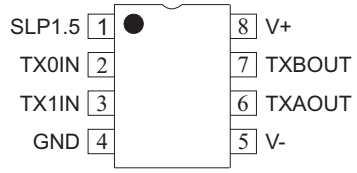
The HI-8570 has 37.5 ohms in series with each line driver output. The HI-8571 provides the option to bypass part of the output resistance so external resistance may be added for lightning protection circuits.

The HI-8570 or the HI-8571 along with the HI-8588 line receiver offer the smallest options available to get on and off the ARINC 429 bus.

FEATURES

- Direct ARINC 429 line driver interface in a small package
- On-chip line driver slope control and selection by logic input
- Low current 5 volt supplies
- CMOS / TTL logic pins
- Plastic and ceramic package options - surface mount and DIP
- Thermally enhanced SOIC packages
- Mil processing available

PIN CONFIGURATION



SUPPLY VOLTAGES

V+ = +5V
V- = -5V

FUNCTION TABLE

TX1IN	TX0IN	SLP1.5	TXAOUT	TXBOUT	SLOPE
0	0	X	0V	0V	N/A
0	1	0	-5V	5V	10μs
0	1	1	-5V	5V	1.5μs
1	0	0	5V	-5V	10μs
1	0	1	5V	-5V	1.5μs
1	1	X	0V	0V	N/A

PIN DESCRIPTION TABLE

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	SLP 1.5	LOGIC INPUT	CMOS OR TTL, V+ IS OK
2	TX0IN	LOGIC INPUT	CMOS OR TTL
3	TX1IN	LOGIC INPUT	CMOS OR TTL
4	GND	POWER	GROUND
5	V-	POWER	-5 VOLTS
6	TXAOUT	OUTPUT	LINE DRIVER TERMINAL A
7	TXBOUT	OUTPUT	LINE DRIVER TERMINAL B
8	V+	POWER	+5 VOLTS

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the line driver. The +5V and -5V levels are generated from the supply voltages. Currents for slope control are set by zener voltages across on-chip resistors.

The TX0IN and TX1IN inputs receive logic signals from a control transmitter chip such as the HI-6010, HI-3282, HI-8282A, HI-8584 or HI-8783. TXAOUT and TXBOUT hold each side of the ARINC bus at Ground until one of the inputs becomes a One. If for example TX1IN goes high, a charging path is enabled to 5V on an “A” side internal capacitor while the “B” side is enabled to -5V. The charging current is selected by the SLP1.5 pin. If the SLP1.5 pin is high, the capacitor is nominally charged from 10% to 90% in 1.5µs. If SLP1.5 is low, the rise and fall times are 10µs.

A unity gain buffer receives the internally generated slopes and differentially drives the ARINC line. Current is limited by the series output resistors at each pin. There are no fuses at the outputs of the HI-8570 as exists on the HI-8382.

The HI-8570 has 37.5 ohms in series with each output and the HI-8571 has 27.5 ohms in series with each output. The HI-8571 is for applications where external series resistance is required, typically for lightning protection devices.

Both the HI-8570 and HI-8571 are built using high-speed CMOS technology. Care should be taken to ensure the V+ and V- supplies are locally decoupled and that the input waveforms are free from negative voltage spikes which may upset the chip’s internal slope control circuitry.

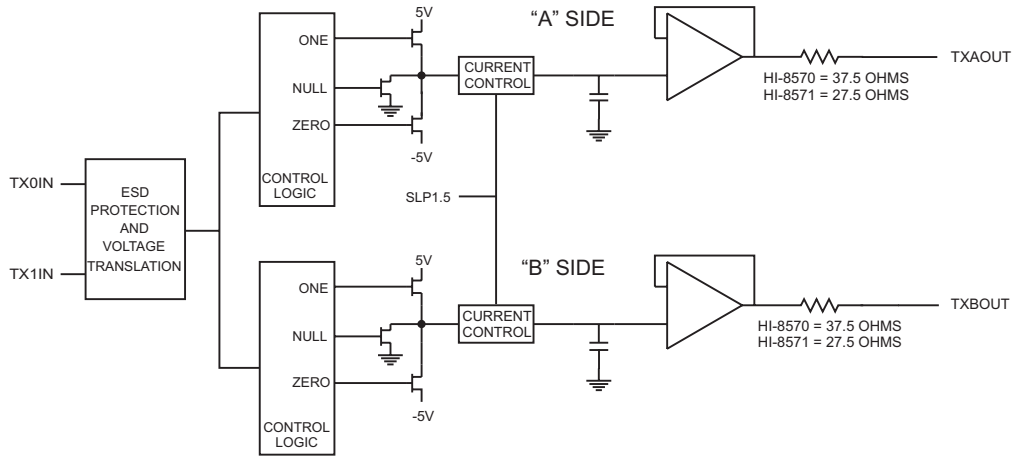


FIGURE 1 - LINE DRIVER BLOCK DIAGRAM

APPLICATION INFORMATION

Figure 2 shows a possible application of the HI-8570/8571 interfacing an ARINC transmit channel from the HI-6010.

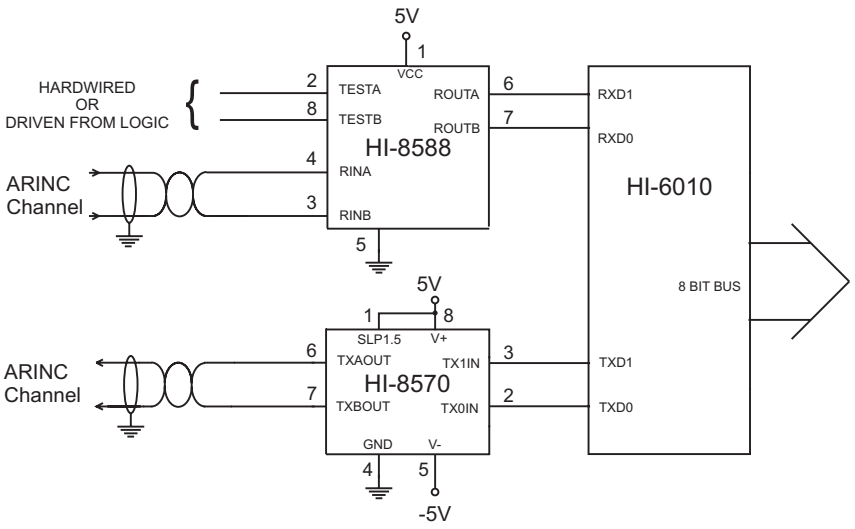


FIGURE 2 - APPLICATION DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Voltages referenced to Ground

Supply voltages
V+.....+7V
V-.....-7V

DC current per input pin..... +10mA

Power dissipation at 25°C
plastic DIL.....1.0W, derate 10mW/°C
ceramic DIL.....0.5W, derate 7mW/°C

Solder Temperature .....275°C for 10 sec

Storage Temperature.....-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltages
V+.....+4.8V to +5.3V
V-..... -5.3V to -4.8V

Temperature Range
Industrial Screening.....-40°C to +85°C
Hi-Temp Screening.....-55°C to +125°C
Military Screening.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

V+ = +5V, V- = -5V, T_A = Operating Temperature Range (unless otherwise stated)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage (TX1IN, TX0IN, SLP1.5)						
high	V_{IH}		2.1	-	V+	volts
low	V_{IL}		-	-	0.5	volts
Input current (TX1IN, TX0IN, SLP1.5)						
source	I_{IH}	V_{IN} = 0V	-	-	0.1	μA
sink	I_{IL}	V_{IN} = 5V	-	-	0.1	μA
ARINC output voltage (Differential)						
one	V_{DIFF1}	no load; TXAOUT - TXBOUT	9.00	10.00	11.00	volts
zero	V_{DIFF0}	no load; TXAOUT - TXBOUT	-11.00	-10.00	-9.00	volts
null	V_{DIFFN}	no load; TXAOUT - TXBOUT	-0.50	0	0.50	volts
ARINC output voltage (Ref. to GND)						
one or zero	V_{DOUT}	no load & magnitude at pin	4.50	5.00	5.50	volts
null	V_{NOUT}	no load	-0.25	0	0.25	volts
Operating supply current		SLP1.5 = V+				
V+	I_{DD}	TX1IN & TX0IN = 0V: no load	-	6.0	10.0	mA
V-	I_{EE}	TX0IN & TX1IN = 0V: no load	-10.0	-6.0	-	mA
ARINC output impedence	Z_{OUT}					
HI-8570			-	37.5	-	ohms
HI-8571			-	27.5	-	ohms

AC ELECTRICAL CHARACTERISTICS

V+ = 5.0V, V- = -5V, T_A = Operating Temperature Range (unless otherwise stated)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Driver propagation delay		defined in Figure 3, no load				
Output high to low	t_{phlx}		-	500	-	ns
Output low to high	t_{plhx}		-	500	-	ns
Line Driver transition times						
High Speed		SLP 1.5 = V+				
Output high to low	t_{fx}	pin 1 = logic 1	1.0	1.5	2.0	µs
Output low to high	t_{rx}	pin 1 = logic 1	1.0	1.5	2.0	µs
Low Speed		SLP 1.5 = GND				
Output high to low	t_{fx}	pin 1 = logic 0	5.0	10.0	15.0	µs
Output low to high	t_{rx}	pin 1 = logic 0	5.0	10.0	15.0	µs
Input capacitance (1)						
logic	C_{IN}		-	-	10	pF

Notes:
1. Guaranteed but not tested

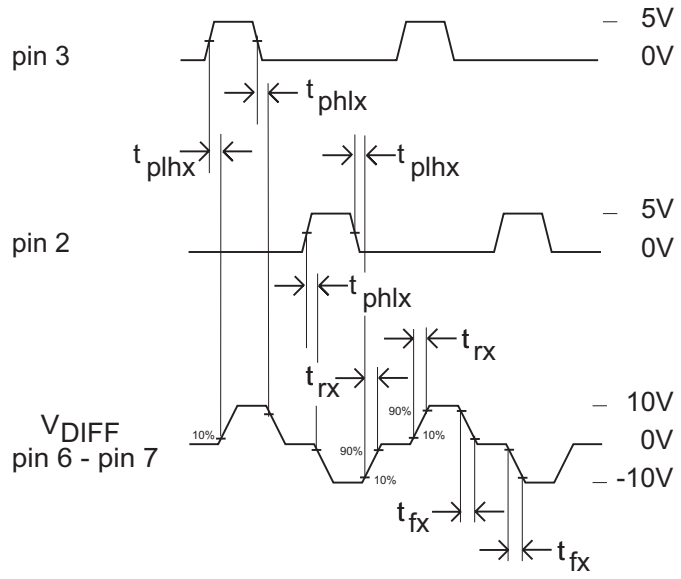


FIGURE 3 - LINE DRIVER TIMING

PACKAGE THERMAL CHARACTERISTICS

Maximum ARINC Load

PACKAGE STYLE[1]	ARINC 429 DATA RATE	SUPPLY CURRENT (mA)[2]			JUNCTION TEMP, Tj °C		
		Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
8 Lead Plastic ESOIC[5]	Low Speed[3]	20.98	20.96	20.96	38.24	98.34	138.92
	High Speed[4]	26.40	26.16	25.96	44.78	104.66	144.59

TXAOUT and TXBOUT Shorted to Ground [6,7,8]

PACKAGE STYLE[1]	ARINC 429 DATA RATE	SUPPLY CURRENT (mA)[2]			JUNCTION TEMP, Tj °C		
		Ta = 25°C	Ta = 85°C	Ta = 125°C	Ta = 25°C	Ta = 85°C	Ta = 125°C
8 Lead Plastic ESOIC[5]	Low Speed[3]	30.26	29.22	28.46	53.75	112.76	152.04
	High Speed[4]	30.44	29.42	28.68	53.92	112.95	152.25

Notes:

1. All data taken in still air.
2. At 100% duty cycle, 5V power supplies.
3. Low Speed: Data Rate = 12.5 Kbps, Load: R = 400 Ohms, C = 30 nF.
4. High Speed: Data Rate = 100 Kbps, Load: R = 400 Ohms, C = 10 nF. Data not presented for C = 30 nF as this is considered unrealistic for high speed operation.
5. 8 Lead Plastic ESOIC (Thermally enhanced SOIC with built in heat sink). Heat sink not soldered.
6. Similar results would be obtained with TXAOUT shorted to TXBOUT.
7. For applications requiring survival with continuous short circuit, operation above Tj = 175°C is not recommended.
8. Data will vary depending on air flow and the method of heat sinking employed.

HEAT SINK - ESOIC PACKAGES

An 8-pin thermally enhanced SOIC package is used for the HI-8570/HI-8571 products. The ESOIC package includes a metal heat sink located on the bottom surface of the device. This heat sink should be soldered down to the printed circuit board for optimum thermal dissipation. The heat sink is electrically isolated from the chip and can be soldered to any ground or power plane. However, since the chip's substrate is at V+, connecting the heat sink to this power plane is recommended to avoid coupling noise into the circuit.

ORDERING INFORMATION

HI - 857x xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No
M	-55°C TO +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PD	8 PIN PLASTIC DIP (8P)
PS	8 PIN PLASTIC NARROW BODY ESOIC (8HNE)
CR	8 PIN CERDIP (8D) not available Pb-free

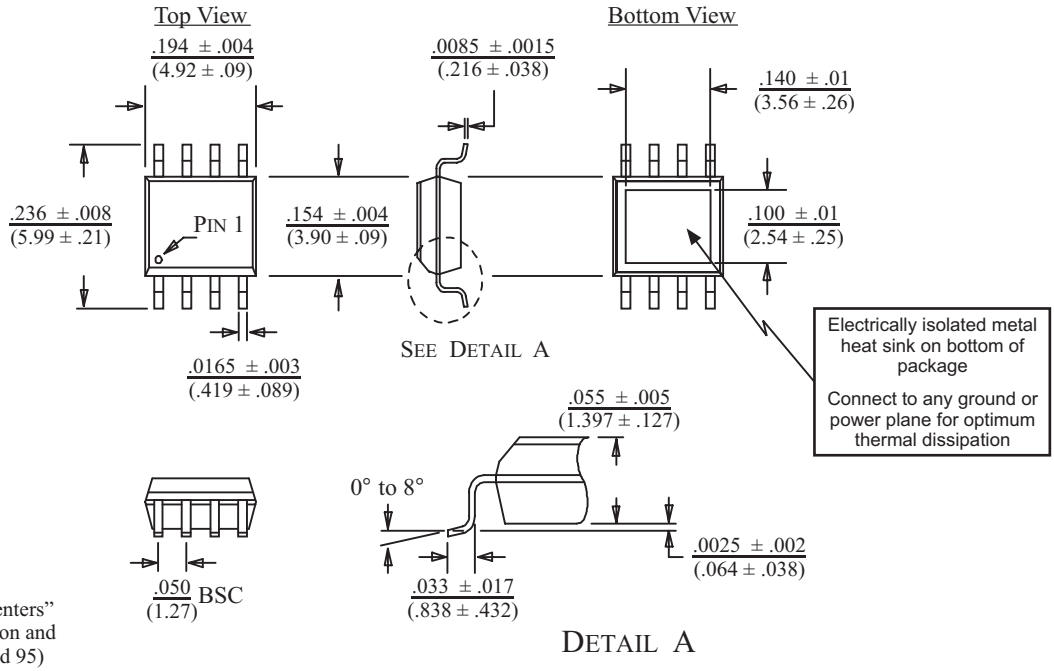
PART NUMBER	OUTPUT SERIES RESISTANCE	
	BUILT-IN	REQUIRED EXTERNALLY
8570	37.5 Ohms	0
8571	27.5 Ohms	10 Ohms

Legend: ESOIC - Thermally Enhanced Small Outline Package (SOIC) with built-in heat sink

8-PIN PLASTIC SMALL OUTLINE (ESOIC) - NB
(Narrow Body, Thermally Enhanced)

inches (millimeters)

Package Type: 8HNE

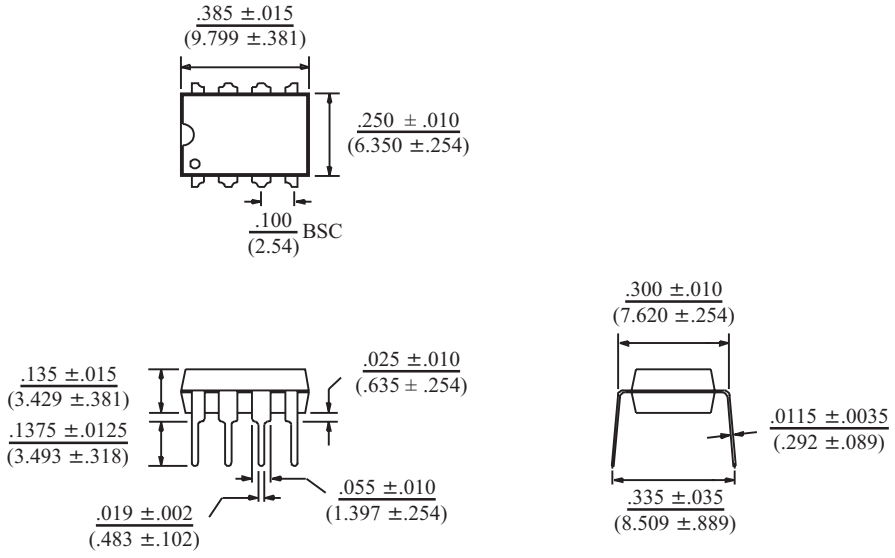


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

8-PIN PLASTIC DIP

inches (millimeters)

Package Type: 8P



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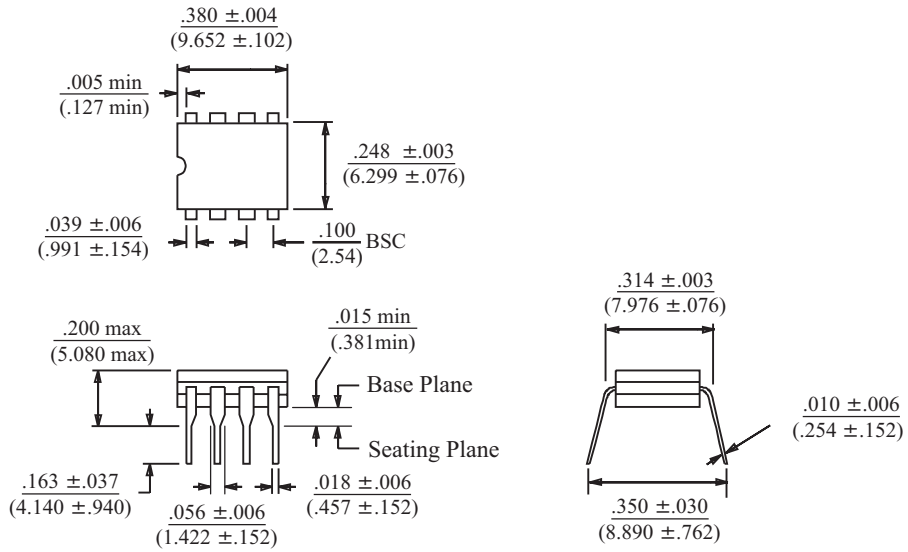
8-PIN CERDIP

inches (millimeters)

Package Type: 8D



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