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National Semiconductor

54F/74F433
First-In First-Out (FIFO) Buffer Memory

General Description

The 'F433 is an expandable fall-through type high-speed first-in first-out (FIFO) buffer memory that is optimized for high-speed disk or tape controller and communication buffer applications. It is organized as 64 words by 4 bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

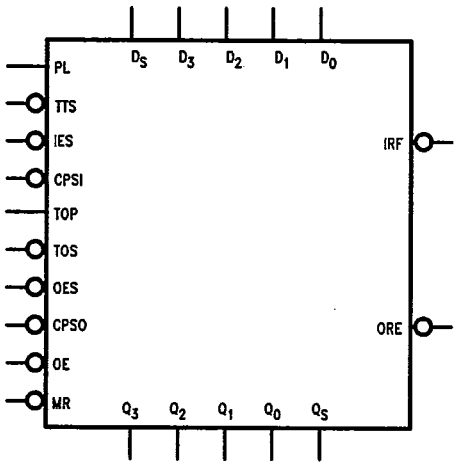
The 'F433 has TRI-STATE® outputs that provide added versatility, and is fully compatible with all TTL families.

Features

- Serial or parallel input
- Serial or parallel output
- Expandable without additional logic
- TRI-STATE outputs
- Fully compatible with all TTL families
- Slim 24-pin package
- 9423 replacement

Ordering Code: See Section 5

Logic Symbol



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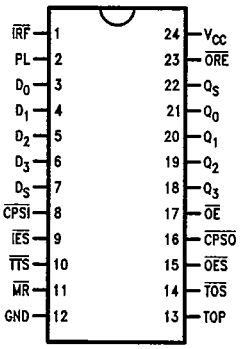
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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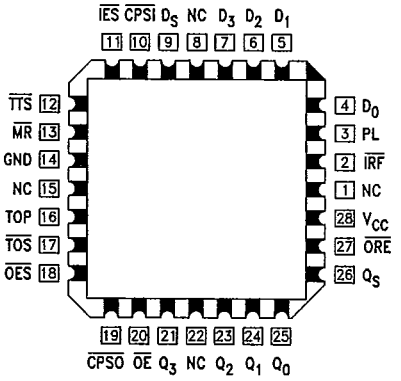
Pin Assignment for LCC and PCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F U.L. HIGH/LOW	54F/74F Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
PL	Parallel Load Input	1.0/0.66	20 μA/400 μA
$\overline{CPSI}$	Serial Input Clock	1.0/0.66	20 μA/400 μA
$\overline{IES}$	Serial Input Enable	1.0/0.66	20 μA/400 μA
$\overline{TTS}$	Transfer to Stack Input	1.0/0.66	20 μA/400 μA
$\overline{MR}$	Master Reset	1.0/0.66	20 μA/400 μA
$\overline{OES}$	Serial Output Enable	1.0/0.66	20 μA/400 μA
TOP	Transfer Out Parallel	1.0/0.66	20 μA/400 μA
$\overline{TOS}$	Transfer Out Serial	1.0/0.66	20 μA/400 μA
$\overline{CPSO}$	Serial Output Clock	1.0/0.66	20 μA/400 μA
$\overline{OE}$	Output Enable	1.0/0.66	20 μA/400 μA
D_0–D_3	Parallel Data Inputs	1.0/0.66	20 μA/400 μA
D_S	Serial Data Input	1.0/0.66	20 μA/400 μA
Q_0–Q_3	Parallel Data Outputs	285/10	5.7 mA/16 mA
Q_S	Serial Data Output	285/10	5.7 μA/16 mA
$\overline{IRF}$	Input Register Full	20/5	400 μA/8 mA
$\overline{ORE}$	Output Register Empty	20/5	400 μA/8 mA

Functional Description

As shown in the block diagram, the 'F433 consists of three sections:

1. An Input Register with parallel and serial data inputs, as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit-wide, 62-word-deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs, as well as control inputs and outputs for output handshaking and expansion.

These three sections operate asynchronously and are virtually independent of one another.

Input Register (Data Entry)

The Input Register can receive data in either bit-serial or 4-bit parallel form. It stores this data until it is sent to the fall-through stack, and also generates the necessary status and control signals.

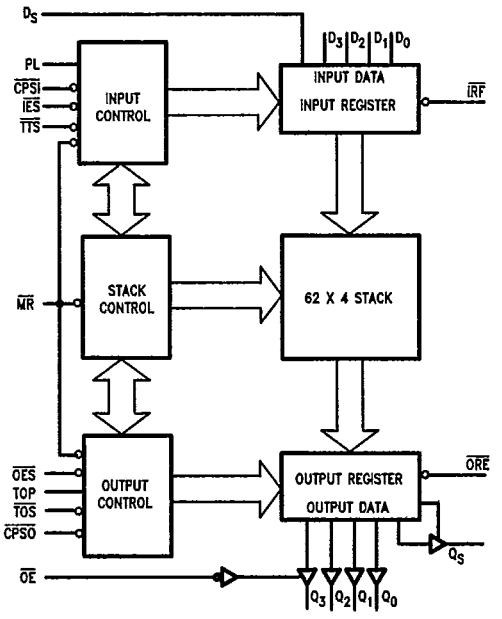
This 5-bit register (see *Figure 1*) is initialized by setting flip-flop F_3 and resetting the other flip-flops. The $\overline{Q}$-output of the last flip-flop (FC) is brought out as the Input Register Full (IRF) signal. After initialization, this output is HIGH.

Parallel Entry—A HIGH on the Parallel Load (PL) input loads the D_0–D_3 inputs into the F_0–F_3 flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW, indicating that the input register is full. During parallel entry, the Serial Input Clock ($\overline{CPSI}$) input must be LOW.

Serial Entry—Data on the Serial Data (D_S) input is serially entered into the shift register (F_3, F_2, F_1, F_0, FC) on each HIGH-to-LOW transition of the $\overline{CPSI}$ input when the Serial Input Enable ($\overline{IES}$) signal is LOW. During serial entry, the PL input should be LOW.

After the fourth clock transition, the four data bits are located in flip-flops F_0–F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ pulses from affecting the register. *Figure 2* illustrates the final positions in an 'F433 resulting from a 256-bit serial bit train (B_0 is the first bit, B_{255} the last).

Block Diagram



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Functional Description (Continued)

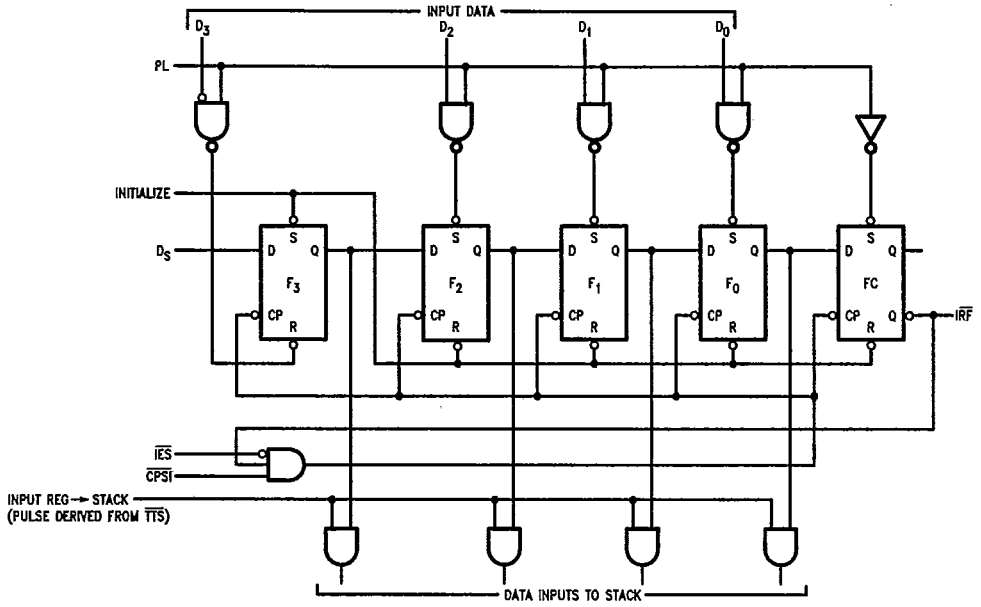

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FIGURE 1. Conceptual Input Section

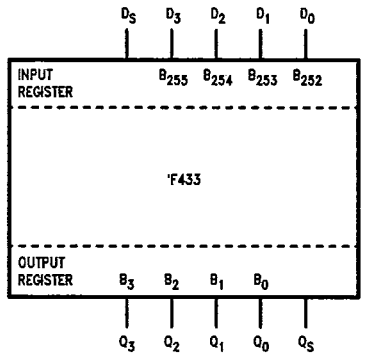

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FIGURE 2. Final Positions in an 'F433 Resulting from a 256-Bit Serial Train

Fall-Through Stack—The outputs of flip-flops F_0–F_3 feed the stack. A LOW level on the Transfer to Stack ($\overline{TTS}$) input initiates a fall-through action; if the top location of the stack is empty, data is loaded into the stack and the input register is reinitialized. (Note that this initialization is delayed until PL is LOW). Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS-type flip-flop (the initialization flip-flop) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack even though $\overline{IRF}$ and $\overline{TTS}$ may still be LOW; the initialization flip-flop is not cleared until PL goes LOW.

Once in the stack, data falls through automatically, pausing only when it is necessary to wait for an empty next location. In the 'F433, the master reset ($\overline{MR}$) input only initializes the stack control section and does not clear the data.

Output Register

The Output Register (see *Figure 3*) receives 4-bit data words from the bottom stack location, stores them, and outputs data on a TRI-STATE, 4-bit parallel data bus or on a TRI-STATE serial data bus. The output section generates and receives the necessary status and control signals.

Parallel Extraction—When the FIFO is empty after a LOW pulse is applied to the MR input, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the Transfer Out Parallel (TOP) input is HIGH. As a result of the data transfer, $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided that the TRI-STATE buffer is enabled). The TOP input can then be used to clock out the next word.

When TOP goes LOW, $\overline{ORE}$ also goes LOW, indicating that the output data has been extracted; however, the data itself remains on the output bus until a HIGH level on TOP permits the transfer of the next word (if available) into the output register. During parallel data extraction, the serial output clock ($\overline{CPSO}$) line should be LOW. The Transfer Out Serial ($\overline{TOS}$) line should be grounded for single-slice operation or connected to the appropriate $\overline{ORE}$ line for expanded operation (refer to the 'Expansion' section).

The TOP signal is not edge-triggered. Therefore, if TOP goes HIGH before data is available from the stack but data becomes available before TOP again goes LOW, that data is transferred into the output register. However, internal

Functional Description (Continued)

control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{ORE}$ remains LOW, indicating that there is no valid data at the outputs.

Serial Extraction—When the FIFO is empty after a LOW is applied to the MR input, the $\overline{ORE}$ output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the output register, if the $\overline{TOS}$ input is LOW and TOP is HIGH. As a result of the data transfer, $\overline{ORE}$ goes HIGH, indicating that valid data is in the register.

The TRI-STATE Serial Data Output (Q_S) is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the output register. The fourth transition empties the shift register, forces $\overline{ORE}$ LOW, and disables the serial output, Q_S. For serial operation, the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

Expansion

Vertical Expansion—The 'F433 may be vertically expanded, without external components, to store more words. The interconnections necessary to form a 190-word by 4-bit FIFO are shown in *Figure 4*. Using the same technique, any FIFO of (63n + 1)-words by 4-bits can be configured, where n is the number of devices. Note that expansion does not sacrifice any of the 'F433 flexibility for serial/parallel input and output.

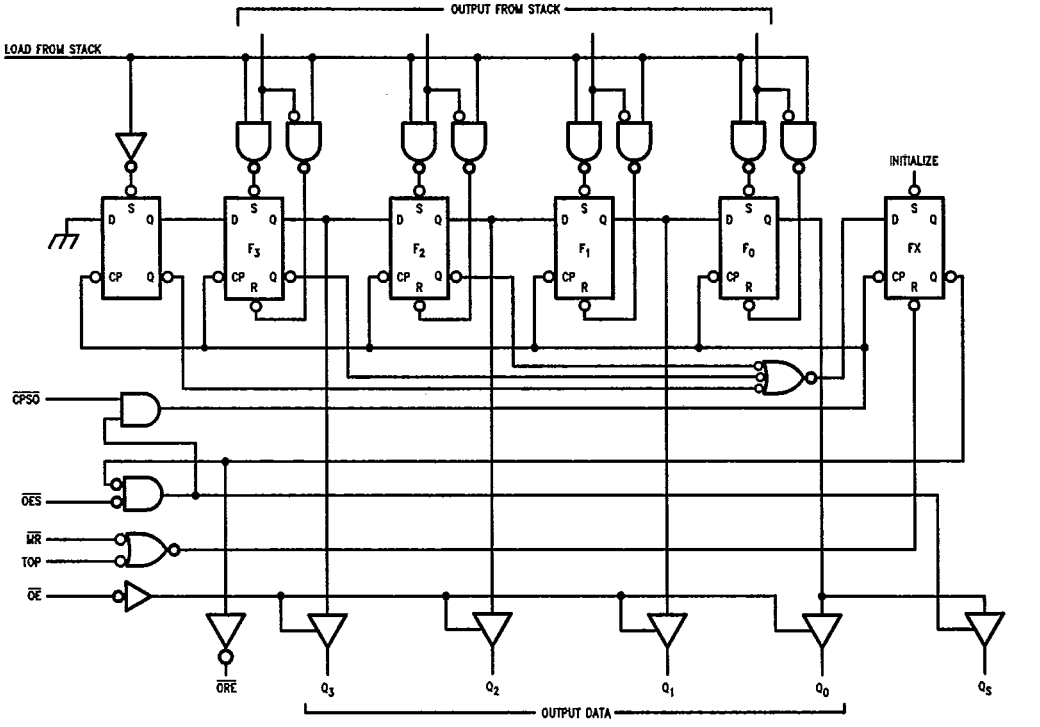

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FIGURE 3. Conceptual Output Section

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Functional Description (Continued)

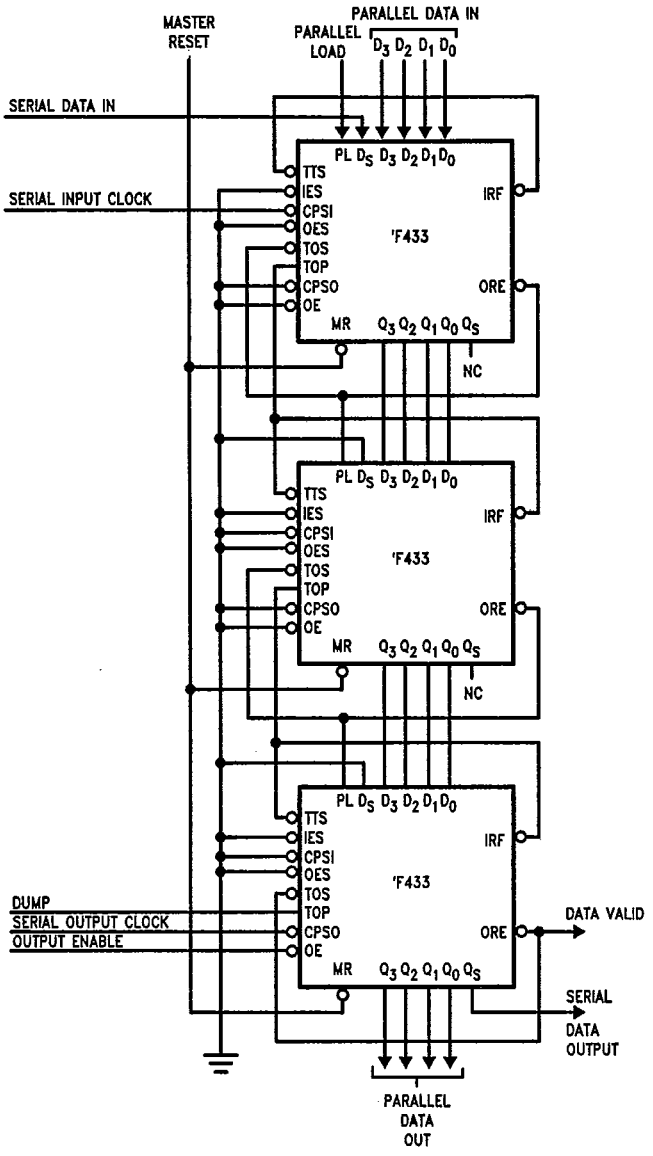

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FIGURE 4. A Vertical Expansion Scheme

Functional Description (Continued)

Horizontal Expansion—The 'F433 can be horizontally expanded, without external logic, to store long words (in multiples of 4-bits). The interconnections necessary to form a 64-word by 12-bit FIFO are shown in *Figure 5*. Using the same technique, any FIFO of 64-words by 4n-bits can be constructed, where n is the number of devices.

The right-most (most significant) device is connected to the $\overline{TTS}$ inputs of all devices. Similarly, the $\overline{ORE}$ output of the most significant device is connected to the $\overline{TOS}$ inputs of all devices. As in the vertical expansion scheme, horizontal expansion does not sacrifice any of the 'F433 flexibility for serial/parallel input and output.

It should be noted that the horizontal expansion scheme shown in *Figure 5* exacts a penalty in speed.

Horizontal and Vertical Expansion—The 'F433 can be expanded in both the horizontal and vertical directions without any external components and without sacrificing any of its FIFO flexibility for serial/parallel input and output. The interconnections necessary to form a 127-word by 16-bit FIFO are shown in *Figure 6*. Using the same technique, any FIFO of (63m+1)-words by 4n-bits can be configured, where m is the number of devices in a column and n is the number of devices in a row. *Figures 7* and *8* illustrate the timing diagrams for serial data entry and extraction for the FIFO shown in *Figure 6*. *Figure 9* illustrates the final positions of bits in an expanded 'F433 FIFO resulting from a 2032-bit serial bit train.

Interlocking Circuitry—Most conventional FIFO designs provide status signal analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit-to-unit operating speed require external gating to ensure that all devices have completed an operation. The 'F433 incorporates simple but effective 'master/slave' interlocking circuitry to eliminate the need for external gating.

In the 'F433 array of *Figure 6*, devices 1 and 5 are the row masters; the other devices are slaves to the master in their rows. No slave in a given row initializes its input register until it has received a LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

Similarly, the $\overline{ORE}$ outputs of slaves do not go HIGH until their inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes HIGH and that output data for the array may be extracted when the $\overline{ORE}$ output of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground, while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next-higher priority device. When an array of 'F433 FIFOs is initialized with a HIGH on the MR inputs of all devices, the $\overline{IRF}$ outputs of all devices are HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization.

Figure 10 is a conceptual logic diagram of the internal circuitry that determines master/slave operation. When $\overline{MR}$ and $\overline{IES}$ are LOW, the master latch is set. When $\overline{TTS}$ goes LOW, the initialization flip-flop is set. If the master latch is HIGH, the input register is immediately initialized and the initialization flip-flop reset. If the master latch is reset, the input register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ request flip-flop. If the master latch is set, the last output register flip-flop is set and the $\overline{ORE}$ line goes HIGH. If the master latch is reset, the $\overline{ORE}$ output is LOW until a Serial Output Enable ($\overline{OES}$) input is received.

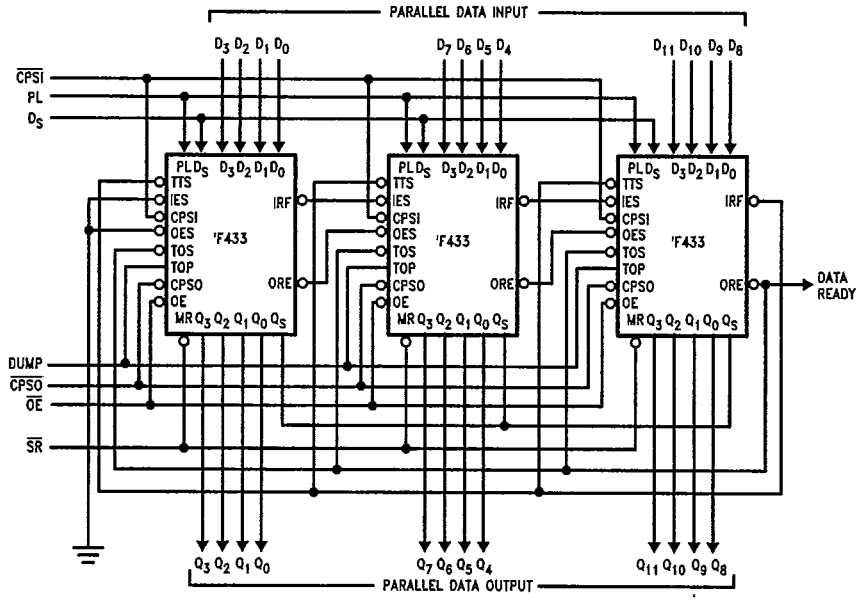

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FIGURE 5. A Horizontal Expansion Scheme

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Functional Description (Continued)

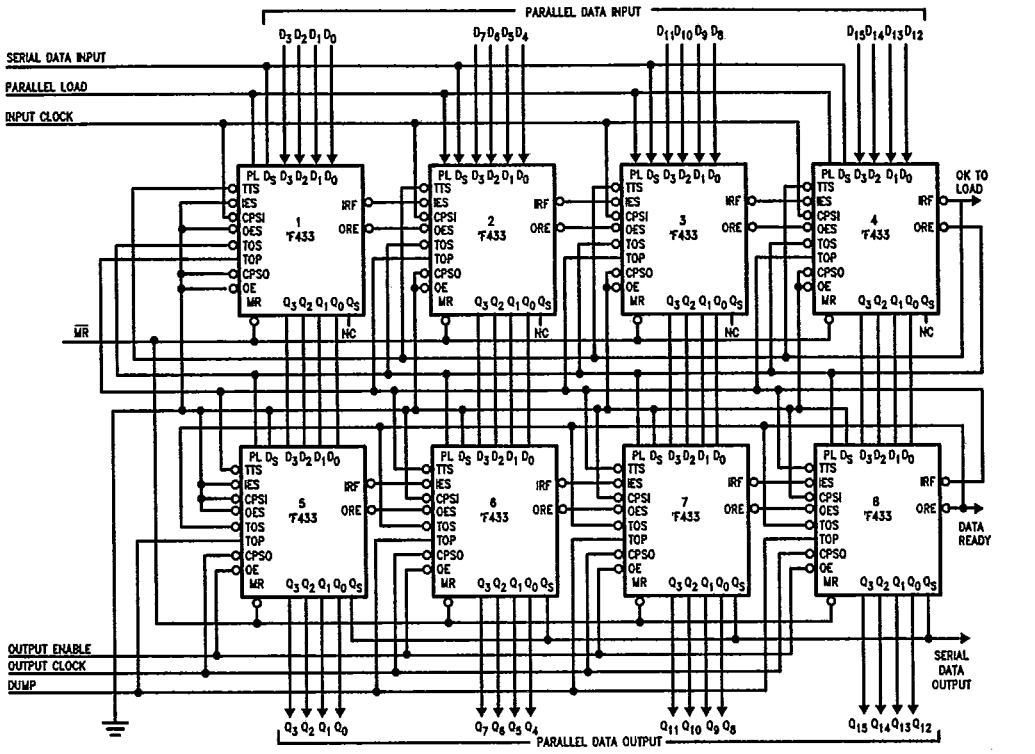

FIGURE 6. A 127 x 16 FIFO Array

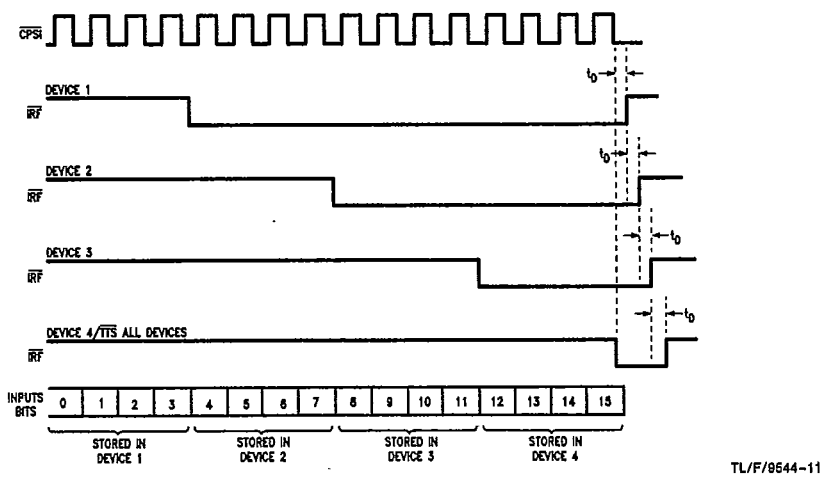

FIGURE 7. Serial Data Entry for Array of *Figure 6*

Functional Description (Continued)

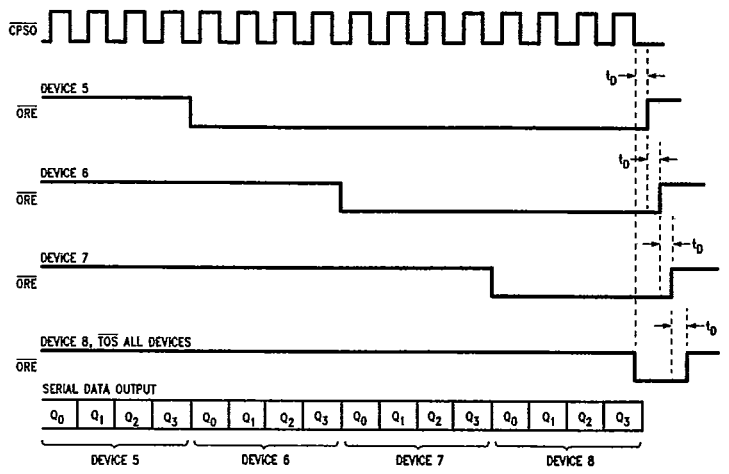

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FIGURE 8. Serial Data Extraction for Array of *Figure 6*

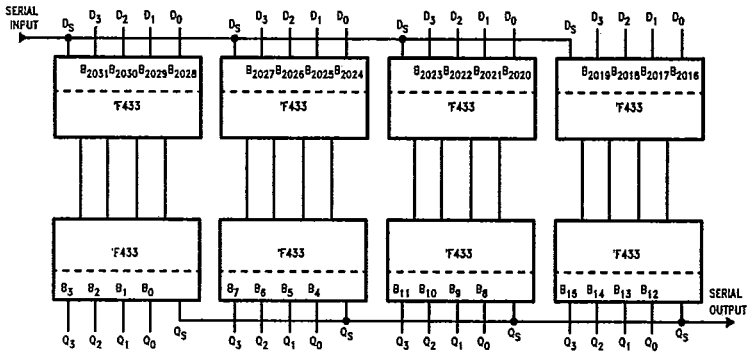

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FIGURE 9. Final Position of a 2032-Bit Serial Input

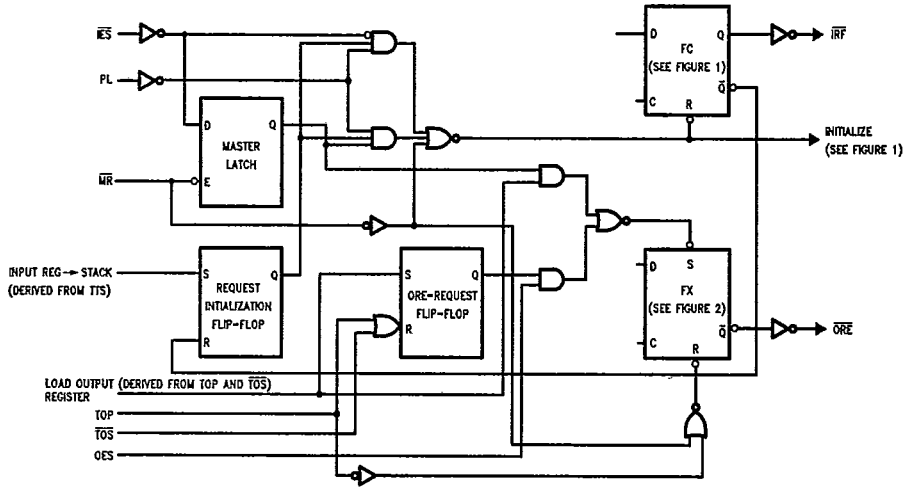

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FIGURE 10. Conceptual Diagram, Interlocking Circuitry

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.5	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.4			V	Min	I_{OH} = 400 μA ($\overline{ORE}$, $\overline{IRF}$)
		54F 10% V_{CC}	2.4					I_{OH} = 5.7 mA (Q_n, Q_s)
		74F 10% V_{CC}	2.4					I_{OH} = 400 μA ($\overline{ORE}$, $\overline{IRF}$)
		74F 10% V_{CC}	2.4					I_{OH} = 5.7 mA (Q_n, Q_s)
		74F 5% V_{CC}	2.7					I_{OH} = 400 μA ($\overline{ORE}$, $\overline{IRF}$)
		74F 5% V_{CC}	2.7					I_{OH} = 5.7 mA (Q_n, Q_s)
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.50	V	Min	I_{OL} = 8 mA ($\overline{ORE}$, $\overline{IRF}$)
		74F 10% V_{CC}			0.50			I_{OL} = 16 mA (Q_n, Q_s)
I_{IH}	Input HIGH Current				20	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				100	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−0.4	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V (Q_n, Q_s)
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V (Q_n, Q_s)
I_{OS}	Output Short-Circuit Current		−20		−130	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current				250	μA	Max	V_{OUT} = V_{CC}
I_{CC}	Power Supply Current			150	215	mA	Max	

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF		54F $T_A, V_{CC} =$ Mil $C_L = 50$ pF		74F $T_A, V_{CC} =$ Com $C_L = 50$ pF		Units	Fig No
		Min	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay, Negative-Going CPSI to $\overline{IRF}$ Output	2.0	17.0			2.0	18.0	ns	433-a,b
t_{PLH}	Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$	9.0	34.0			8.0	38.0		
t_{PLH} t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to Q_S Output	4.0 5.0	25.0 20.0			3.0 5.0	27.0 21.0	ns	433-c,d
t_{PLH} t_{PHL}	Propagation Delay, Positive-Going TOP to Q_0–Q_3 Outputs	8.0 7.0	35.0 30.0			7.0 7.0	38.0 32.0	ns	433-e
t_{PHL}	Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$	7.0	25.0			6.0	28.0	ns	433-c,d
t_{PHL}	Propagation Delay, Negative-Going TOP to $\overline{ORE}$	6.0	26.0			6.0	28.0	ns	433-e
t_{PLH}	Propagation Delay, Positive-Going TOP to $\overline{ORE}$	13.0	48.0			12.0	51.0		
t_{PLH}	Propagation Delay, Negative-Going $\overline{TOS}$ to Positive-Going $\overline{ORE}$	13.0	45.0			12.0	50.0	ns	433-c,d
PHL	Propagation Delay, Positive-Going PL to Negative-Going $\overline{IRF}$	4.0	22.0			4.0	23.0	ns	433-g,h
PLH	Propagation Delay, Negative-Going PL to Positive-Going $\overline{IRF}$	7.0	31.0			6.0	35.0		
PLH	Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$	9.0	38.0			8.0	44.0	ns	
PLH	Propagation Delay Positive-$\overline{IRF}$ Going $\overline{IES}$ to Positive-Going	5.0	25.0			5.0	27.0	ns	433-h
PHL	Propagation Delay MR to $\overline{ORE}$	7.0	28.0			7.0	31.0	ns	
PLH	Propagation Delay MR to $\overline{IRF}$	5.0	27.0			5.0	30.0	ns	
PZH PZL	Enable Time $\overline{OE}$ to Q_0–Q_3	1.0 1.0	16.0 14.0			1.0 1.0	18.0 16.0	ns	
PHZ PLZ	Disable Time $\overline{OE}$ to Q_0–Q_3	1.0 1.0	10.0 23.0			1.0 1.0	12.0 30.0		
PZH PZL	Enable Time Negative-Going $\overline{OES}$ to Q_S	1.0 1.0	10.0 14.0			1.0 1.0	12.0 15.0	ns	
PHZ PLZ	Disable Time Negative-Going $\overline{OES}$ to Q_S	1.0 1.0	10.0 14.0			1.0 1.0	12.0 16.0		
PZH PZL	Enable Time $\overline{TOS}$ to Q_S	1.0 1.0	35.0 35.0			1.0 1.0	42.0 39.0	ns	
DFT	Fall-Through Time	0.2	0.9			0.2	1.0	ns	433-f
AP	Parallel Appearance Time $\overline{ORE}$ to Q_0–Q_3	−20.0	−2.0			−20.0	−2.0	ns	
AS	Serial Appearance Time $\overline{ORE}$ to Q_S	−20.0	5.0			−20.0	5.0		

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AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units	Fig No
		Min	Max	Min	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_S to Negative $\overline{CPSI}$	7.0 7.0				7.0 7.0		ns	433-a,b
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_S to $\overline{CPSI}$	2.0 2.0				2.0 2.0			
$t_s(L)$	Setup Time, LOW $\overline{TTS}$ to $\overline{IRF}$, Serial or Parallel Mode	0.0				0.0		ns	433-a,b,g,h
$t_s(L)$	Setup Time, LOW Negative-Going $\overline{ORE}$ to Negative-Going $\overline{TOS}$	0.0				0.0		ns	433-c,d
$t_s(L)$	Setup Time, LOW Negative-Going $\overline{IES}$ to $\overline{CPSI}$	8.0				9.0		ns	433-b
$t_s(L)$	Setup Time, LOW Negative-Going $\overline{TTS}$ to $\overline{CPSI}$	30.0				33.0		ns	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW Parallel Inputs to PL	0.0 0.0				0.0 0.0		ns	
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW Parallel Inputs to PL	4.0 4.0				4.0 4.0			
$t_w(H)$ $t_w(L)$	$\overline{CPSI}$ Pulse Width HIGH or LOW	10.0 5.0				11.0 6.0		ns	433-a,b
$t_w(H)$	PL Pulse Width, HIGH	7.0				9.0		ns	433-g,h
$t_w(L)$	$\overline{TTS}$ Pulse Width, LOW Serial or Parallel Mode	7.0				9.0		ns	433-a,b,c,d
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	7.0				9.0		ns	433-f
$t_w(H)$ $t_w(L)$	TOP Pulse Width HIGH or LOW	14.0 7.0				16.0 7.0		ns	433-e
$t_w(H)$ $t_w(L)$	$\overline{CPSO}$ Pulse Width HIGH or LOW	14.0 7.0				16.0 7.0		ns	433-c,d
t_{rec}	Recovery Time $\overline{MR}$ to Any Input	8.0				15.0		ns	433-f

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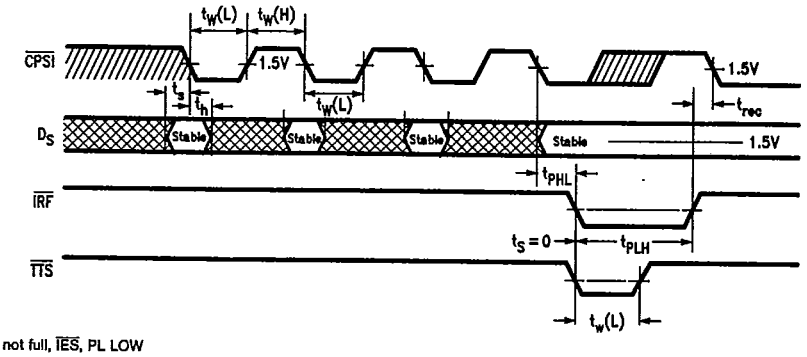
Timing Waveforms



Conditions: Stack not full, $\overline{IES}$, PL LOW

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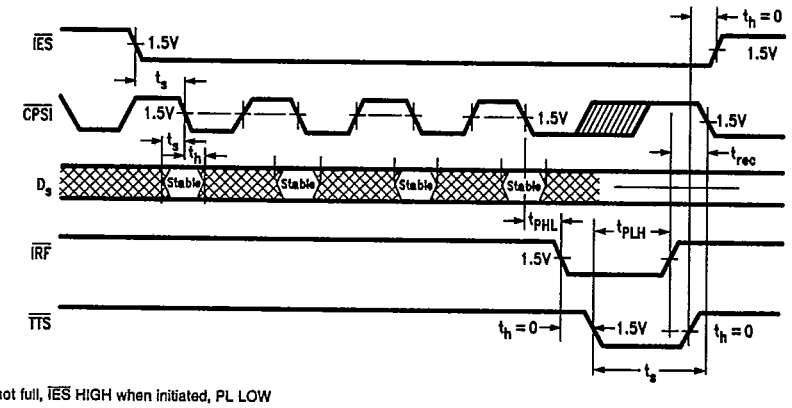
FIGURE 433-a. Serial Input, Unexpanded or Master Operation



Conditions: Stack not full, $\overline{IES}$ HIGH when initiated, PL LOW

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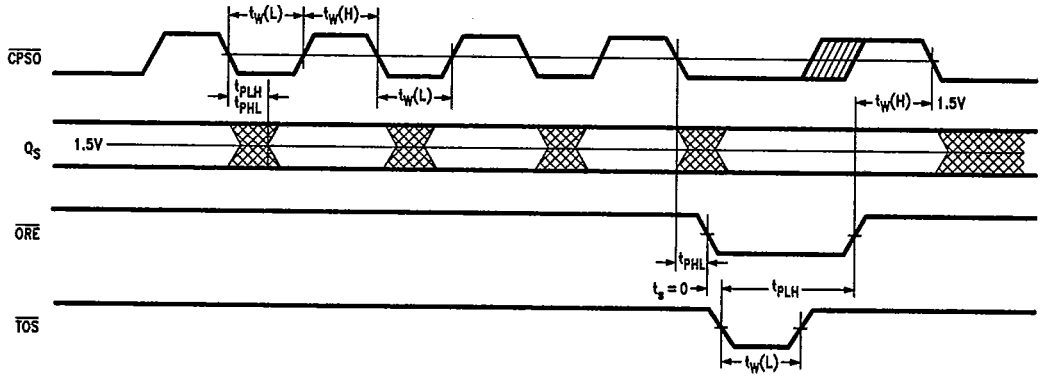
FIGURE 433-b. Serial Input, Expanded Slave Operation



Conditions: Data in stack, TOP HIGH, $\overline{IES}$ LOW when initiated, $\overline{OES}$ LOW

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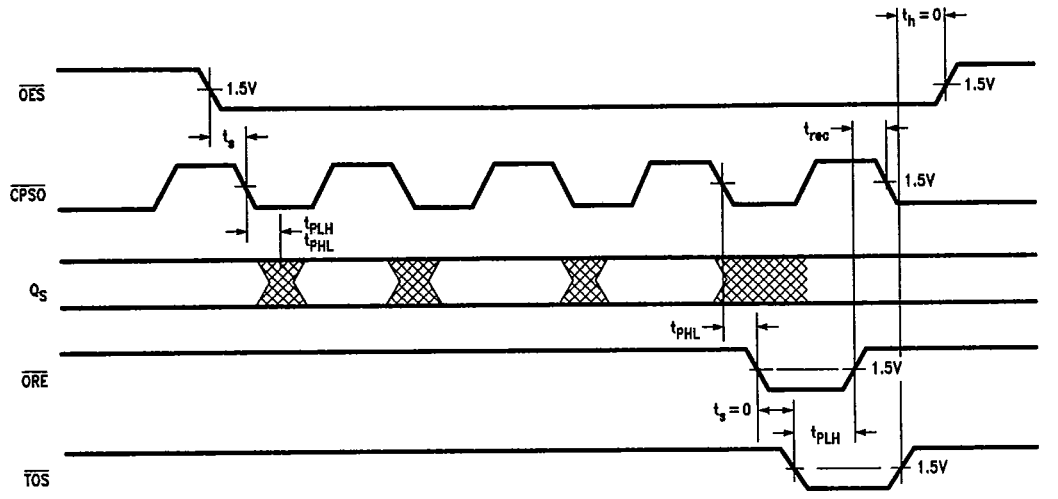
FIGURE 433-c. Serial Output, Unexpanded or Master Operation

Timing Waveforms (Continued)



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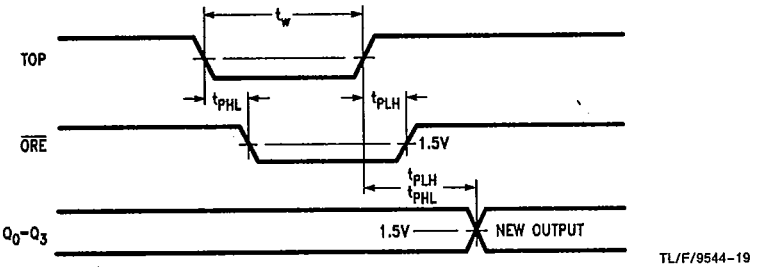
Conditions: Data in stack, TOP HIGH, $\overline{IES}$ HIGH when initiated

FIGURE 433-d. Serial Output, Slave Operation



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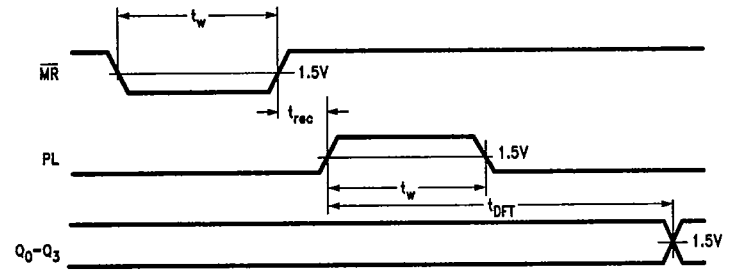
Conditions: $\overline{IES}$ LOW when initiated, $\overline{OE}$, $\overline{CPSO}$ LOW; data available in stack

FIGURE 433-e. Parallel Output, 4-Bit Word or Master in Parallel Expansion



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Conditions: $\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{OE}$, $\overline{CPSO}$ LOW, TOP HIGH

FIGURE 433-f. Fall Through Time