

TrenchMOS™ transistor Logic level FET

BUK9880-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. The device features very low on-state resistance and has integral zener diodes giving ESD protection. It is intended for use in automotive and general purpose switching applications.

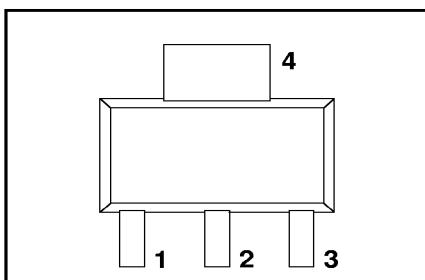
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current	7.5	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 5$ V	80	$\text{m}\Omega$

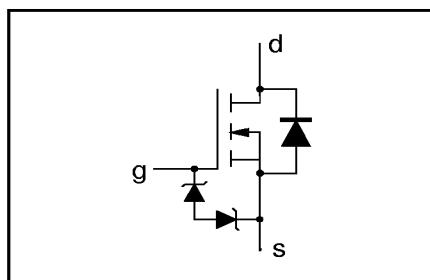
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	7.5	A
I_D	Drain current (DC)	On PCB in Fig.2	-	3.5	A
I_D	Drain current (DC)	$T_{amb} = 25 \text{ }^\circ\text{C}$	-	2.2	A
I_{DM}	Drain current (pulse peak value)	On PCB in Fig.2	-	40	A
P_{tot}	Total power dissipation	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	8.3	W
P_{tot}	Total power dissipation	$T_{sp} = 25 \text{ }^\circ\text{C}$	-	1.8	W
T_{stg}, T_j	Storage & operating temperature	On PCB in Fig.2	-	150	$^\circ\text{C}$
		$T_{amb} = 25 \text{ }^\circ\text{C}$	-55		

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 k Ω)	-	2	kV

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	From junction to solder point	Mounted on any PCB	12	15	K/W
$R_{th\ j-amb}$	From junction to ambient	Mounted on PCB of Fig.18	-	70	K/W

STATIC CHARACTERISTICS $T_j = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 V; I_D = 0.25 \text{ mA}$	55	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$T_j = -55^\circ C$	50	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	1.0	1.5	2.0	V
I_{GSS}	Gate source leakage current	$T_j = 150^\circ C$	0.6	-	-	V
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	$T_j = -55^\circ C$	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{DS} = 55 V; V_{GS} = 0 V;$ $I_G = \pm 1 \text{ mA}$	-	0.05	10	μA
		$T_j = 150^\circ C$	-	-	100	μA
		$V_{GS} = \pm 5 V$	-	0.02	1	μA
		$I_G = \pm 1 \text{ mA}$	-	-	5	μA
		$V_{GS} = 5 V; I_D = 5 \text{ A}$	10	-	-	V
			-	65	80	$m\Omega$
			-	-	148	$m\Omega$
		$T_j = 150^\circ C$	-	-	-	

DYNAMIC CHARACTERISTICS $T_{mb} = 25^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25 V; I_D = 5 A; T_j = 25^\circ C$	4	8	-	S
C_{iss}	Input capacitance	$V_{GS} = 0 V; V_{DS} = 25 V; f = 1 \text{ MHz}$	-	500	650	pF
C_{oss}	Output capacitance		-	110	135	pF
C_{rss}	Feedback capacitance		-	60	85	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30 V; I_D = 7 A;$	-	10	15	ns
t_r	Turn-on rise time	$V_{GS} = 5 V; R_G = 10 \Omega;$	-	30	50	ns
$t_{d\ off}$	Turn-off delay time		-	30	45	ns
t_f	Turn-off fall time	$T_j = 25^\circ C$	-	30	40	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = -55$ to $175^\circ C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	$T_{sp} = 25^\circ C$	-	-	7.5	A
I_{DRM}	Pulsed reverse drain current	$T_{sp} = 25^\circ C$	-	-	40	A
V_{SD}	Diode forward voltage	$I_F = 5 A; V_{GS} = 0 V$	-	0.85	1.1	V
t_{rr}	Reverse recovery time	$I_F = 5 A; -dI_F/dt = 100 A/\mu s;$	-	38	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = -10 V; V_R = 30 V$	-	0.2	-	μC

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AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 2.5 \text{ A}$; $V_{DD} \leq 25 \text{ V}$; $V_{GS} = 5 \text{ V}$; $R_{GS} = 50 \Omega$; $T_{sp} = 25^\circ\text{C}$	-	-	30	mJ

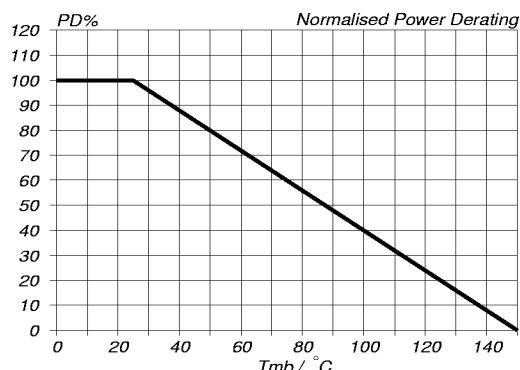


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D/P_{D, 25^\circ\text{C}} = f(T_{sp})$

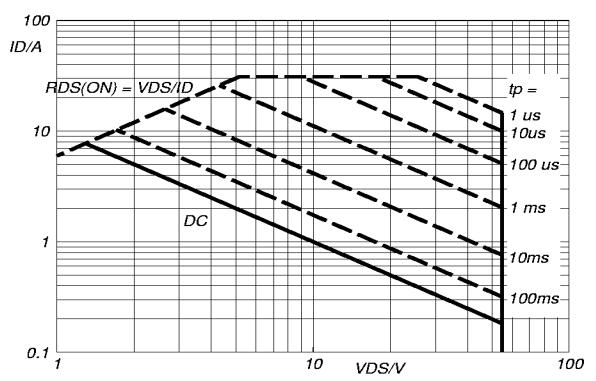


Fig.3. Safe operating area. $T_{sp} = 25^\circ\text{C}$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

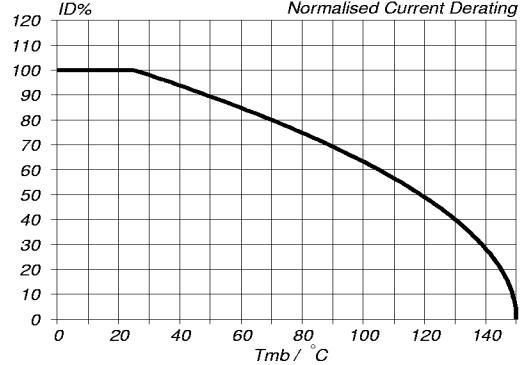


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D/I_{D, 25^\circ\text{C}} = f(T_{sp})$; conditions: $V_{GS} \geq 5 \text{ V}$

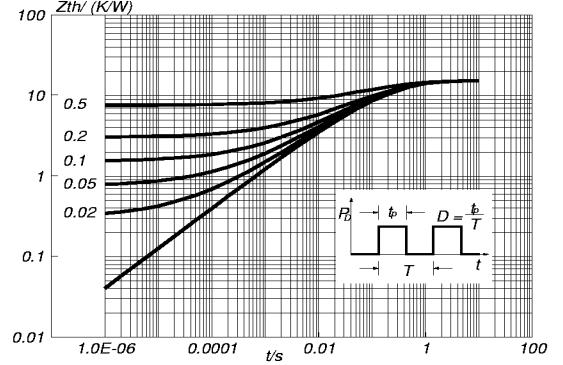


Fig.4. Transient thermal impedance.
 $Z_{th,j-sp} = f(t)$; parameter $D = t_p/T$

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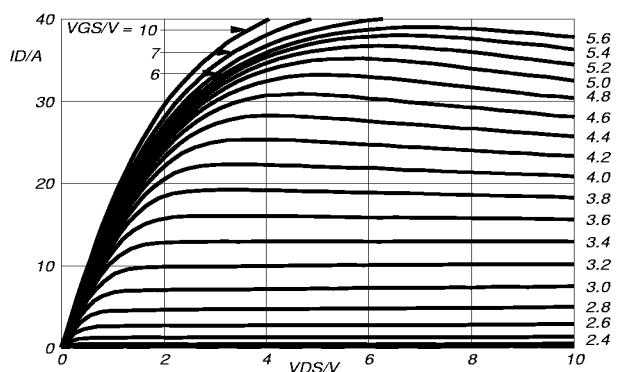


Fig.5. Typical output characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

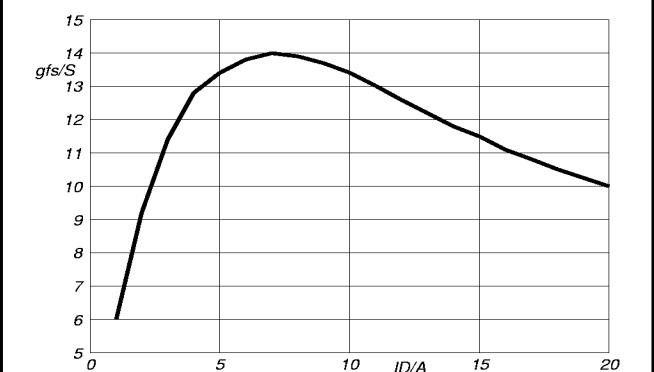


Fig.8. Typical transconductance, $T_j = 25^\circ\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

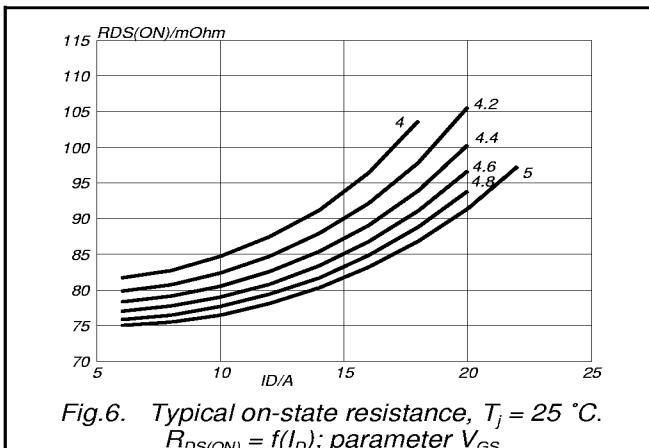


Fig.6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

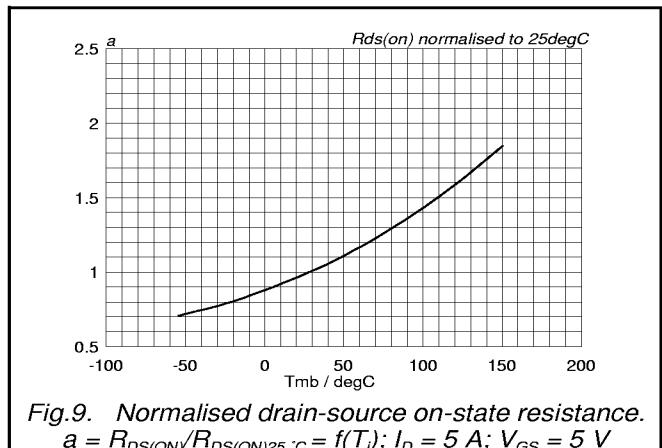


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25^\circ\text{C}} = f(T_j)$; $I_D = 5\text{ A}$; $V_{GS} = 5\text{ V}$

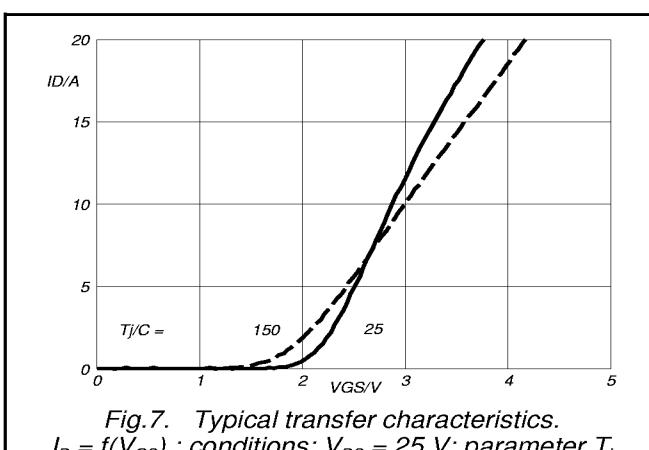


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

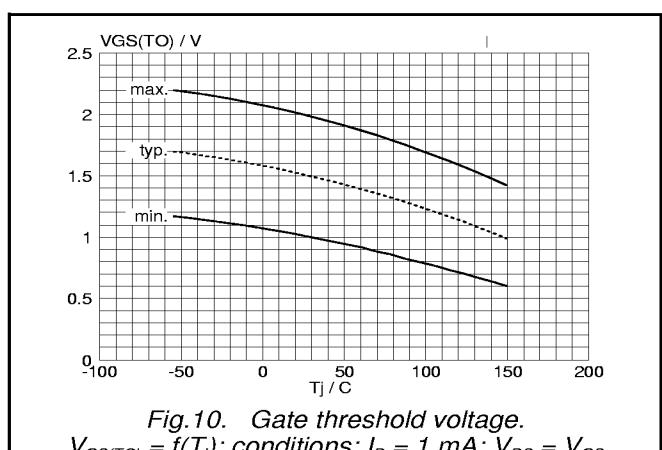


Fig.10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

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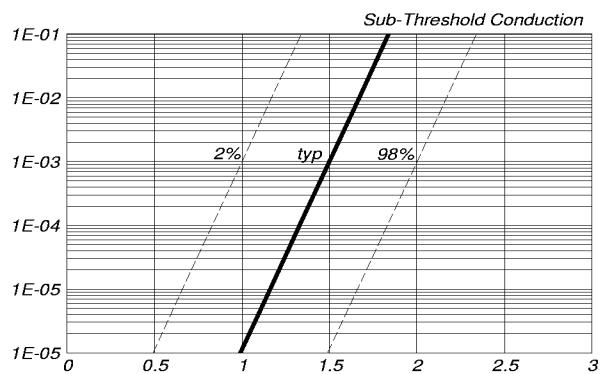


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

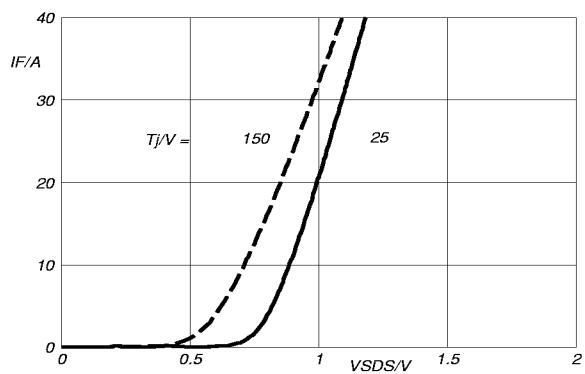


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0 \text{ V}$; parameter T_j

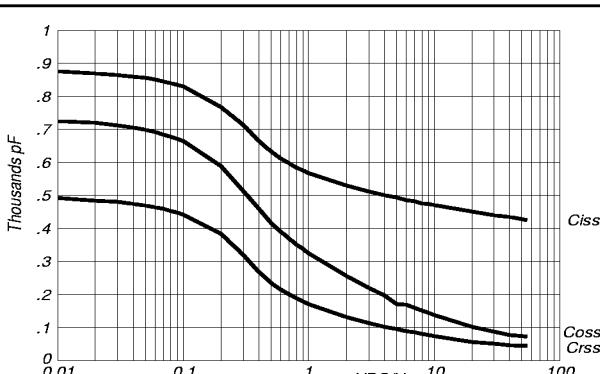


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} , C_{riss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

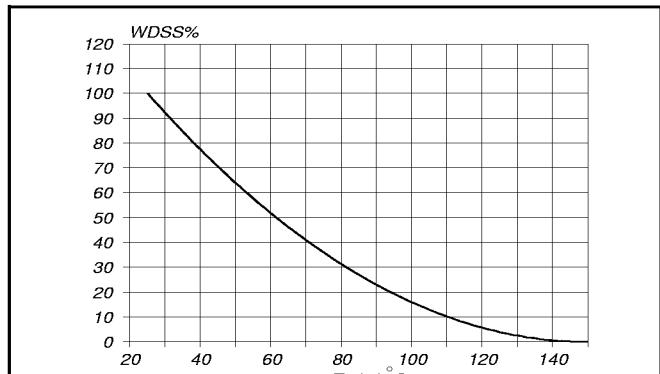


Fig.15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{sp})$; conditions: $I_D = 2.5 \text{ A}$

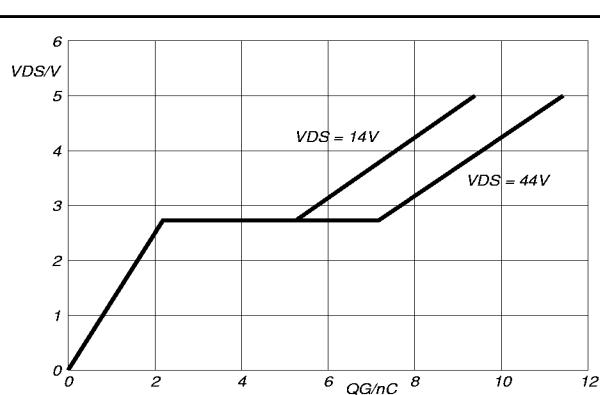


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 7 \text{ A}$; parameter V_{DS}

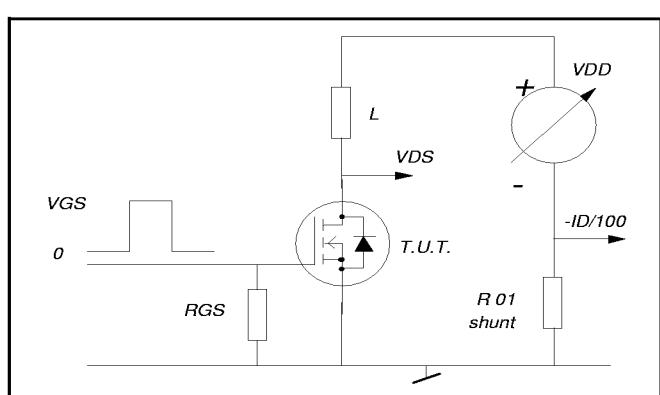
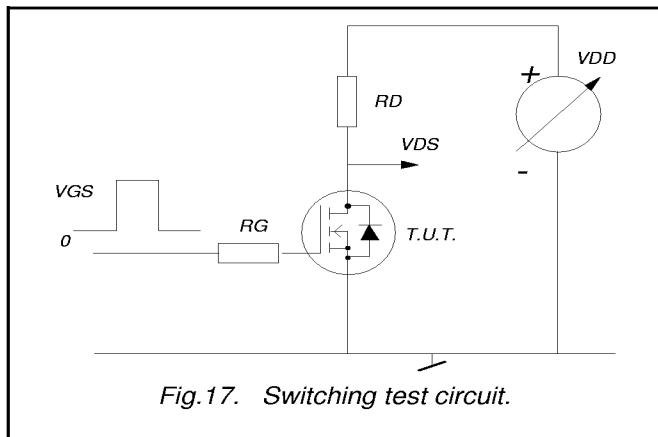
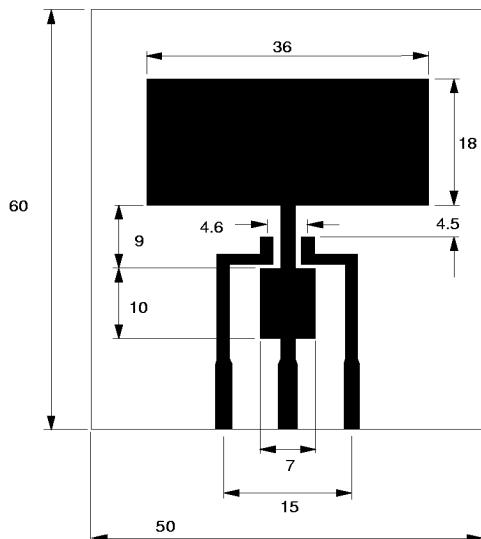


Fig.16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

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**TrenchMOS™ transistor
Logic level FET****BUK9880-55****PRINTED CIRCUIT BOARD***Dimensions in mm.*

*Fig.18. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).*

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MECHANICAL DATA*Dimensions in mm*

Net Mass: 0.11 g

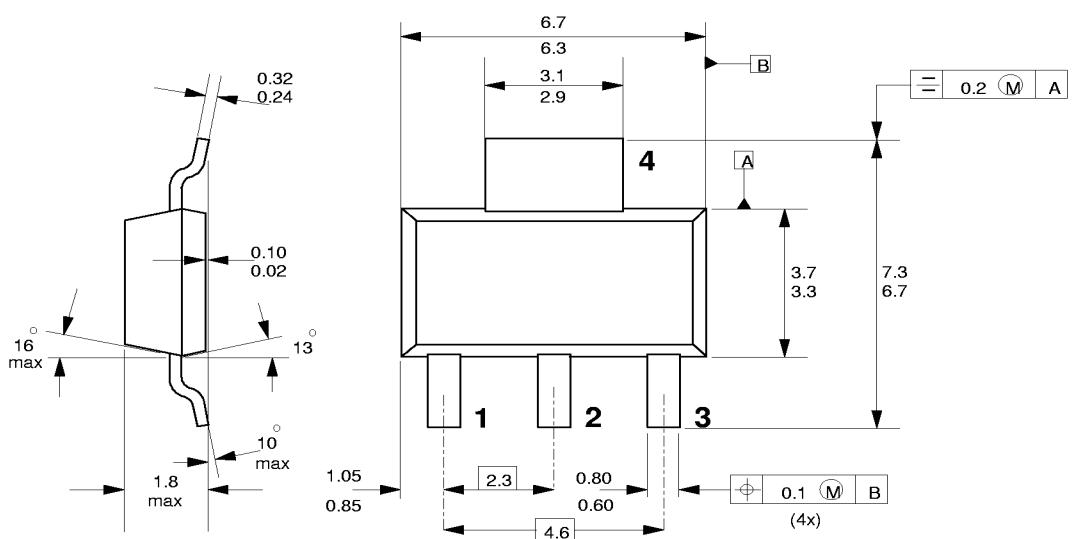


Fig.19. SOT223 surface mounting package.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".