18 Mb Burst of 4 Pipelined SRAM with QDR Architecture

Features

- Separate Independent Read and Write Data Ports
  - Supports concurrent transactions
- 167 MHz Clock for High Bandwidth
  - 2.5 ns Clock-to-Valid access time
- 4-Word Burst for reducing the address bus frequency
- Double Data Rate (DDR) interfaces on both Read & Write Ports (data transferred at 333 MHz) @167 MHz
- Two input clocks (K and $\overline{K}$) for precise DDR timing
  - SRAM uses rising edges only
- Two output clocks (C and $\overline{C}$) accounts for clock skew and flight time mis-matches
- Single multiplexed address input bus latches address inputs for both READ and WRITE ports
- Separate Port Selects for depth expansion
- Synchronous internally self-timed writes
- 2.5V core power supply with HSTL Inputs and Outputs
- 13x15 mm 1.0 mm pitch fBGA package, 165 ball (11x15 matrix)
- Variable drive HSTL output buffers
- Expanded HSTL output voltage (1.4V–1.9V)
- JTAG Interface

Configurations

CY7C1305V25 – 1 Mb x 18

CY7C1307V25 – 512K x 36

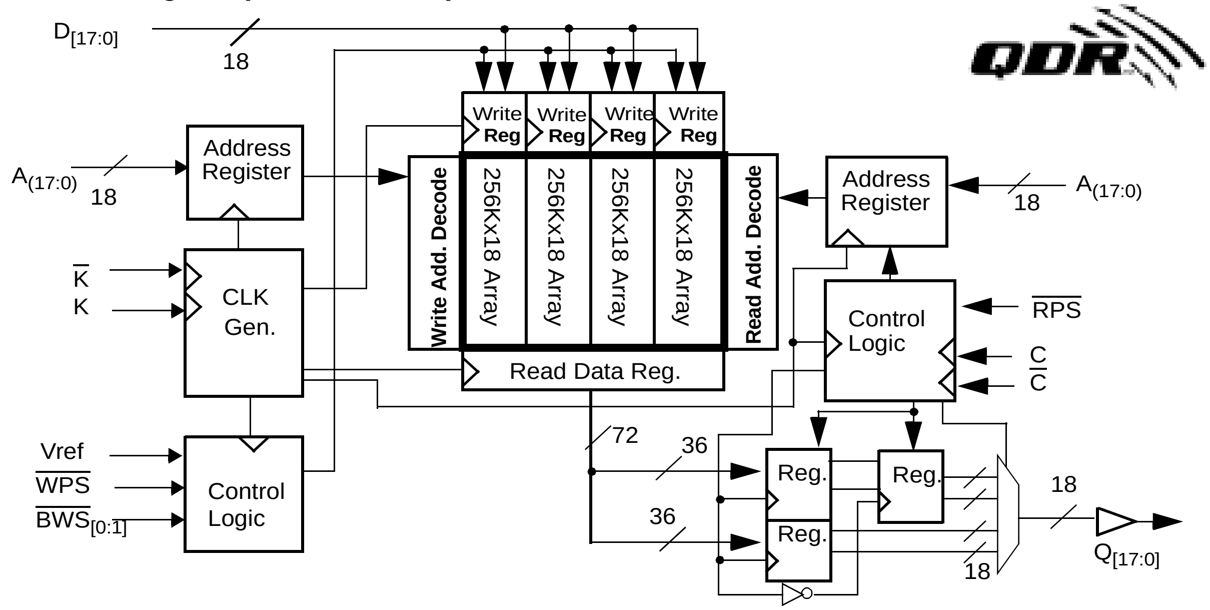
Functional Description

The CY7C1305V25/CY7C1307V25 are 2.5V Synchronous Pipelined SRAMs equipped with QDR architecture. QDR architecture consists of two separate ports to access the memory array. The Read port has dedicated Data Outputs to support Read operations and the Write Port has dedicated Data Inputs to support Write operations. QDR architecture has separate data inputs and data outputs to completely eliminate the need to "turn-around" the data bus required with common I/O devices. Access to each port is accomplished through a common address bus. Addresses for Read and Write addresses are latched on alternate rising edges of the input (K) clock. Accesses to the device's Read and Write ports are completely independent of one another. In order to maximize data throughput, both Read and Write ports are equipped with Double Data Rate (DDR) interfaces. Each address location is associated with four 18-bit words (CY7C1305V25) and four 36-bit words (CY7C1307V25) that burst sequentially into or out of the device. Since data can be transferred into and out of the device on every rising edge of both input clocks (K/$\overline{K}$ and C/$\overline{C}$) memory bandwidth is maximized while simplifying system design by eliminating bus "turn-arounds."

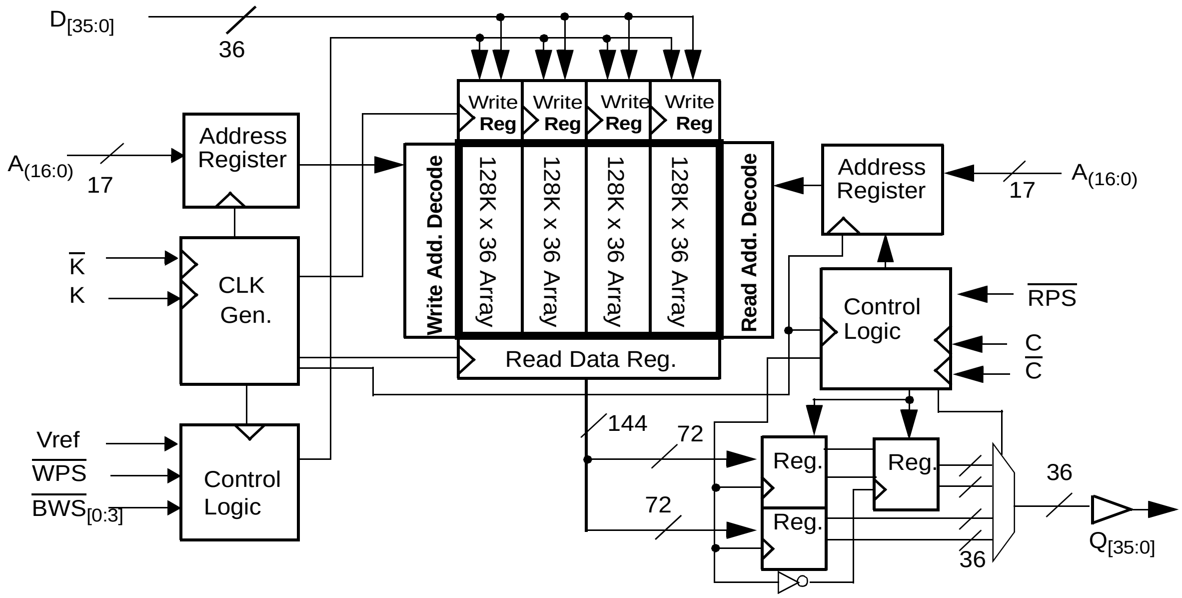
Depth expansion is accomplished with Port Selects for each port. Port selects allow each port to operate independently.

All synchronous inputs pass through input registers controlled by the K or $\overline{K}$ input clocks. All data outputs pass through output registers controlled by the C or $\overline{C}$ input clocks. Writes are conducted with on-chip synchronous self-timed write circuitry.

Logic Block Diagram (CY7C1305V25)



Logic Block Diagram (CY7C1307V25)



Selection Guide[1]

	7C1305V25-200 7C1307V25-200	7C1305V25-167 7C1307V25-167	7C1305V25-133 7C1307V25-133	7C1305V25-100 7C1307V25-100
Maximum Operating Frequency (MHz)	200	167	133	100
Maximum Operating Current (mA)	500	450	350	230

Note:
1. Shaded areas contain advance information.

Pin Configuration - CY7C1305V25 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	Gnd/ 144M	NC/ 36M	$\overline{\text{WPS}}$	$\overline{\text{BWS}}_1$	$\overline{\text{K}}$	NC	$\overline{\text{RPS}}$	A	Gnd/ 72M	NC
B	NC	Q9	D9	A	NC	K	$\overline{\text{BWS}}_0$	A	NC	NC	Q8
C	NC	NC	D10	VSS	A	NC	A	VSS	NC	Q7	D8
D	NC	D11	Q10	VSS	VSS	VSS	VSS	VSS	NC	NC	D7
E	NC	NC	Q11	VDDQ	VSS	VSS	VSS	VDDQ	NC	D6	Q6
F	NC	Q12	D12	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	Q5
G	NC	D13	Q13	VDDQ	VDD	VSS	VDD	VDDQ	NC	NC	D5
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	NC	NC	D14	VDDQ	VDD	VSS	VDD	VDDQ	NC	Q4	D4
K	NC	NC	Q14	VDDQ	VDD	VSS	VDD	VDDQ	NC	D3	Q3
L	NC	Q15	D15	VDDQ	VSS	VSS	VSS	VDDQ	NC	NC	Q2
M	NC	NC	D16	VSS	VSS	VSS	VSS	VSS	NC	Q1	D2
N	NC	D17	Q16	VSS	A	A	A	VSS	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	$\overline{\text{C}}$	A	A	A	TMS	TDI

Pin Configuration - CY7C1307V25 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	Gnd/ 288M	NC/ 72M	$\overline{WPS}$	$\overline{BWS_2}$	$\overline{K}$	$\overline{BWS_1}$	$\overline{RPS}$	NC/36 M	Gnd/ 144M	NC
B	Q27	Q18	D18	A	$\overline{BWS_3}$	K	$\overline{BWS_0}$	A	D17	Q17	Q8
C	D27	Q28	D19	VSS	A	NC	A	VSS	D16	Q7	D8
D	D28	D20	Q19	VSS	VSS	VSS	VSS	VSS	Q16	D15	D7
E	Q29	D29	Q20	VDDQ	VSS	VSS	VSS	VDDQ	Q15	D6	Q6
F	Q30	Q21	D21	VDDQ	VDD	VSS	VDD	VDDQ	D14	Q14	Q5
G	D30	D22	Q22	VDDQ	VDD	VSS	VDD	VDDQ	Q13	D13	D5
H	NC	VREF	VDDQ	VDDQ	VDD	VSS	VDD	VDDQ	VDDQ	VREF	ZQ
J	D31	Q31	D23	VDDQ	VDD	VSS	VDD	VDDQ	D12	Q4	D4
K	Q32	D32	Q23	VDDQ	VDD	VSS	VDD	VDDQ	Q12	D3	Q3
L	Q33	Q24	D24	VDDQ	VSS	VSS	VSS	VDDQ	D11	Q11	Q2
M	D33	Q34	D25	VSS	VSS	VSS	VSS	VSS	D10	Q1	D2
N	D34	D26	Q25	VSS	A	A	A	VSS	Q10	D9	D1
P	Q35	D35	Q26	A	A	C	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

Pin Definitions

Name	I/O	Description
$D_{[x:0]}$	Input-Synchronous	Data input signals, sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations. CY7C1305V25 – $D_{[17:0]}$ CY7C1307V25 – $D_{[35:0]}$
$\overline{WPS}$	Input-Synchronous	Write Port Select, active LOW. Sampled on the rising edge of the K clock. When asserted active, a write operation is initiated. Deasserting will deselect the Write port. Deselecting the Write port will cause $D_{[x:0]}$ to be ignored.
$\overline{BWS}_0$, $\overline{BWS}_1$, $\overline{BWS}_2$, $\overline{BWS}_3$	Input-Synchronous	Byte Write Select 0, 1, 2, and 3 - active LOW. Sampled on the rising edge of the K and $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. CY7C1305V25 - $\overline{BWS}_0$ controls $D_{[8:0]}$ and $\overline{BWS}_1$ controls $D_{[17:9]}$ CY7C1307V25 - $\overline{BWS}_0$ controls $D_{[8:0]}$, $\overline{BWS}_1$ controls $D_{[17:9]}$, $\overline{BWS}_2$ controls $D_{[26:18]}$ and $\overline{BWS}_3$ controls $D_{[35:27]}$ All the byte writes are sampled on the same edge as the data. Deselecting a Byte Write Select will cause the corresponding byte of data to be ignored and not written into the device.
A	Input-Synchronous	Address Inputs. Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both Read and Write operations. Internally, the device is organized as 1 Mb x 18 (4 arrays each of 256K x 18) for CY7C1305V25 and 256K x 36 (4 arrays each of 128K x 36) for CY7C1307V25. Therefore, only 18 address inputs for CY7C1305V25 and 17 address inputs for CY7C1307V25.These inputs are ignored when the appropriate port is deselected.
$Q_{[x:0]}$	Outputs-Synchronous	Data Output signals. These pins drive out the requested data during a Read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during Read operations or K and $\overline{K}$. when in single clock mode. When the Read port is deselected, $Q_{[x:0]}$ are automatically three-stated. CY7C1305V25 - $Q_{[17:0]}$ CY7C1307V25 - $Q_{[35:0]}$
$\overline{RPS}$	Input-Synchronous	Read Port Select, active LOW. Sampled on the rising edge of positive input clock (K). When active, a Read operation is initiated. Deasserting will cause the Read port to be deselected. When deselected, the pending access is allowed to complete and the output drivers are automatically three-stated following the next rising edge of the K clock. Each read access consists of a burst of four sequential 18-bit or 36-bit transfers.
C	Input-Clock	Positive Output Clock, input. C is used in conjunction with $\overline{C}$ to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
$\overline{C}$	Input-Clock	Negative Output Clock, input. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board cack to the controller. See application example for further details.
K	Input-Clock	Positive Input Clock, input. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input-Clock	Negative Input Clock Input. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through $Q_{[x:0]}$ when in single clock mode.
ZQ	Input	Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. $Q_{[x:0]}$ output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to V_{DD}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

Pin Definitions

TDO	Output	TDO for JTAG.
TCK	Input	TCK pin for JTAG.
TDI	Input	TDI pin for JTAG.
TMS	Input	TMS pin for JTAG.
NC/36M	Input	Address expansion for 36M. This is not connected to the die. Can be connected to any voltage level on CY7C1305V25/CY7C1307V25.
GND/72M	Input	Address expansion for 72M. This should be tied low on the CY7C1305V25
NC/72M	Input	Address expansion for 72M. This can be connected to any voltage level on CY7C1307V25
GND/144M	Input	Address expansion for 144M. This should be tied low on CY7C1305V25/CY7C1307V25.
GND/288M	Input	Address expansion for 144M. This should be tied low on CY7C1307V25.
V_{REF}	Input-Reference	Reference Voltage Input. Static input used to set the reference level for HSTL inputs and Outputs as well as A/C measurement points.
V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 2.5V power supply.
V_{SS}	Ground	Ground for the device. Should be connected to ground of the system.
V_{DDQ}	Power Supply	Power supply inputs for the outputs of the device. Should be connected to 1.5V power supply.
NC	NC	No connect

Introduction

Functional Overview

The CY7C1305V25/CY7C1307V25 are synchronous pipelined Burst SRAMs equipped with both a Read Port and a Write Port. The Read port is dedicated to Read operations and the Write Port is dedicated to Write operations. Data flows into the SRAM through the Write port and out through the Read Port. These devices multiplex the address inputs in order to minimize the number of address pins required. By having separate Read and Write ports, the device completely eliminates the need to "turn-around" the data bus and avoids any possible data contention, thereby simplifying system design. Each access consists of four 18/36-bit data transfers in two clock cycles.

Accesses for both ports are initiated on the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and $\overline{K}$) and all output timing is referenced to the output clocks (C and $\overline{C}$, or K and $\overline{K}$ when in single clock mode).

All synchronous data inputs ($D_{[x:0]}$) inputs pass through input registers controlled by the input clocks (K and $\overline{K}$). All synchronous data outputs ($Q_{[x:0]}$) outputs pass through output registers controlled by the rising edge of the output clocks (C and $\overline{C}$ or K and $\overline{K}$ when in single clock mode).

All synchronous control ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS}_{[0:x]}$) inputs pass through input registers. $\overline{RPS}$ and $\overline{WPS}$ are controlled by the rising edge of the input clock (K). $\overline{BWS}_{[0:x]}$ are controlled by the rising edges of input clocks (K and $\overline{K}$).

The following descriptions take CY7C1305V25 as an example. However, the same is true for the other QDR SRAM, CY7C1307V25.

Read Operations

The CY7C1305V25 is organized internally as a 256Kx72 SRAM. Accesses are completed in a burst of four sequential 18-bit data words. Read operations are initiated by asserting $\overline{RPS}$ active at the rising edge of the positive input clock (K). The address presented to Address inputs are stored in the Read address register. Following the next K clock rise the corresponding lowest order 18-bit word of data is driven onto the $Q_{[17:0]}$ using C as the output timing reference. On the subsequent rising edge of $\overline{C}$ the next 18-bit data word is driven onto the $Q_{[17:0]}$. This process continues until all four 18-bit data words have been driven out onto $Q_{[17:0]}$. The requested data will be valid 2.5ns from the rising edge of the output clock (C or $\overline{C}$, 167 MHz device). In order to maintain the internal logic, each read access must be allowed to complete. Each Read access consists of four 18-bit data words and takes 2 clock cycles to complete. Therefore, Read accesses to the device can not be initiated on two consecutive K clock rises. The internal logic of the device will ignore the second Read request. Read accesses can be initiated on every other K clock rise. Doing so will pipeline the data flow such that data is transferred out of the device on every rising edge of the output clocks (C and $\overline{C}$, or K and $\overline{K}$ when in single clock mode).

When the read port is deselected, the CY7C1305V25 will first complete the pending read transactions. Synchronous internal circuitry will automatically three-state the outputs following the next rising edge of the negative output clock ($\overline{C}$). This will allow for a seamless transition between devices without the insertion of wait states in a depth expanded memory.

Write Operations

Write operations are initiated by asserting $\overline{WPS}$ active at the rising edge of the positive input clock (K). On the following K clock rise the data presented to $D_{[17:0]}$ is latched and stored into the lower 18-bit Write Data register provided $\overline{BWS}_{[1:0]}$ are both asserted active. On the subsequent rising edge of the negative input clock ($\overline{K}$) the information presented to $D_{[17:0]}$ is also stored into the Write Data Register provided $\overline{BWS}_{[1:0]}$ are both asserted active. This process continues for one more cycle until four 18-bit words (a total of 72 bits) of data are stored in the SRAM. The 72 bits of data are then written into the memory array at the specified location. Therefore, Write accesses to the device can not be initiated on two consecutive K clock rises. The internal logic of the device will ignore the second Write request. Write accesses can be initiated on every other rising edge of the positive clock (K). Doing so will pipeline the data flow such that 18-bits of data can be transferred into the device on every rising edge of the input clocks (K and $\overline{K}$).

When deselected, the write port will ignore all inputs after the pending Write operations have been completed.

Byte Write Operations

Byte Write operations are supported by the CY7C1305V25. A write operation is initiated as described in the Write Operation section above. The bytes that are written are determined by $\overline{BWS_0}$ and $\overline{BWS_1}$ which are sampled with each set of 18-bit data word. Asserting the appropriate Byte Write Select input during the data portion of a write will allow the data being presented to be latched and written into the device. De-asserting the Byte Write Select input during the data portion of a write will allow the data stored in the device for that byte to remain unaltered. This feature can be used to simplify READ/MODIFY/WRITE operations to a Byte Write operation.

Single Clock Mode

The CY7C1305V25 can be used with a single clock that controls both the input and output registers. In this mode the device will recognize only a single pair of input clocks (K and $\overline{K}$) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/$\overline{K}$ and C/$\overline{C}$ clocks. All timing parameters remain the same in this mode. To use this mode of operation, the user must tie C and $\overline{C}$ HIGH at power-on. This function is a strap option and not alterable during device operation.

Concurrent Transactions

The Read and Write ports on the CY7C1305V25 operate completely independently of one another. Since each port latches the address inputs on different clock edges, the user can Read or Write to any location, regardless of the transaction on the other port. If the ports access the same location at the same time, the SRAM will deliver the most recent information associated with the specified address location. This includes forwarding data from a Write cycle that was initiated on the previous K clock rise.

Read accesses and Write access must be schedule such that one transaction is initiated on any clock cycle. If both ports are selected on the same K clock rise, the arbitration depends on the previous state of the SRAM. If both ports were deselected, the Read port will take priority. If a Read was initiated on the previous cycle, the Write port will assume priority (since Read operations can not be initiated on consecutive cycles). If a Write was initiated on the previous cycle, the Read port will assume priority (since Write operations can not be initiated on consecutive cycles). Therefore, asserting both port selects active from a deselected state will result in alternating Read/Write operations being initiated, with the first access being a Read.

Depth Expansion

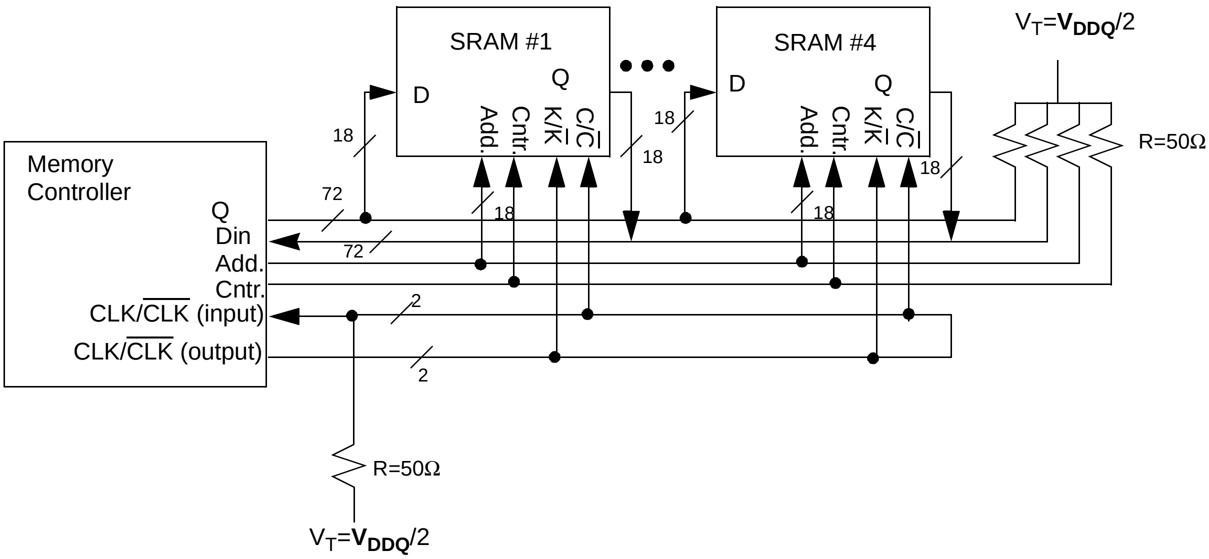
The CY7C1305V25 has a Port Select input for each port. This allows for easy depth expansion. Both Port Selects are sampled on the rising edge of the positive input clock only (K). Each port select input can deselect the specified port. Deselecting a port will not affect the other port. All pending transactions (Read and Write) will be completed prior to the device being deselected.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be 5X the value of the intended line impedance driven by the SRAM, The allowable range of RQ to guarantee impedance matching with a tolerance of ±10% is between 175Ohms and 350Ohms, with V_{DDQ}=1.5V. The output impedance is adjusted every 1024 cycles to adjust for drifts in supply voltage and temperature.

Application Example

CY7C1305V25 in an Application



Note:

2. The above concept applies similarly to the CY7C1307V25.

Truth Table[3,4,5,6,7,8,9]

Operation	K	$\overline{RPS}$	$\overline{WPS}$	DQ	DQ	DQ	DQ
Write Cycle: Load address, input write data on 2 consecutive K and $\overline{K}$ rising edges.	L-H	H[8]	L[9]	D(A+00)at K(t+1) ¦	D(A+01) at $\overline{K}$(t+1) ¦	D(A+10) at K(t+2) ¦	D(A+11) at $\overline{K}$(t+2) ¦
Read Cycle: Load address, read data on 2 consecutive C and $\overline{C}$ rising edges.	L-H	L[9]	X	Q(A+00) at C(t+1) ¦	Q(A+01) at $\overline{C}$(t+1) ¦	Q(A+10) at C(t+2) ¦	Q(A+11) at $\overline{C}$(t+2) ¦
NOP: No operation	L-H	H	H	High-Z	High-Z	High-Z)	High-Z
Standby: Clock stopped	Stopped	X	X	Previous state	Previous state	Previous state	Previous state

Notes:

3. X=Don't Care, H=Logic HIGH, L=Logic LOW ¦represents rising edge.
4. Device will power-up deselected and the outputs in a three-state condition.
5. A represents address location latched by the devices when transaction was initiated. A+00, A+01, A+10 and A+11 represents the addresses sequence in the burst.
6. Data inputs are registered at K and $\overline{K}$ rising edges. Data outputs are delivered on C and $\overline{C}$ rising edges, except when in single clock mode.
7. It is recommended that K = $\overline{K}$ and C = $\overline{C}$ when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
8. If this signal was LOW to initiate the previous cycle, this signal becomes a don't care for this operation.FM
9. This signal was HIGH on previous K clock rise. Initiating consecutive Read or Write operations on consecutive K clock rises is not permitted. The device will ignore the second Read request.

Write Cycle Descriptions (CY7C1305V25) [10]

$\overline{BWS_0}$	$\overline{BWS_1}$	K	$\overline{K}$	Comments
L	L	L-H	-	During the Data portion of a Write sequence, both bytes ($D_{[17:0]}$) are written into the device.
L	L	-	L-H	During the Data portion of a Write sequence, both bytes ($D_{[17:0]}$) are written into the device.
L	H	L-H	-	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
L	H	-	L-H	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
H	L	L-H	-	During the Data portion of a Write sequence, only the upper byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
H	L	-	L-H	During the Data portion of a Write sequence, only the upper byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ will remain unaltered.
H	H	L-H	-	No data is written into the device during this portion of a write operation.
H	H	-	L-H	No data is written into the device during this portion of a write operation.

Note:

10. Assumes a Write cycle was initiated per the Write Port Cycle Description Truth Table. $\overline{BWS_0}$ and $\overline{BWS_1}$ (CY7C1305V25) and $\overline{BWS_2}$ and $\overline{BWS_3}$ (CY7C1307V25) can be altered on different portions of a write cycle, as long as the set-up and hold requirements are achieved.

Write Cycle Descriptions (CY7C1307V25)[10]

$\overline{BWS_0}$	$\overline{BWS_1}$	$\overline{BWS_2}$	$\overline{BWS_3}$	K	$\overline{K}$	Comments
L	L	L	L	L-H	-	During the Data portion of a Write sequence, all the four bytes ($D_{[35:0]}$) are written into the device.
L	L	L	L	-	L-H	During the Data portion of a Write sequence, all the four bytes ($D_{[35:0]}$) are written into the device.
L	H	H	H	L-H	-	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[35:9]}$ will remain unaltered.
L	H	H	H	-	L-H	During the Data portion of a Write sequence, only the lower byte ($D_{[8:0]}$) is written into the device. $D_{[17:9]}$ will remain unaltered.
H	L	H	H	L-H	-	During the Data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ will remain unaltered.
H	L	H	H	-	L-H	During the Data portion of a Write sequence, only the byte ($D_{[17:9]}$) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ will remain unaltered.
H	H	L	H	L-H	-	During the Data portion of a Write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ will remain unaltered.
H	H	L	H	-	L-H	During the Data portion of a Write sequence, only the byte ($D_{[26:18]}$) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ will remain unaltered.
H	H	H	L	L-H		During the Data portion of a Write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ will remain unaltered.
H	H	H	L	-	L-H	During the Data portion of a Write sequence, only the byte ($D_{[35:27]}$) is written into the device. $D_{[26:0]}$ will remain unaltered.
H	H	H	H	L-H	-	No data is written into the device during this portion of a write operation.
H	H	H	H	-	L-H	No data is written into the device during this portion of a write operation.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND ....–0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State[11] ....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage[11]............................–0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW)..20 mA

Static Discharge Voltage.. >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature[12]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	2.5 ±100 mV	1.4V to 1.9V

Electrical Characteristics Over the Operating Range[1,13]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			2.4	2.6	V
V_{DDQ}	I/O Supply Voltage			1.4	1.9	V
V_{OH}	Output HIGH Voltage	I_{OH} = -2.0 mA, nominal impedance		V_{DDQ}/2+0.3	V_{DDQ}	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA, nominal impedance		V_{SS}	V_{DDQ}/2–0.3	V
V_{IH}	Input HIGH Voltage			V_{REF}+0.1	V_{DDQ}+0.3	V
V_{IL}	Input LOW Voltage[11]			–0.3	V_{REF}–0.1	V
I_X	Input Load Current	GND < V_I < V_{DDQ}		-5	5	mA
I_{OZ}	Output Leakage Current	GND < V_I < $V_{DDQ,}$ Output Disabled		-5	5	mA
V_{REF}	Input Reference Voltage	Typical value = 0.75V		0.68	0.95	V
I_{DD}	V_{DD} Operating Supply	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	5.0 ns cycle, 200 MHz		500	mA
			6.0 ns cycle, 167MHz		450	mA
			7.5 ns cycle, 133 MHz		350	mA
			10 ns cycle, 100 MHz		230	mA
I_{SB1}	Automatic Power-Down Current	Max. V_{DD}, Both Ports Deselected, V_{IN} Š V_{IH} or V_{IN} < V_{IL} f = f_{MAX} = 1/$t_{CYC,}$ Inputs Static	5.0 ns cycle, 200 MHz		125	mA
			6.0 ns cycle, 167MHz		100	mA
			7.5 ns cycle, 133 MHz		80	mA
			10 ns cycle, 100 MHz		60	mA

AC Input Requirements Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.	Max.
V_{IH}	Input High (Logic 1) Voltage		V_{REF} + 0.2	–	–
V_{IL}	Input Low (Logic 0) Voltage		–	–	V_{REF} - 0.2

Notes:
11. Minimum voltage equals -2.0V for pulse duration less than 20 ns.
12. T_A is the case temperature.
13. All voltages referenced to ground.

Switching Characteristics Over the Operating Range [1,14,15,16]

Cypress Parameter	Consortium Parameter	Description	-200		-167		-133		-100		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{Power}[17]		V_{CC} (typical) to the first access read or write	10		10		10		10		us
Cycle Time											
t_{CYC}	t_{KHKH}	K Clock and C Clock Cycle Time	5.0		6.0		7.5		10.0		ns
t_{KH}	t_{KHKL}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) HIGH	2.0		2.4		3.2		3.5		ns
t_{KL}	t_{KLKH}	Input Clock (K/$\overline{K}$ and C/$\overline{C}$) LOW	2.0		2.4		3.2		3.5		ns
$t_{KH\overline{K}H}$	$t_{KH\overline{K}H}$	K/$\overline{K}$ Clock rise to $\overline{K}$/K Clock rise and C/$\overline{C}$ to C/$\overline{C}$ rise (rising edge to rising edge)	2.4	2.6	2.7	3.3	3.4	4.1	4.4	5.4	ns
t_{KHCH}	t_{KHCH}	K/$\overline{K}$ Clock rise to C/$\overline{C}$ clock rise (rising edge to rising edge)	0.0	1.5	0.0	2.0	0.0	2.5	0.0	3.0	ns
Set-up Times											
t_{SA}	t_{SA}	Address set-up to clock (K and $\overline{K}$) rise	0.6		0.7		0.8		1.0		ns
t_{SC}	t_{SC}	Control set-up to clock (K and $\overline{K}$) rise ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS_0}$, $\overline{BWS_1}$)	0.6		0.7		0.8		1.0		ns
t_{SD}	t_{SD}	$D_{[17:0]}$ set-up to clock (K and $\overline{K}$) rise	0.6		0.7		0.8		1.0		ns
Hold Times											
t_{HA}	t_{HA}	Address Hold after clock (K and $\overline{K}$) rise	0.6		0.7		0.8		1.0		ns
t_{HC}	t_{HC}	Control signals Hold after clock (K and $\overline{K}$) rise ($\overline{RPS}$, $\overline{WPS}$, $\overline{BWS_0}$, $\overline{BWS_1}$)	0.6		0.7		0.8		1.0		ns
t_{HD}	t_{HD}	$D_{[17:0]}$ Hold after clock (K and $\overline{K}$) rise	0.6		0.7		0.8		1.0		ns
Output Times											
t_{CO}	t_{CHQV}	C/$\overline{C}$ Clock rise (or K/$\overline{K}$ in single clock mode) to Data Valid[15]		2.3		2.5		3.0		3.0	ns
t_{DOH}	t_{CHQX}	Data Output Hold After Output C/$\overline{C}$ clock Rise (Active to Active)	0.8		1.2		1.2		1.2		ns
t_{CHZ}	t_{CHZ}	Clock (C and $\overline{C}$) rise to High-Z (Active to High-Z)[15, 16]		2.3		2.5		3.0		3.0	ns
t_{CLZ}	t_{CLZ}	Clock (C and $\overline{C}$) rise to Low-Z[15, 16]	0.8		1.2		1.2		1.2		ns

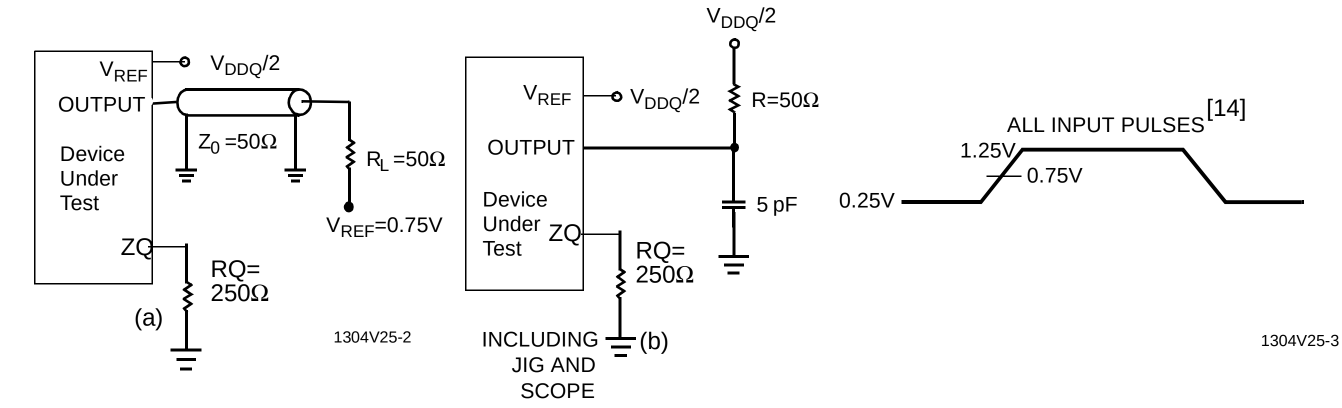
Notes:

14. Unless otherwise noted, test conditions assume signal transition time of 2V/ns, timing reference levels of 0.75V,Vref = 0.75V, RQ = 250 Ohms, V_{DDQ} = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in (a) of AC test loads.
15. t_{CHZ}, t_{CLZ}, are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 100 mV from steady-state voltage.
16. At any given voltage and temperature t_{CHZ} is less than t_{CLZ} and, t_{CHZ} less than t_{CO}.
17. This part has a voltage regulator that steps down the voltage internally; t_{Power} is the time power needs to be supplied above V_{DD} minimum initially before a read or write operation can be initiated.

Capacitance[18]

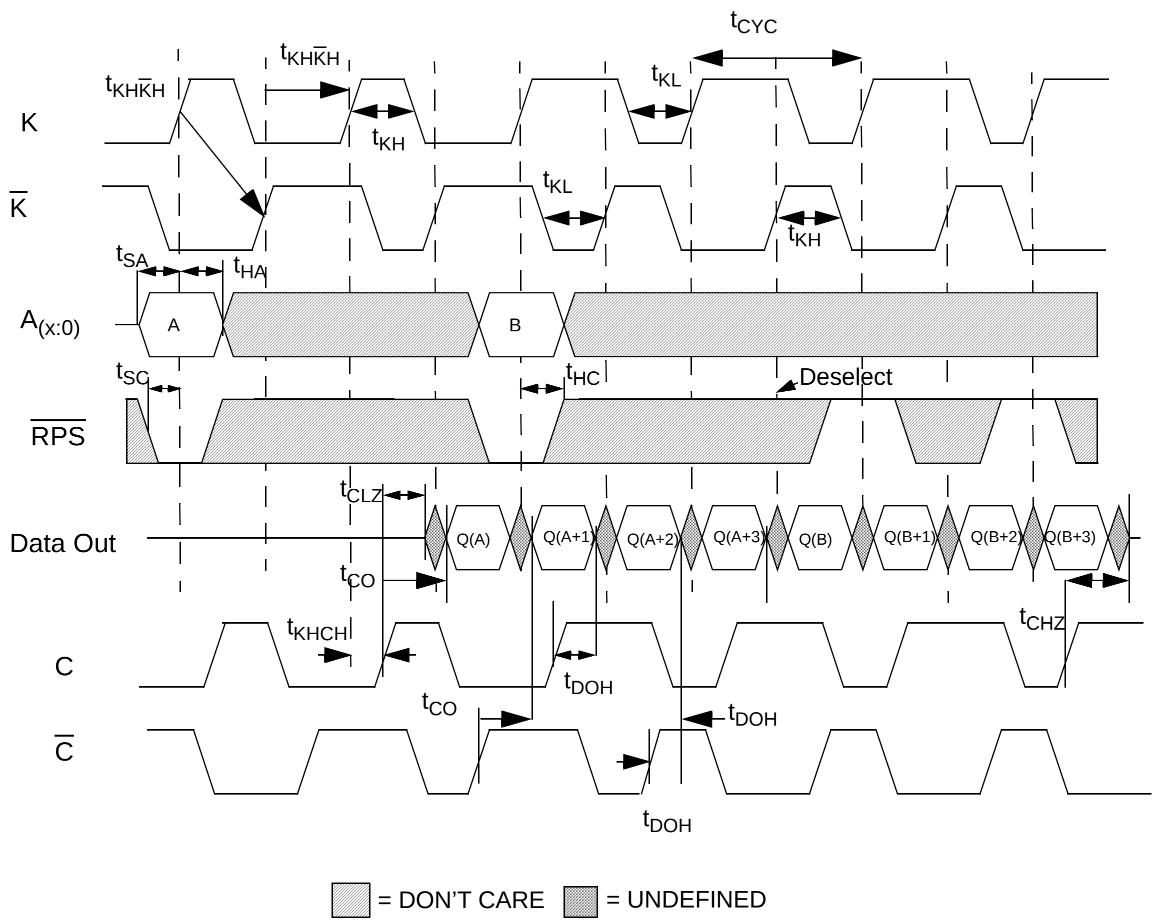
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25×C, f = 1 MHz, V_{DD} = 2.5V. V_{DDQ} = 1.5V	3	pF
C_{CLK}	Clock Input Capacitance		3	pF
C_O	Output Capacitance		3	pF

Note:
18. Tested initially and after any design or process change that may affect these parameters.



Switching Waveforms

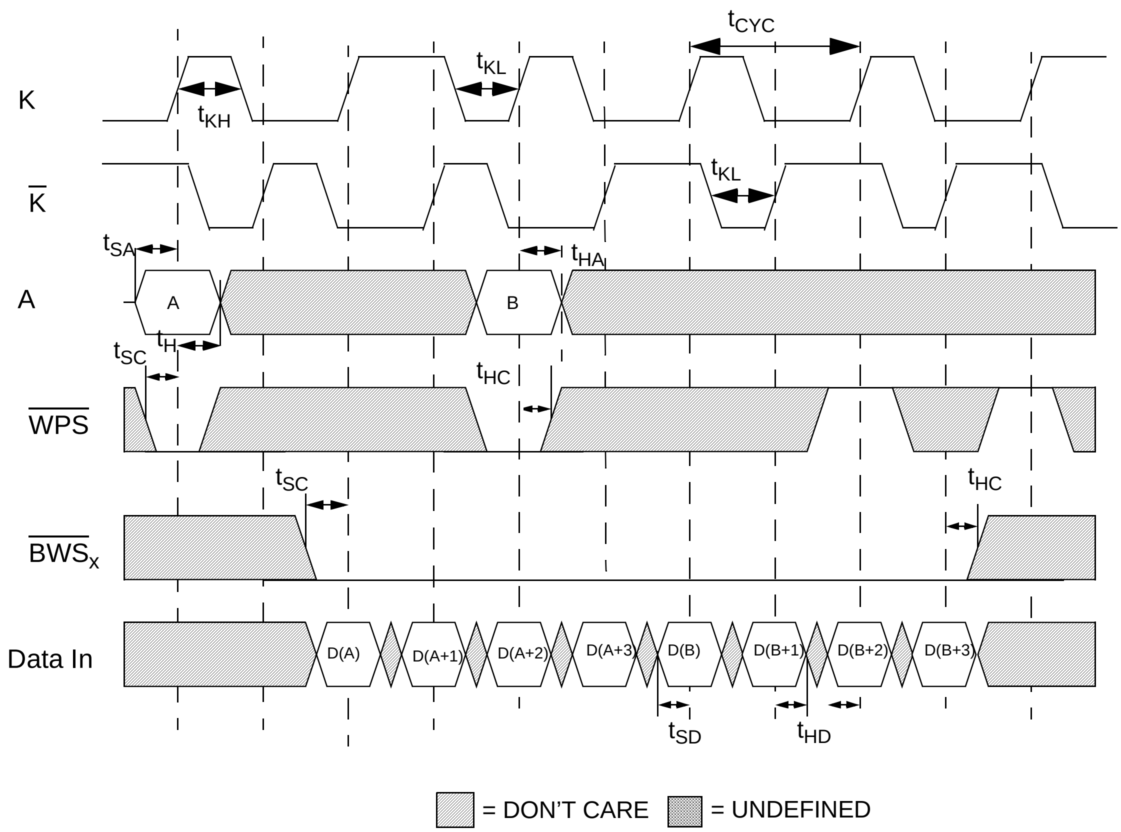
Read/Deselect Sequence [19]



Note:
19. Device originally deselected.

Switching Waveforms

Write/Deselect Sequence [20,21]

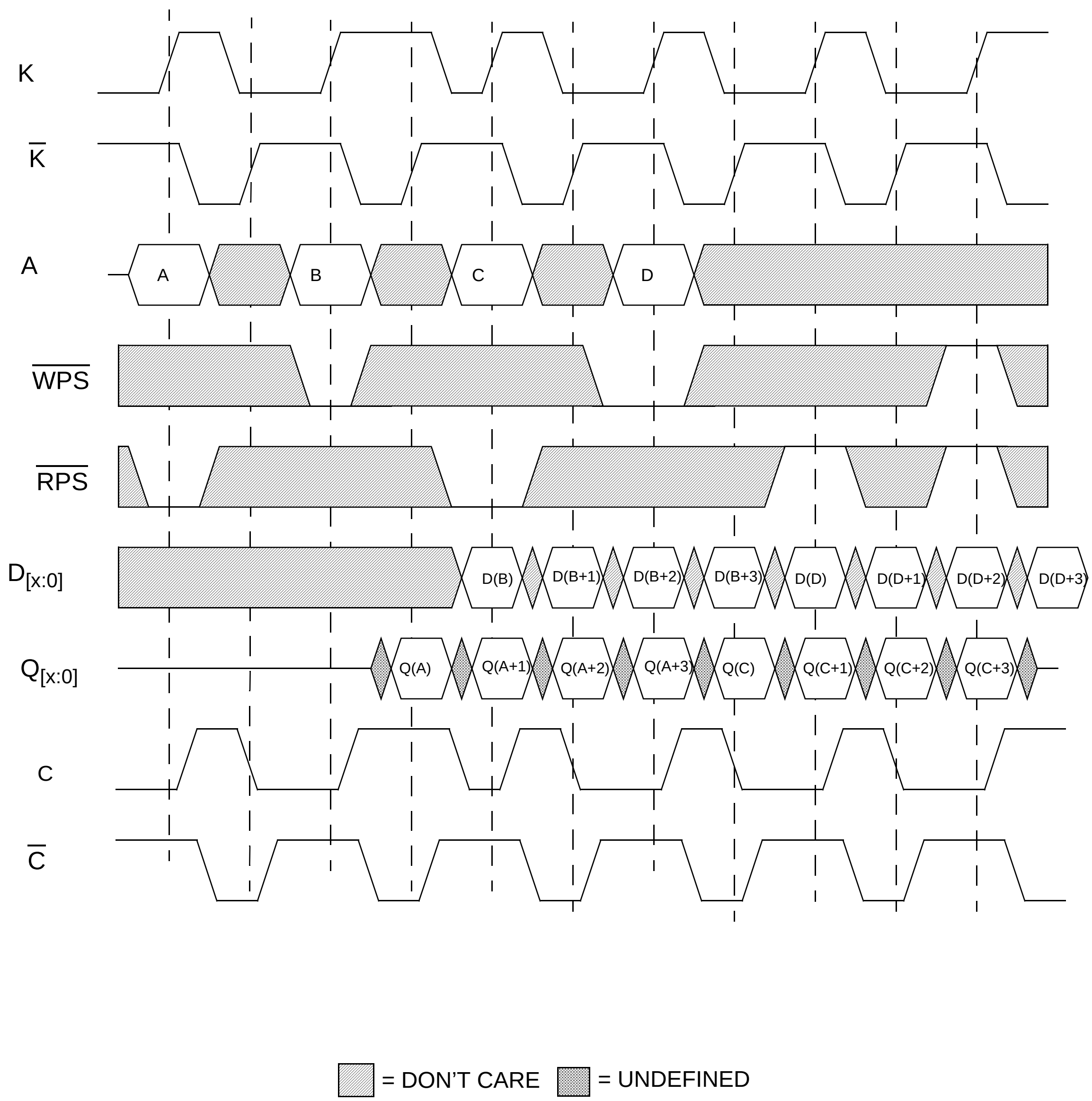


Notes:

20. C and $\overline{C}$ reference to Data Outputs and do not affect Writes.
21. Activity on the BWS_x LOW = Valid, Byte writes allowed, see Byte write table for details.

Switching Waveforms

Read/Write/Deselect Sequence[22,23]



Notes:

22. Read Port previously deselected.
23. $BWS_{[1:0]}$ both assumed active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan test access port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard #1149.1-1900. The TAP operates using JEDEC standard 1.8V I/O logic levels.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

Test Access Port–Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

Test Data-Out (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine (see Instruction codes). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating. At power-up, the TAP is reset internally to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in TAP Controller Block Diagram. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture IR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all of the input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Code table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High-Z state until the next command is given during the “Update IR” state.

SAMPLE/PRELOAD

SAMPLE / PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE / PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE / PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD allows an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required - that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

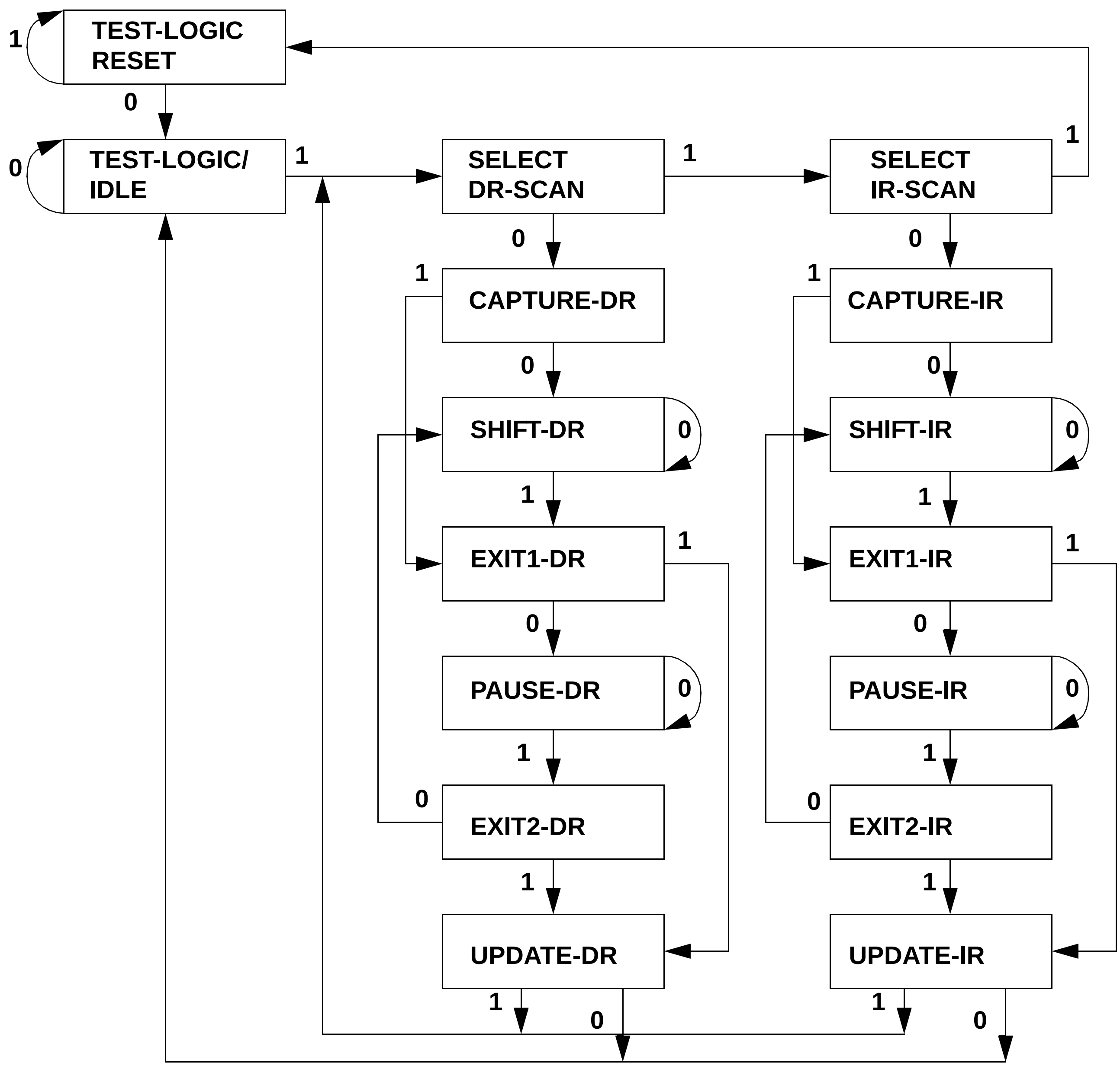
The boundary scan register has a special bit located at bit #47. When this scan cell, called the "extest output bus tristate", is latched into the preload register during the "Update-DR" state in the TAP controller, it will directly control the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it will enable the output buffers to drive the output bus. When LOW, this bit will place the output bus into a High-Z condition.

This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the "Shift-DR" state. During "Update-DR", the value loaded into that shift-register cell will latch into the preload register. When the EXTEST instruction is entered, this bit will directly control the output Q-bus pins. Note that this bit is pre-set LOW to enable the output when the device is powered-up, and also when the TAP controller is in the "Test-Logic-Reset" state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

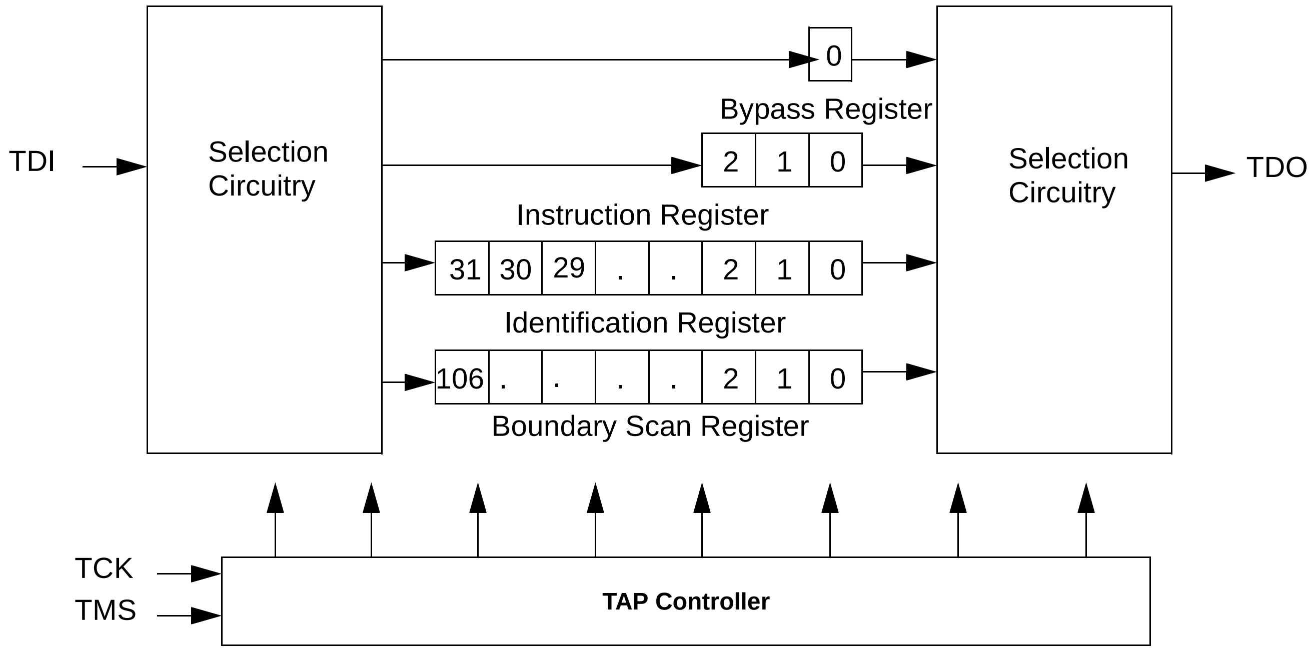
TAP Controller State Diagram[24]



Note:

24. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

TAP Controller Block Diagram



TAP Electrical Characteristics Over the Operating Range[13, 25, 26]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –2.0 mA	1.7		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 2.0 mA		0.7	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.7	V
I_X	Input and Output Load Current	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA

Notes:

25. Overshoot: V_{IH}(AC)≤V_{DD}+0.5V for t≤t_{TCYC}/2. Undershoot V_{IL}(AC)≤0.5V for t≤t_{TCYC}/2. Power-up: V_{IH}<2.6V and V_{DD}<2.4V and V_{DDQ}<1.4V for t<200 ms.
26. These characteristic pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the Electrical Characteristics Table.

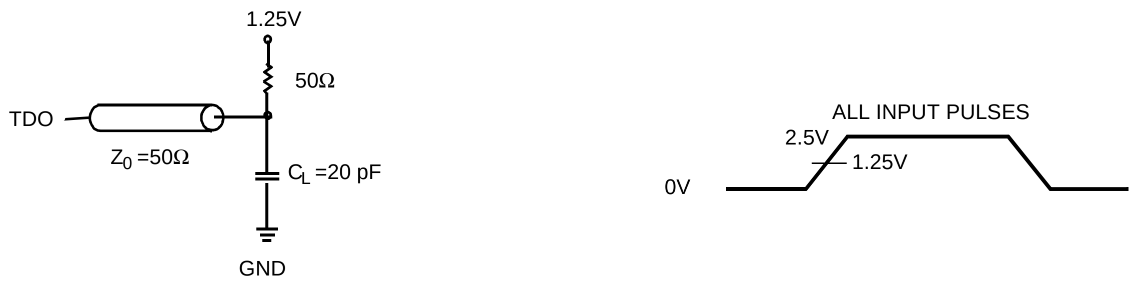
TAP AC Switching Characteristics Over the Operating Range [27,28]

Parameter	Description	Min.	Max.	Unit
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TF}	TCK Clock Frequency		10	MHz
t_{TH}	TCK Clock HIGH	40		ns
t_{TL}	TCK Clock LOW	40		ns
Set-up Times				
t_{TMSS}	TMS set-up to TCK clock rise	10		ns
t_{TDIS}	TDI set-up to TCK clock rise	10		ns
t_{CS}	Capture set-up to TCK rise	10		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK clock rise	10		ns
t_{TDIH}	TDI Hold after clock rise	10		ns
t_{CH}	Capture Hold after clock rise	10		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO valid		20	ns
t_{TDOX}	TCK Clock LOW to TDO invalid	0		ns

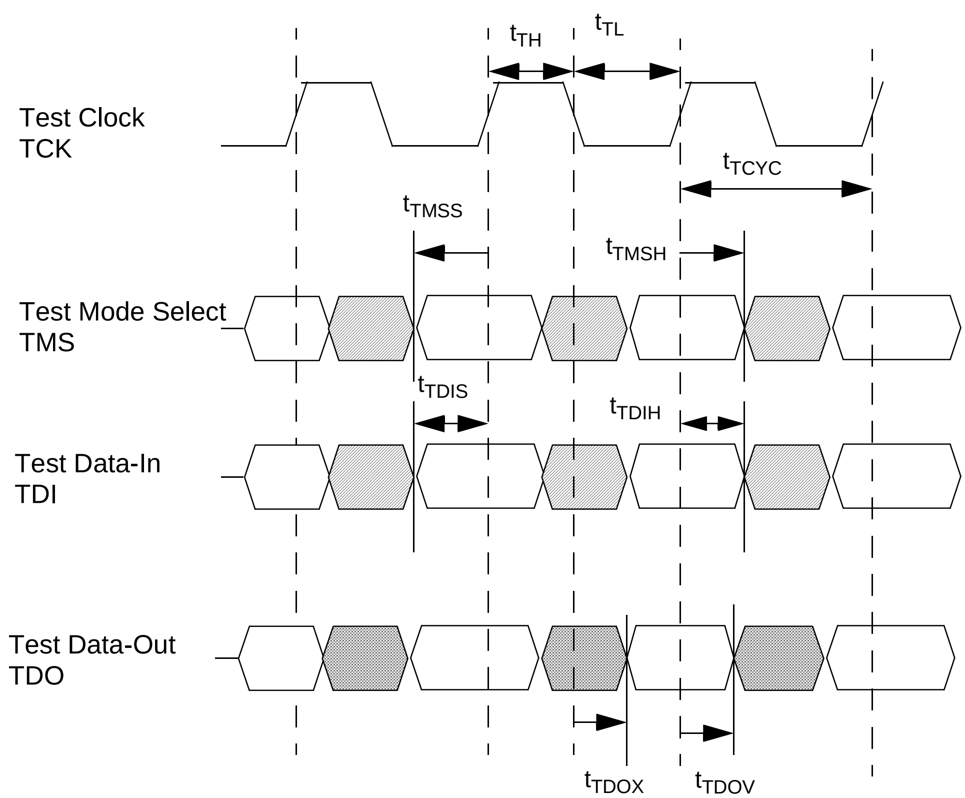
Notes:

27. Parameters t_{CS} and t_{CH} refer to the set-up and hold time requirements of latching data from the boundary scan register.
28. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

TAP Timing and Test Conditions[28]



(a)



Identification Register Definitions

Instruction Field	Value		Description
	CY7C1305V25	CY7C1307V25	
Revision Number (31:29)	000	000	Version number.
Cypress Device ID (28:12)	01011010011010101	01011010011100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100		Allows unique identification of SRAM vendor.
ID Register Presence (0)	1		Indicate the presence of an ID register.

Scan Register sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the Input/Output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the Input/Output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the Input/Output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

Boundary Scan Order

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N

Boundary Scan Order

Bit #	Bump ID
5	7R
6	8R
7	8P
8	9R
9	11P

Boundary Scan Order

Bit #	Bump ID
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B

Boundary Scan Order

Bit #	Bump ID
46	11A
47	Internally Pre-set LOW
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	Internally Pre-set LOW
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G

Boundary Scan Order

Bit #	Bump ID
82	2G
83	1J
84	2J
85	3K
86	3J
87	2K
88	1K
89	2L
90	3L
91	1M
92	1L
93	3N
94	3M
95	1N

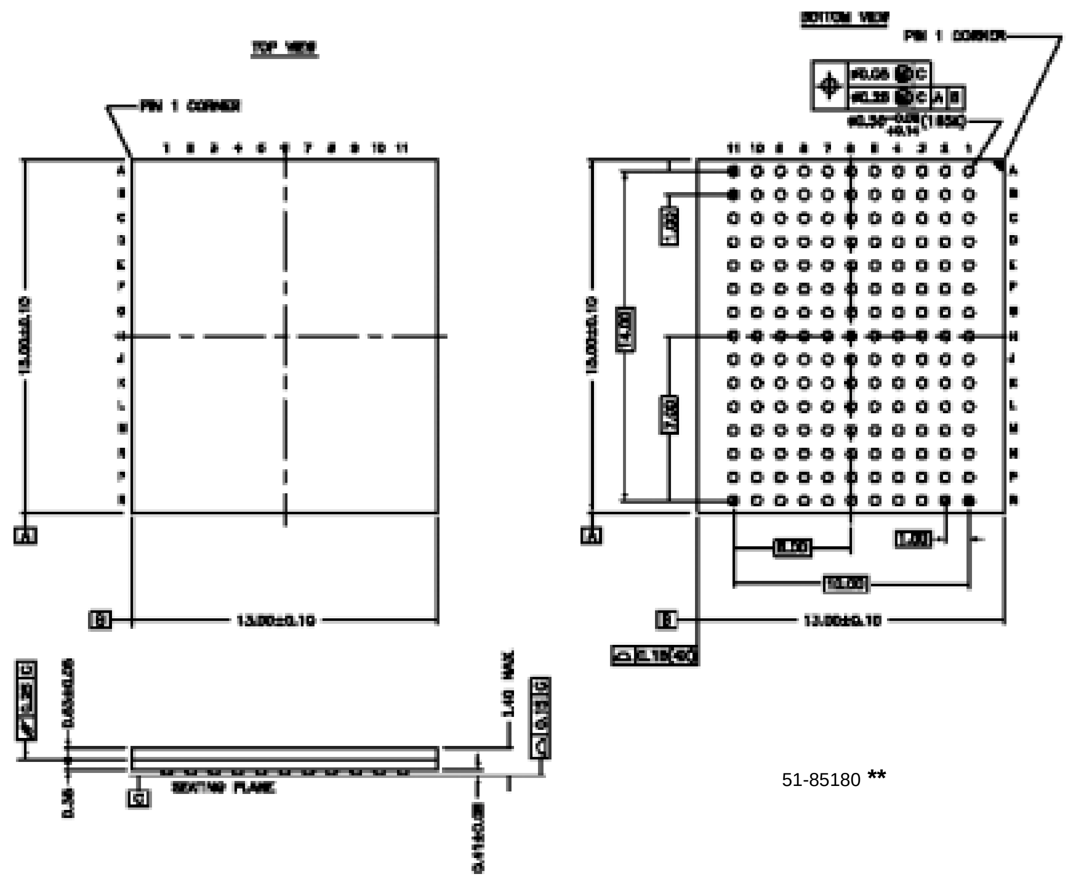
Boundary Scan Order

Bit #	Bump ID
96	2M
97	3P
98	2N
99	2P
100	1P
101	3R
102	4R
103	4P
104	5P
105	5N
106	5R

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
200	CY7C1305V25-200BZC	BB165D	13 x 15 mm FBGA	Commercial
	CY7C1307V25-200BZC			
167	CY7C1305V25-167BZC	BB165D	13 x 15 mm FBGA	
	CY7C1307V25-167BZC			
133	CY7C1305V25-133BZC	BB165D	13 x 15 mm FBGA	
	CY7C1307V25-133BZC			
100	CY7C1305V25-1300BZC	BB165D	13 x 15 mm FBGA	
	CY7C1307V25-100BZC			

165-ball FBGA (13 x 15 x 1.4 mm) BB165D



51-85180 **

Document Title: CY7C1305V25 / CY7C1307V25 18Mb Burst of 4 Pipelined SRAM with QDR Architecture Document Number: 38-05099				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107654	07/10/01	SKX	New Data Sheet
*A	122949	03/14/03	RCS	1. Changed Status to Preliminary from Advanced Information (All Pages) 2. Added Ex-Test feature to JTAG. This implementation is backwards compatible with the previous Non-Ex-Test feature set. (Page 19 and 24) 3. Changed Boundary Scan Order to 106 Cells from 69 (Page 24, 25 and 26) 4. Changed Cells 47 and 63 to an Internal Cells that are Pre-Set to LOW in the Boundary Scan Order. Note that these pins are 100% compatible with the previous scan order because they had previosly been connected to V_{SS}. (Page 25) 5. Specified minimum and maximum input voltages for AC conditions. (Page 12) 6. Changed packaged height to 1.4 mm from 1.2 mm. (Page 27) 7. Changed ball diameter to 0.5 mm from 0.45 mm. (Page 27) 8. Added t_{Power} specification and note 17. These devices require 10 us of of V_{DD} above V_{DD} minimum (2.4V) before operating. (page 13)